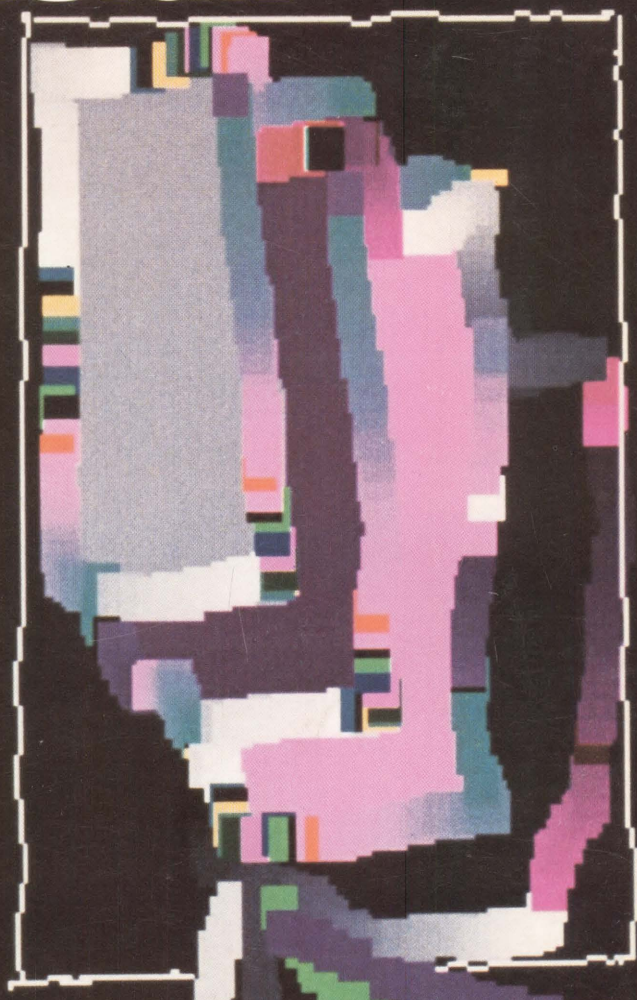
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NOV. 1981

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

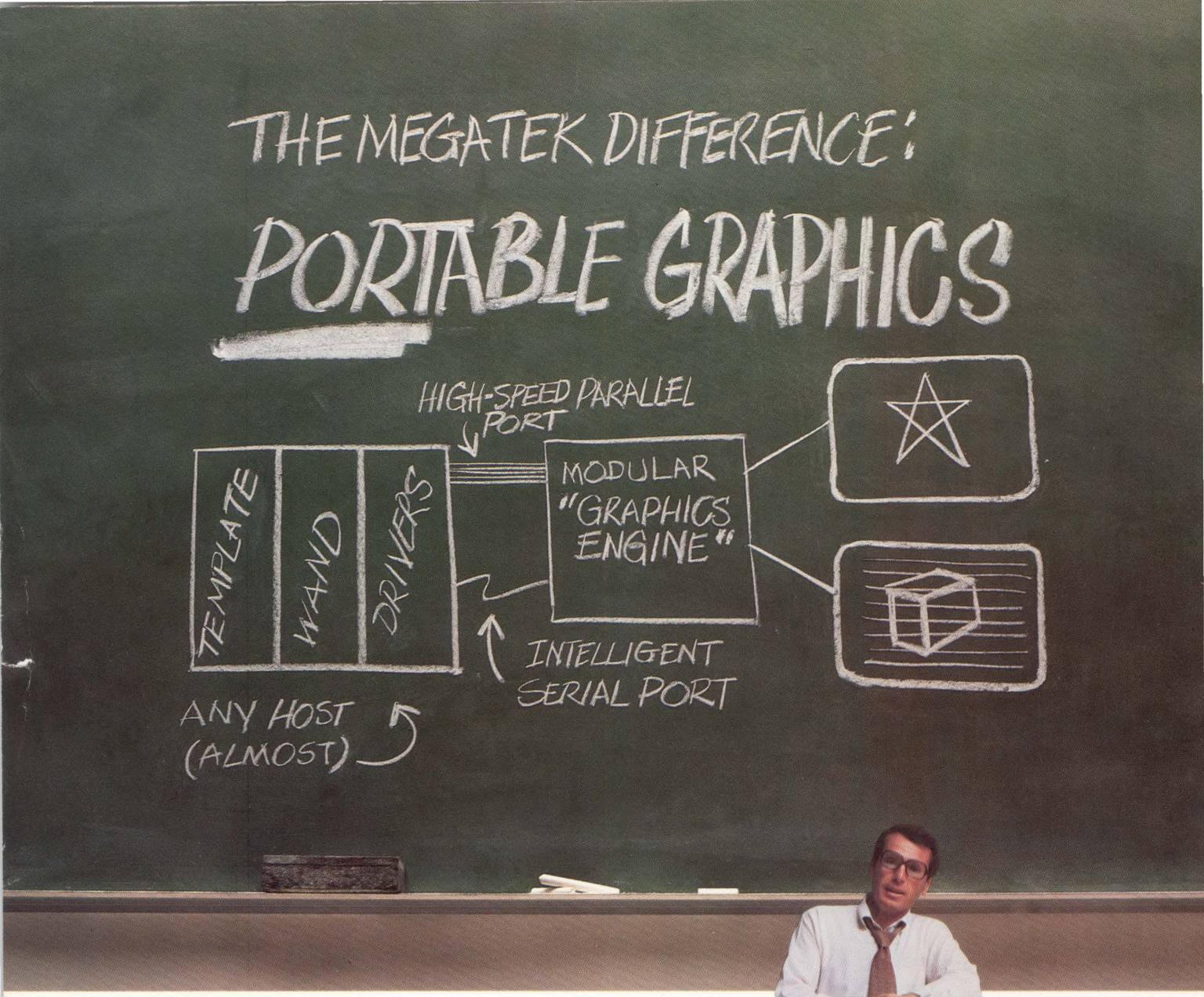


SPECIAL REPORT: CONTROL & AUTOMATION

FLEXIBLE PROCESSOR EXTENDS DESIGN OPTIONS

RAPID BUS MULTIPROCESSOR SYSTEM

ARRAY PROCESSOR SPEEDS DATA CONVERSION



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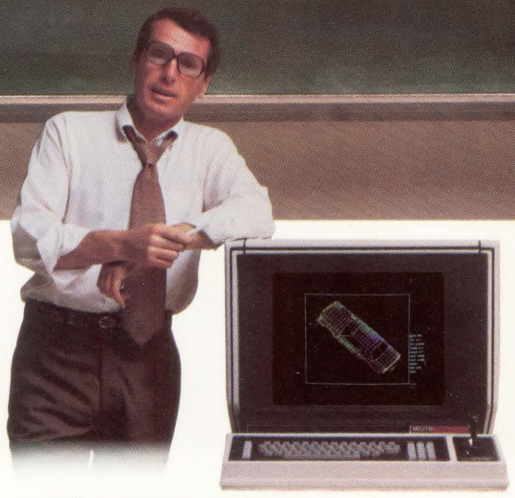
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CIRCLE 3 ON INQUIRY CARD

UP FRONT

West Coast Managing Editor named

Thomas R. Williams has been appointed West Coast Managing Editor for *Computer Design*. Before joining *Computer Design*, he was Computers and Peripherals Editor for *Electronic Design* magazine.

Active in journalism since the early days of personal computing, Williams was Editor of *Dr. Dobb*'s *Journal* and later the founding Editor in Chief of *InfoWorld*. Previously, he taught English and English literature in Ahaus, West Germany. He earned his Bachelor's degree at the University of Missouri and at Bonn University, in Germany, and his Master's degree at Washington University.

Tom has set up *Computer Design*'s Western editorial office at 540 Weddell Dr, Suite 8, Sunnyvale, CA 94086 (Tel: 408/745-0715).

Computer Society Tutorial Week is exported to Europe

Tutorial Week Europe '82, an expansion of the IEEE Computer Society's semiannual U.S. counterparts, will be held next April 24 to 28 in Hanover, Germany, concurrently with Hanover Fair. Discussion tracks will cover VLSI technology, computer graphics, software design and test, and local networks and office automation. Program and registration information can be obtained from Tutorial Week Europe, PO Box 639, Silver Spring, MD 20901.

Program generator decreases development time

Indicative of the new wave in cutting through the programming language barrier, an interactive program generator called I*COPS is claimed to decrease COBOL program development time by 25% to 60%. All that is required to learn to write programs is an understanding of COBOL and one hour of training. Information is available from Labyrinth Systems, Ltd, PO Box 99, Great Neck, NY 11022.

Forth aids discovery of hole in outer space

Astronomers at Arizona's Kitt National Observatory and Mount Hopkins Observatory who discovered a void in the universe that could hold 2000 Milky Way size galaxies used Forth programming methodology to position their telescopes and to transcribe telescopic images into computer terms. A Forth based data acquisition unit transfers telescopic images onto computer tape for study by astronomers and computer analysts to chart actual positions of stars in the universe.

Line card chip to obsolete single- and multi-chip filter/codecs

That's the claim from the Semiconductor Components Group (SCG) of Northern Telecom Ltd. In conjunction with Bell-Northern Research, this group has developed the LSI E99 line card chip that integrates most of the functions of a digital line card on the same chip as the filter/codec. In addition, the device monitors busy or idle states of the telephone set, controls the ringing function, and provides automatic impedance matching and gain switching to accommodate a wide variety of subscriber loop conditions. The chip also provides a digital interface to the control processors of the firm's DMS-100 family of digital switching systems and allows centralized testing of subscriber loops. Northern Telecom SCG plants in Ottawa and San Diego are expected to produce nearly two million such chips by 1983.

Surprise U.S. trio unveils bus structure at European show

A new microprocessor bus standard has been jointly announced by Mostek, Motorola, Signetics/Philips, and Thompson of France. Called the VME bus, the standard will meet the DIN 41612 and 41494 single- and double-Eurocard mechanical standards. The VME system supports single- and multiprocessor systems and microprocessor architectures up to 32 bits of address and 32 bits of data, allows block mode and data transfers up to 20M bytes/s, and provides non-multiplexed asynchronous data transfer protocol. All companies involved will announce independently developed products based on the VME bus.

Pretriggers

Peripherals

The 4113, latest member of Tektronix's 4110 series of intelligent display terminals, combines raster color capability with local intelligence. It melds a 19″, 60 Hz, 640 x 480 color display with all the pan, zoom, and viewport features of the monochrome 4112 raster display, plus compatibility with the high resolution 4114 storage tube display.

Building a graphics terminal with nonvolatile bubble memory inside takes it off the desk and puts it into aircraft, according to Industrial Data Terminals.

A dot matrix one-printer solution, developed by Centronics, operates in either high speed draft mode or high quality dual-pass mode to meet small business computer needs.

Data Base Machine takes an architectural approach that CSSN claims breaks through cost barriers to treat database technology as a separate system function.

Computers

A step toward fulfilling the prediction that by 1985 all computer systems will have to be easy to use, Microdata's Sequel™ large business computer system "boasts unparalleled ease of use and the world's first automatic application software generator"—ALL. As many as 127 interactive terminals can be operated simultaneously on the system.

Interface

Both mass storage and its backup are controlled by a single-board Q-bus controller from Andromeda that emulates DEC's Winchester and floppy disc units.

Software

Desnet, a local area network that allows use of different microcomputers as well as a choice of network media, has been developed by the Destek Group. It consists of a network control interface that contains S-100 bus decoding logic, timing control, and DMA control, as well as a parallel and serial port. For systems without DMA, a version with internal serial communication is available.

Data conversion

REMDACS II, a 2-wire modular remote data acquisition and control system from Intersil, features preprogrammed microcomputer controlled cards located close to the signal source or control point. Remote cards are linked to a central receiver/transmitter card. System cards include analog and digital remote stations, motherboards, digital peripheral cards, receiver/transmitter, and accessories.

Communications

A second generation single-chip PCM line filter from Intel operates at lower power and with less noise than its predecessor.

Test & measurement

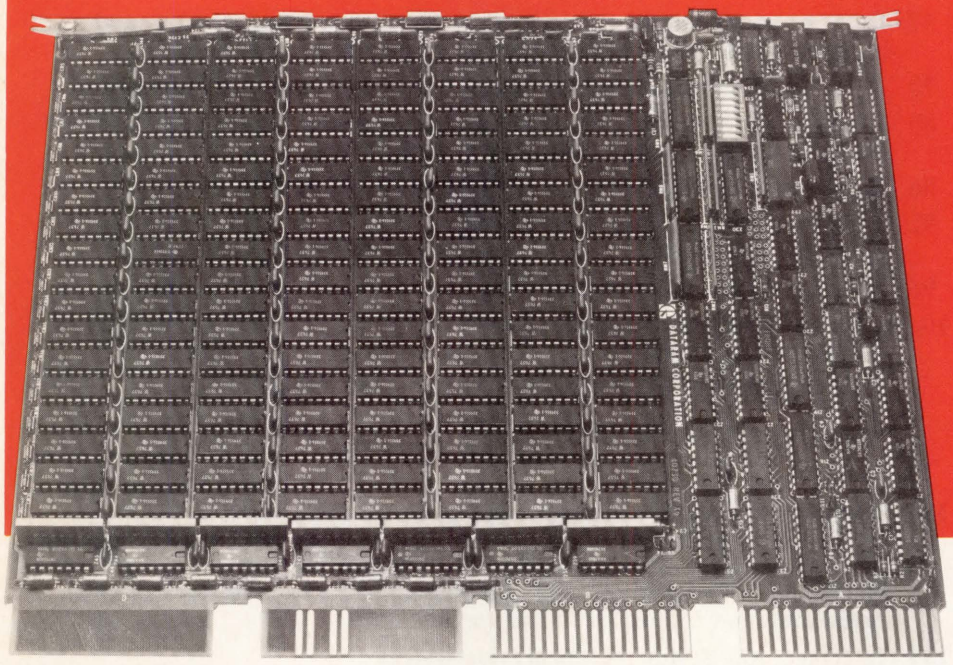
GenRad's family of in-circuit testers has been expanded to accommodate 960- and 3584-pin boards. Complementary software enhancements and a new programming station are also offered.

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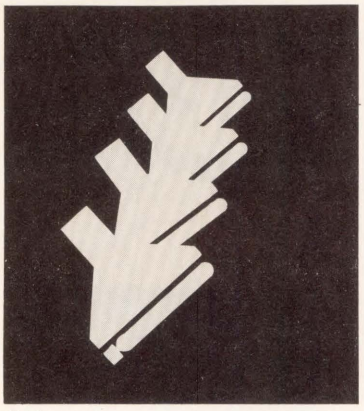
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COMPUTER DESIGN®

System technology



96 *Slight variations in curvature of vibrating mirror produce 3-D display, allowing operator to see different perspectives by moving his head in relation to image*

30 Control & automation: **Low cost, lightweight robot performs industrial functions**
Servo controller adds speed, accuracy to programmable controller
P/ROM based control system operates in harsh environments

48 Microprocessors/microcomputers: **Desktop computer allows users to develop and display graphics**

57 Data communications: **Processors, workstations, interface chip, and personal computer local network aim at the office environment**

70 Interface: **Graphics controller offers dual mode image array selection**

80 Development systems: **Instrument speeds firmware integration for mixed bit slice/microprocessor systems**

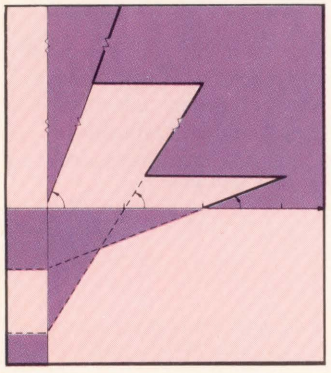
86 Computers: **32-bit mini fits both technical/commercial areas**

92 System elements: **Charge-coupled device chips form high resolution image array assemblies**

96 Peripherals: **Graphics and imaging system presents true 3-D display**

104 Test & measurement: **Access to internal computer expands versatility of 64-channel logic analyzer**
Universal qualifier simplifies testing of storage module drives

System design



203 *In data conversion computation, floating point data, treated as single-word numbers with exponent in MSB and mantissa in LSB, are plotted against horizontal axis*

181 Computers: **Flexible processor extends design options**
by Anthony Lake, Philip Herman, Jr, and Michael Kraley—The concept of a microprogrammable building block permitting user access to the controlling microcode results in an adaptable CPU architecture that can be tailored and refined to fit the application

189 Interface: **RAPID Bus multiprocessor system**
by Mario P. Zoccoli and Arthur C. Sanderson—The combination of a powerful 16-bit microprocessor with a high speed ECL bus yields a versatile, reliable, and economical multiprocessor system

203 Data Conversion: **Array processor speeds data conversion**
by Ching-Ming Lai—Treating the exponent and mantissa of a floating point number as a single 16-bit number provides the speed benefits of integer handling while still achieving the wide dynamic range of floating point representation

209 Software: **Software piracy and the copyright laws**
by Richard H. Stern—Although 1980 amendments to the 1976 Copyright Act attempted to provide some protection for object programs, the actual extent of that protection will not be known until after considerable litigation of the issue

217 Data communications: **TDMA increases SATCOM efficiency**
by Joseph H. Deal—Time division multiple access technology applied to satellite communications simplifies earth station configuration and provides more efficient use of satellite transponder capacity

225 Peripherals: **Laser scribing on magnetic disc**
by Sam R. Cowan and David L. Peterson—Laser technique manufactures "bad" discs for calibrating disc test equipment

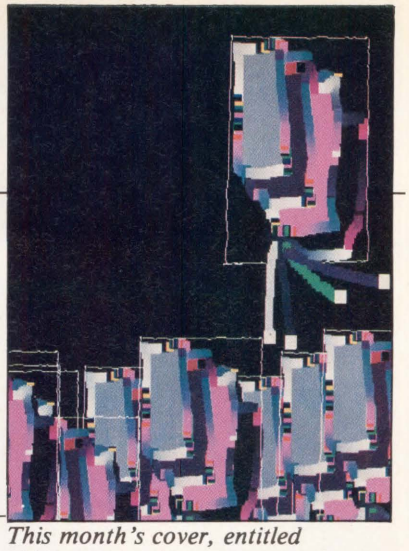
233 Integrated circuits: **VMOS transistors interface ICs to high power loads**
by Bill Roehr—Several precautions, not obvious at first glance, must be taken when VMOS transistors are used to interface high power loads with ICs

245 Software: **Compiler optimization techniques**
by Armond Inselberg and Stan Mazor—Techniques used within the PL/M-86 compiler make the programmer's job easier while supplying highly efficient code

Vol 20, No 11
Nov 1981

Special report on control & automation

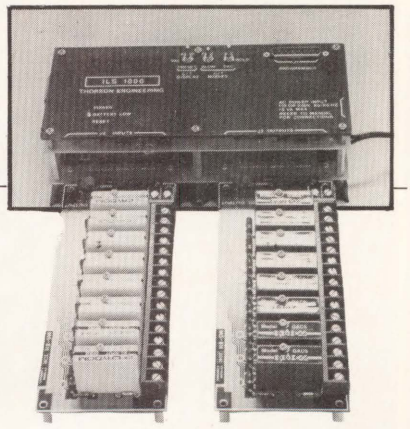
109 Included are a trend report on digital process control; use of CAD in analog PCB layouts; a unique touch pad for harsh environments; an intelligent A-D; use of voice synthesis in monitoring; an airborne data acquisition system using commercial equipment; and a survey of approaches to computerized vision



This month's cover, entitled "Automation," was generated using a Digital Effects VP-3 and D-48 color printer by Larry Gartel

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Editorial reviewer for this issue: Brian W. Pollard

*Appearing in Domestic issues only.

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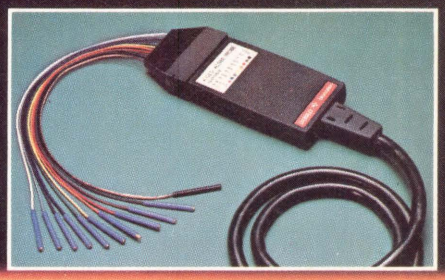
With its 50 MHz clock rate, 48-channel recording and 16 triggering levels, the K101-D isolates software bugs faster and more precisely than ever before. Sophisticated disassembly firmware generates precise mnemonics that cut analyzing time. And 12 external clocks (AND or OR) let you demultiplex 16-bit microprocessors, 16- and 32-bit minicomputers and bit-slice processors.

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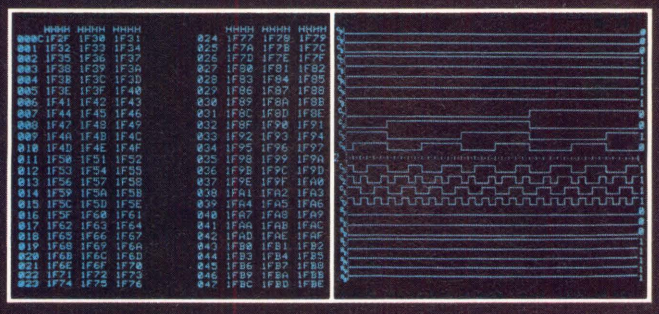
The K101-D's advanced high-performance hybrid probes let you capture glitches as narrow as 5 ns. And, with 48-channel recording, 515-word memory and 16-level triggering, you'll trap the data you need. The convenient display formatting and expansion simplify analysis.

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For powerful hardware debugging, K101-D time domain capabilities include 100 MHz clocking, 48-channel recording, 515-word memory, 5-ns glitch capture, 16-level triggering, channel labeling, new high-performance probe design, as well as horizontal and vertical display expansion for easy reading.

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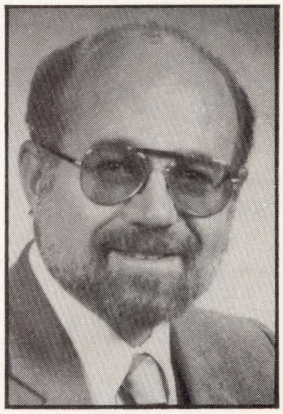
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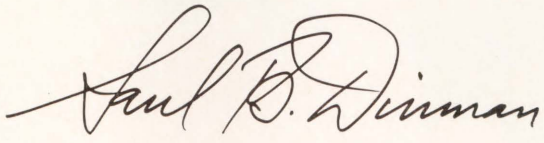
THE THREE NEW FACES OF SYSTEM SOFTWARE



All providers and users of computer based systems are equally and painfully aware of the "software bottleneck." Now, with little machines being pushed by big companies into the hands of more and more "just plain folks," the problem is only going to become more painfully obvious.

As has always been the case, if enough technical people become aware of product needs, there are ample solutions that can fill the gap in a remarkably short time. Thus we see the three new faces of system software emerging. The name of the game is to let the user without a computer science degree do it his own way. Table driven, generalized packages—although conceptually not new—are beginning to appear feasible because of ever increasing throughputs and receding memory costs. High level languages seem to be proliferating again for the same reasons, with definite overtones of natural and specialty or vertical languages. In fact, one of the strongest stimuli for the language area is coming via database development activity; everybody is getting into the act with query languages, report writers, and the like that will run on even the smallest micros. Finally, another approach revisited because of today's economy is the program generator. Rap sessions held at a terminal cause the machine to churn out actual source code programs in BASIC, FORTRAN, etc.

Which one will be the winner? Maybe it will be a combination of all three, or perhaps even a machine structure that directly executes a high level language. That last concept is a real sleeper, which, in light of the complexity of low cost hardware and memory available today, must already be setting some fertile minds to mull over the possibilities of directly executing non-machine architecture related instruction sets.



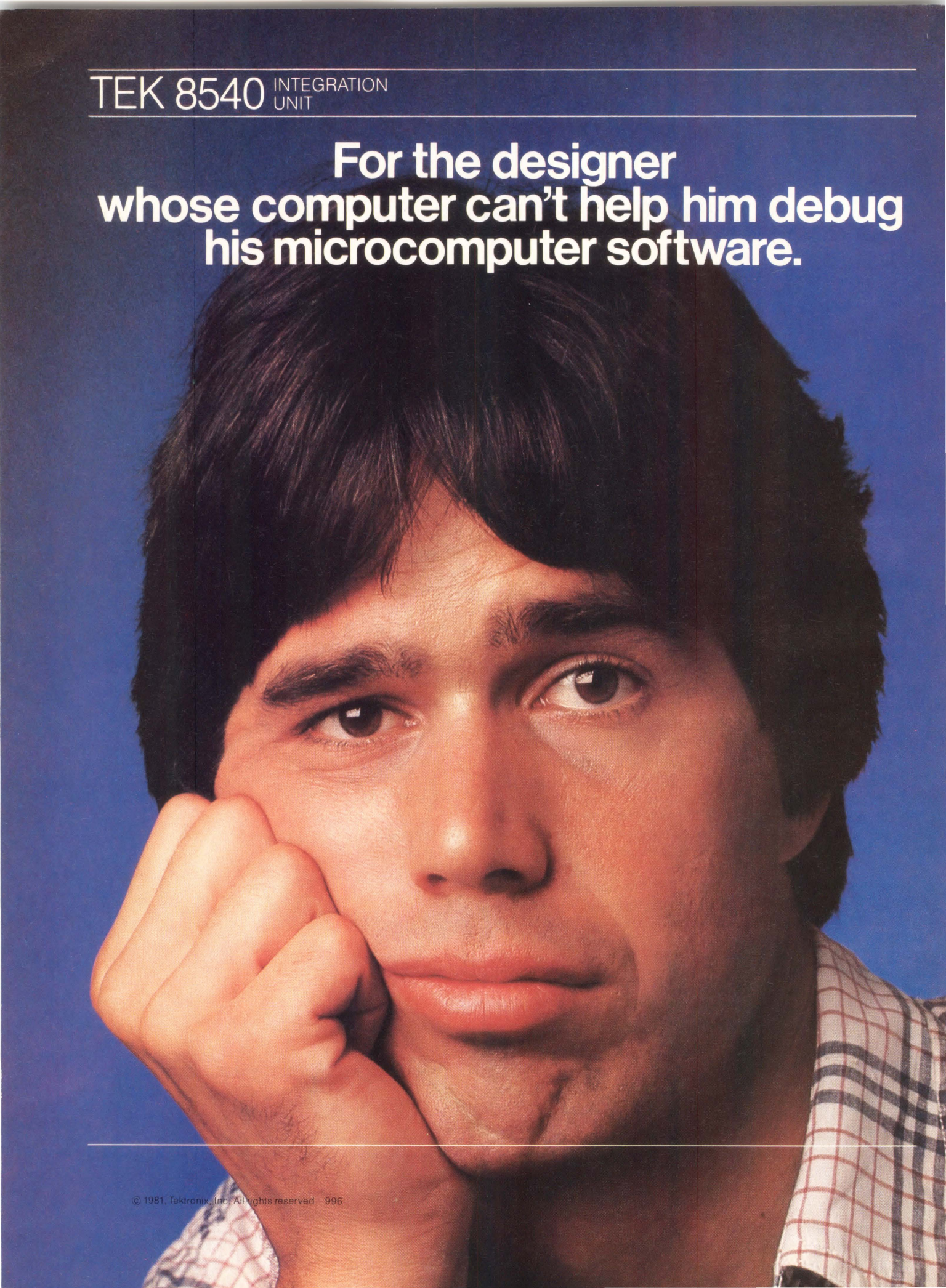
Saul B. Dinman
Editor in Chief

Best Technical Article of the Month—June
"Forth—The Language of Machine Independence"
Gary Feierbach, Inner Access Corporation

This article will now compete with other monthly winning articles for the 1981 Windjammer cruise award.

TEK 8540 INTEGRATION UNIT

For the designer whose computer can't help him debug his microcomputer software.



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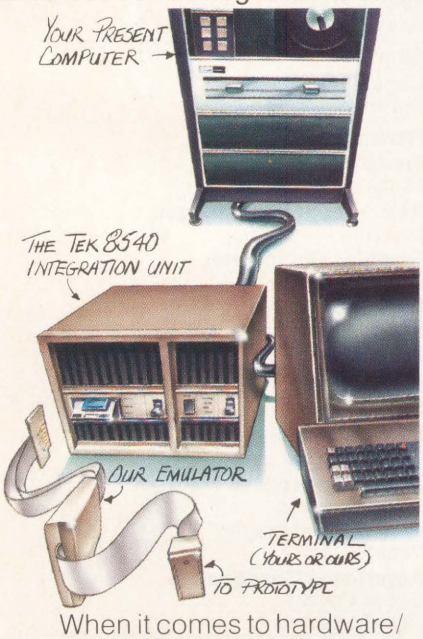
Tek announces the 8540 Integration Unit.

When designing with microcomputers, your resident host computer can be a powerful ally in the fight against impossible design schedules.

But, ultimately, it only gets half the job done.

Even though it gives you everything you need for fast, accurate code development, you still have to install and debug your developed code in the prototype hardware. A process that often consumes half your total design time.

Enter the 8540 Integration Unit.



When it comes to hardware/software integration, Tektronix has the answer. The 8540 Integration Unit. It interfaces easily with almost any host computer using ASCII terminal communications. And, once connected, its high-performance emulators and debug software handle the entire integration process.

All with an unmatched range of chip support.

Your host & the 8540: A synergistic team.

The 8540's sophisticated interface features make the most out of your host's processing power. Like the ability to download symbolic debug tables along with object code to the 8540. Or permanently store your specialized, host-oriented debug commands aboard the 8540 as either key words or command strings.

```
> BK 1 LOOP

> GO BEGIN

LOC    INST                R0   R1   R2   R3   R4   R5   R6   R7    FCW
                           R8   R9   R10  R11  R12  R13  R14  R15

SECTION1:000B50 LOOP
000B50 8D07              NOP
                         0002 0000 0000 4000 0000 0B62 0000 0000   5000
                         0000 0326 0000 0000 804F 0000 0000 407C

        (BREAK     BKPT1)

> DS
PC=000B50

  R0=0002  R1=0000   R2=0000   R3=4000   R4=0000   R5=0B62   R6=0000   R7=0000
  R8=0000  R9=0326  R10=0000  R11=0000  R12=804F  R13=0000  R14=0000  R15=407C

  FCW          Sys EPA VI    NVI . . .    C Z S P/V    D H . .          REFRESH
  5000       x  1   0  1     0  x x x     0 0 0  0     0 0 x x            0

  PSAP  (Offset)  = 1Dxx
  Sys  Stack (S15) = 407C          System Mode
  Norm Stack (N15) = 47FE
```

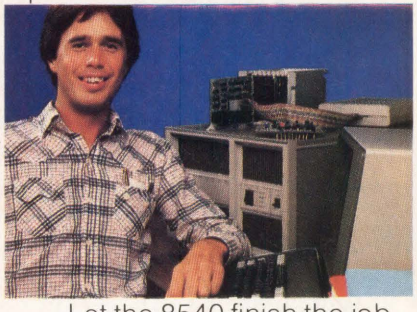
Breakpoint halts program execution at the address label "LOOP." Also shown is a detailed description of the processor's internal status at the breakpoint.

To retain any terminal-oriented command structures you've developed, the same terminal can be used for direct communication with either the 8540 or the host system. There's even a local printer interface on the 8540 so its printing operations won't burden the host.

A Trigger Trace Analyzer for real-time prototype monitoring.

In many applications, the timing of code execution becomes critical. To fully support real-time debugging, the 8540 includes an optional Trigger Trace Analyzer. It has four trigger channels ready to track down even the remotest sections of code execution.

You can do things like identify all non-ASCII writes to an I/O port. Or count the number of calls to a specific subroutine. Or measure the elapsed time of an interrupt handler routine.



Let the 8540 finish the job your computer started.

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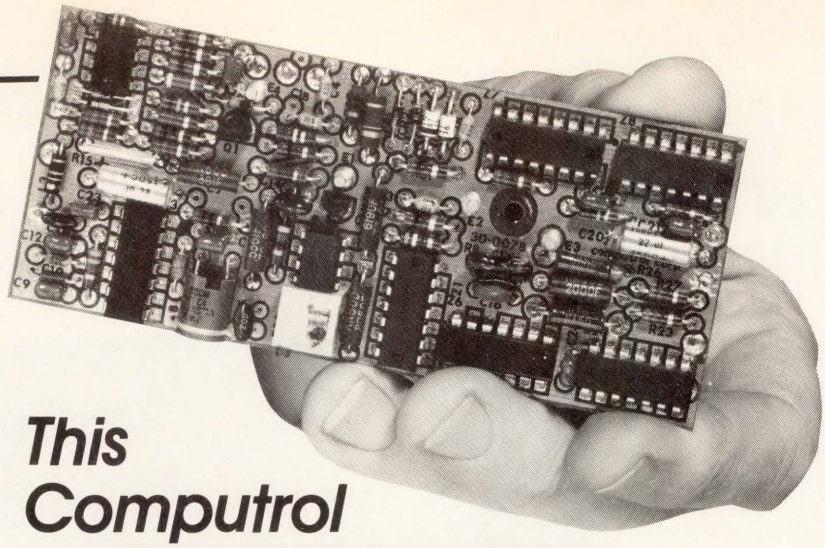
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CONFERENCES

DEC 3—California Computer Show, Hyatt Hotel, Palo Alto, Calif. INFORMATION: Carol L. Reimer, Norm De Nardi Enterprises, 95 Main St, Los Altos, CA 94022. Tel: 415/941-8440

DEC 7-9—Internat'l Electron Devices Meeting, Washington Hilton Hotel, Washington, DC. INFORMATION: Melissa Widerkehr, Courtesy Assocs, 1629 K St NW, Washington, DC 20006. Tel: 202/296-8100

DEC 8—Computer Networking Sym/NBS, Gaithersburg, Md. INFORMATION: Robert Toense, B226, Technology Bldg, Nat'l Bureau of Standards, Washington, DC 20234. Tel: 301/921-3516

DEC 15-19—Gulf Computer Exhibition, Dubai Internat'l Trade Ctr, Dubai, U.A.E. INFORMATION: Seymour House, 17 Waterloo Pl, London SEIY 4AR, England. Tel: 01/930-3881; or Trade Ctr Mgmt Co, PO Box 9292, Dubai, U.A.E., Tel: 472200

JAN 3-8—Annual Meeting of AAAS, Washington, DC. INFORMATION: American Assoc for the Advancement of Science (AAAS), 1515 Massachusetts Ave NW, Washington, DC 20005

JAN 11-13—Western Conf and Expo, Anaheim, Calif. INFORMATION: Col Richard G. Deem, Armed Forces Communications and Electronics Assoc (AFCEA), Skyline One, Suite 300, 5205 Leesburg Pike, Falls Church, VA 22041

JAN 11-15—Communications Networks Conf and Expo, Georgia World Congress Ctr, Atlanta, Ga. INFORMATION: Bill Leitch, CW Conf Mgmt Group, 375 Cochituate Rd, PO Box 880, Framingham, MA 01701. Tel: 617/879-0700; 800/225-4698 (outside Mass)

JAN 14 AND FEB 10—Invitational Computer Confs, South Coast Plaza Hotel, Orange County, Calif; and Pier 66 Hotel, Ft Lauderdale, Fla. INFORMATION: B. J. Johnson & Assocs, Inc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

JAN 18-21—ATE Seminar/Exhibit, Pasadena Ctr, Pasadena, Calif. INFORMATION: Elaine Bull, Promotion Coordinator, ATE Seminar/Exhibit, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

JAN 19-21—SOUTHCON, Orange County Conv Ctr, Orlando, Fla. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

JAN 20-22—Texas Computer Show, Dallas Conv Ctr, Dallas, Tex. INFORMATION: Catherine Manor, Texas Computer Show, PO Box 214035, Dallas, TX 75221. Tel: 214/761-9108

FEB 10-12—Internat'l Solid State Circuits Conf, Hilton Hotel, San Francisco, Calif. INFORMATION: L. Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

FEB 22-25—COMPCON Spring, Jack Tar Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

SEMINARS

Datapro Seminars, various U.S. cities and dates. INFORMATION: Joseph F. Menendez, Mgr, Seminar and Conf Operation, Datapro Research Corp, 1805 Underwood Blvd, Delran, NJ 08075. Tel: 609/764-0100

Digital Seminars, various U.S. cities and dates. INFORMATION: Educational Services, Digital Equipment Corp, U.S. Marketing Group BU/E55, 12 Crosby Dr, Bedford, MA 01730. Tel: 617/276-4111

Data Communications for Minicomputer Users, various U.S. cities and dates. INFORMATION: Seminar Administrator, Micom Systems, Inc, 20151 Nordhoff St, Chatsworth, CA 91311. Tel: 213/998-8844

DEC 2-4—Speech Coding, Jack Tar Hotel, San Francisco, Calif. INFORMATION: McGraw-Hill Conf Ctr, 1221 Ave of the Americas, Rm 3677, New York, NY 10020. Tel: 212/997-4930

DEC 3-4 AND JAN 21-22—Local Network Equipment Seminar, Holiday Inn, San Francisco, Calif; and The Adams Hilton, Phoenix, Ariz. INFORMATION: Architecture Technology Corp, PO Box 24344, Minneapolis, MN 55424. Tel: 612/935-2035

MAR 9-11—Internat'l Zurich Seminar on Digital Communications, Swiss Federal Institute of Technology, Zurich, Switzerland. INFORMATION: Secretariat 82 IZS, Miss M. Frey, EAE, Siemens-Albis AG, CH-8047 Zurich Switzerland. Tel: +41-1-247 51 20

SHORT COURSES

NOV-JUNE—Courses for Developers and Users of Computer Systems, various U.S. cities and dates. INFORMATION: American Management Assocs, Information Systems & Technology Div, 135 W 50th St, New York, NY 10020. Tel: 212/586-8100

1981/1982—IEEE Continuing Education Courses, various U.S. cities and dates. INFORMATION: Continuing Education Dept, IEEE Service Ctr, 445 Hoes Ln, Piscataway, NJ 08854. Tel: 201/981-0060

DEC 1-3, JAN 4-8, JAN 18-20, AND JAN 25-29—Human Factor Issues in Computer Graphics; Data Communications Systems and Networks; Configuration Mgt of Software Programs; Microprocessors and Microcomputers: Theory and Applications, George Washington U, Washington, DC. INFORMATION: Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: 202/676-6106; 800/424-9773 (outside DC)

DEC 7-9—Advanced Programming Microprocessor Workshop, Lafayette, Ind. INFORMATION: Carol Butler, WINTEK Corp, 1801 South St, Lafayette, IN 47904. Tel: 317/742-8428

DEC 7-11—Tutorial Week West, Hotel del Coronado, San Diego, Calif. INFORMATION: Christina E. Taylor, IEEE Computer Society, 10662 Los Vaqueros Circle, Los Alamitos, CA 90720. Tel: 714/821-8380

DEC 8-11—Ada, Sheraton-Lexington, Lexington, Mass. INFORMATION: LeAnne Grillo, Intermetrics, Inc, 733 Concord Ave, Cambridge, MA 02138. Tel: 617/661-1840

JAN 11-15—Applied Interactive Computer Graphics, U of Tennessee Space Institute, Tullahoma, Tenn. INFORMATION: Jules Bernard, U of Tennessee Space Institute, Tullahoma, TN 37388. Tel: 615/455-0631

JAN 19-22—Peripheral Array Processors for Signal Processing & Simulation, Sheraton National Hotel, Washington, DC. INFORMATION: Continuing Education Institute, 10889 Wilshire Blvd, Suite 1030, Los Angeles, CA 90024. Tel: 213/824-9545

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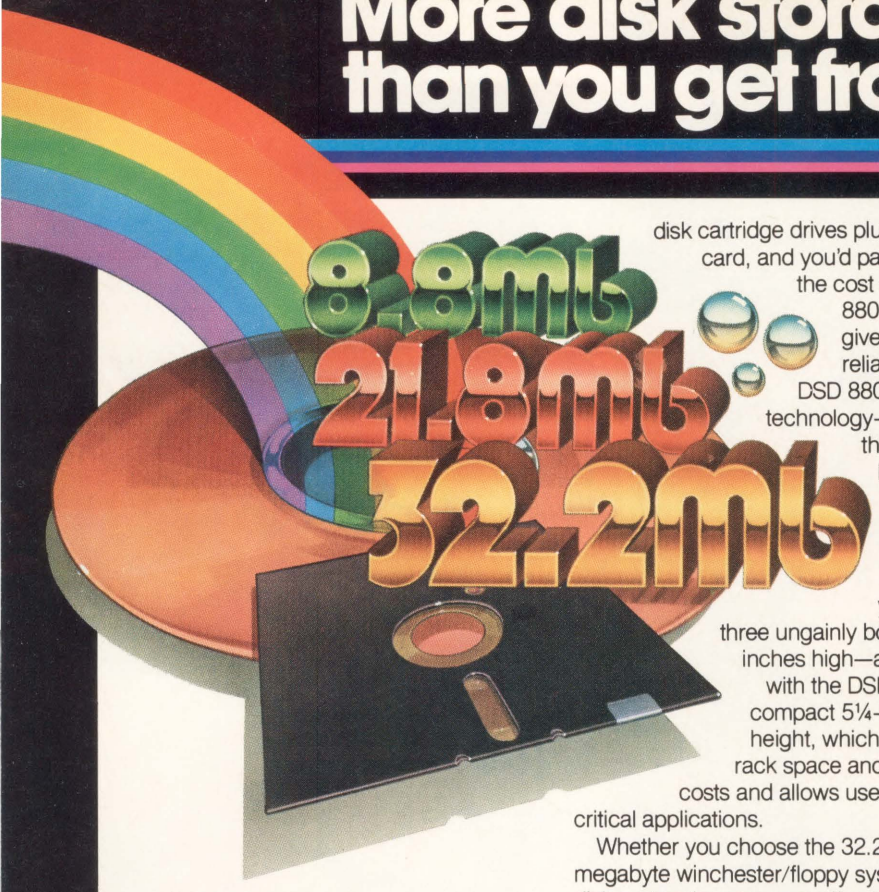


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DSD 880 gives you more megabytes per buck for your PDP-11 and LSI-11.

With the addition of a new DSD 880 version, you now have three choices in winchester disk storage: 31.2, 20.8 or 7.8 megabytes. Each with a choice of 0.5 single- or 1-megabyte double-sided floppy backup. More capacity for less cost-per-megabyte than any comparable DEC alternative.

To match the capacity of the DSD 880's 31.2-megabyte winchester disk, for example, you'd need three DEC RL02 disk cartridge drives plus bootstrap card, and you'd pay about twice the cost of one DSD 880. Plus, you'd give up the high reliability of the DSD 880's winchester technology—a state-of-the-art choice DEC doesn't even offer LSI-11 and PDP-11 users. And you'd have three ungainly boxes over 30 inches high—as compared with the DSD 880's compact 5¼-inch panel height, which saves you rack space and cabinetry costs and allows use in space-critical applications.

Whether you choose the 32.2, 21.8 or 8.8 megabyte winchester/floppy system, your disk system is more cost-effective than any comparable DEC disk drive or combination.

The hardware bootstrap is built right into the interface so you don't have to pay extra for a separate board.

The DSD 880 interfaces require 70% less backplane space than equivalent DEC configurations.

And the HyperDiagnostic™ panel simplifies troubleshooting for cost-effective remote diagnosis.

Fully compatible three ways.

The DSD 880 is hardware-compatible. It integrates with any DEC LSI-11 or PDP-11 computer-based system. Combine the DSD 880 with a VT103 containing an LSI-11/23 and you've got a complete, powerful table-top microcomputer with up to 32.2 megabytes of storage.

Software compatibility is no problem either. You can use your RT-11 or RSX-11 operating systems with RL01 or RL02 (winchester) and RX02 (floppy) handlers. With no modifications at all. And the DSD 880 runs all applicable DEC diagnostics and utilities.

It's media-compatible, too. DSD floppies can use either DEC double-density or IBM single-density formats.

With its higher capacities, smaller size, lower cost and more, the DSD 880 gives your DEC computer-based system the disk storage it deserves.

A choice of 4 floppy systems.

Pick the features you need. Data Systems Design gives you more choices in DEC-compatible floppy disk systems, too.



Each of the four floppy systems is packaged in a low-profile 5¼-inch chassis. All offer built-in hardware bootstrap and complete DEC RX02 compatibility, plus a choice of domestic or international configurations, and complete documentation for easy system integration.

DSD 480 provides double-sided floppy storage for your LSI-11 or PDP-11.

For twice the capacity of DEC's RX02, choose the DSD 480. An optional EXCHNG™ software program lets the DSD 480 transfer files between IBM- and DEC-generated diskettes.

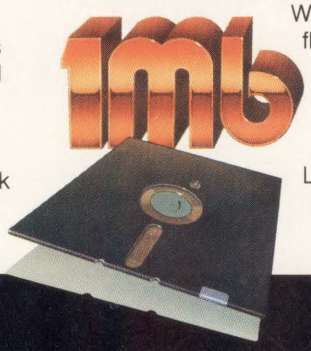
DSD 470 gives you low-cost double-sided floppy storage for your LSI-11.

The DSD 470 is software compatible and can be configured for single- or double-sided diskettes. And its single-board controller/interface* has far fewer parts than separate boards for better space utilization and improved reliability.

Choose DSD 440 for single-sided floppy storage with your LSI-11 or PDP-11.

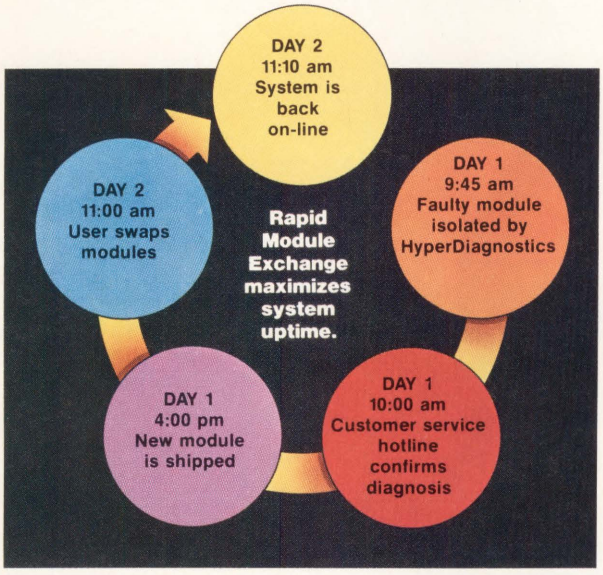
The DSD 440 is RX01 and RX02 software-compatible. It can transfer data 20% faster than DEC's RX02, and features built-in self-diagnostics for easy servicing.

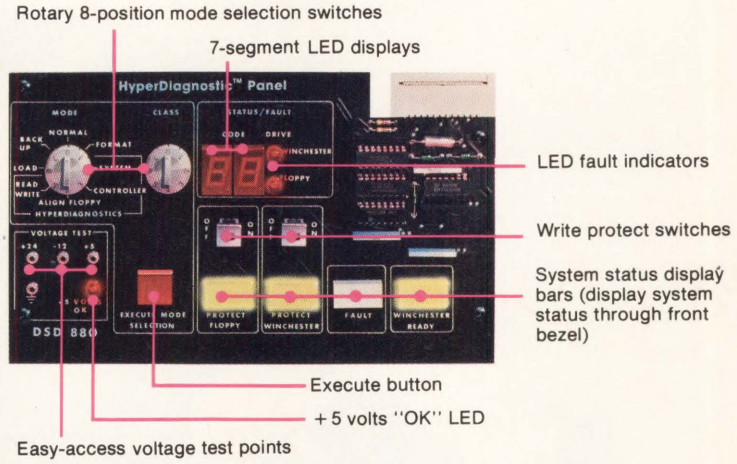
Choose DSD 430 for lowest entry cost with your LSI-11.



With 2 single-sided floppy drives, the DSD 430 gives you full RX02 compatibility and complete LSI-11/23 four-level interrupt support.

More reliable performance and easier maintenance.





DSD 880 HyperDiagnostic™ Panel

A revolutionary concept in uptime: Remote diagnosis ends costly service calls.

The true measure of a system is its ability to perform. Day after day, reading and writing data on demand. Data Systems Design units outlast any other disk system on the market. But even the most rugged system has an occasional problem. And that's when Data Systems Design really shines.

You know the usual service scenario. There's a problem, so you call the service rep. And wait for a return call. Then you wait for someone to show up. And every minute is costing money, in addition to the high cost of the service contract itself.

Data Systems Design ends all that with the service system that will soon be the industry standard: remote diagnosis.

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*This controller/interface is also available separately as the DSD 4140.

†Although these services are available within the U.S.A. only, comparable service is available through our international distributors.

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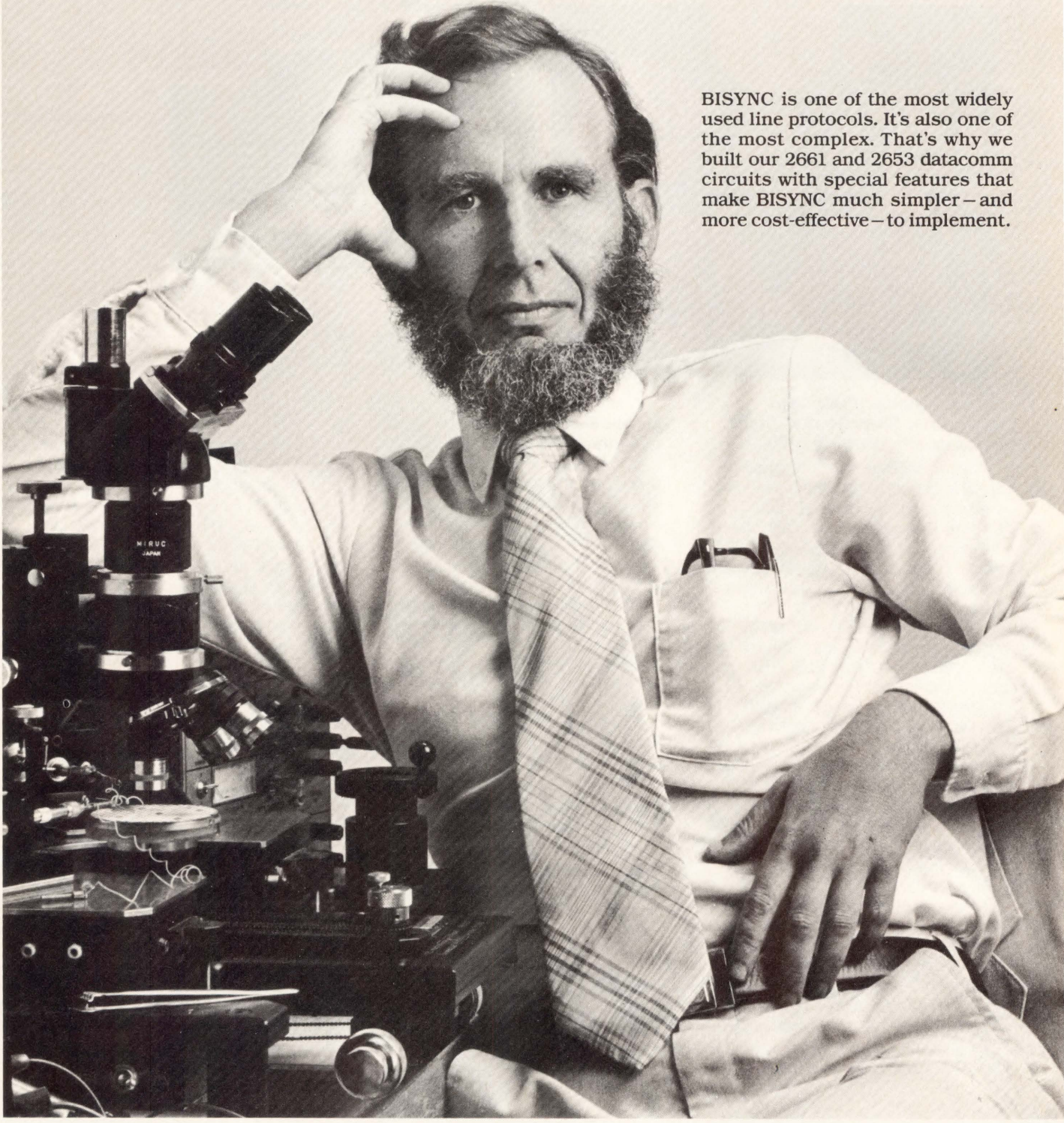
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Data Systems

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That's when they really begin to appreci

John Yarborough, Manager, Circuit Design Engineering



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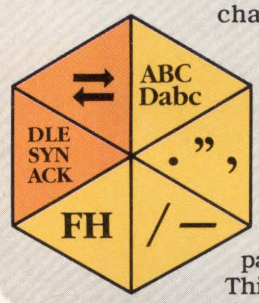
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BISYNC is a character-oriented protocol. Which means it requires two separate character sets to send messages: a control set to manage the data link and delimit the message fields, and an alphanumeric set for text messages.

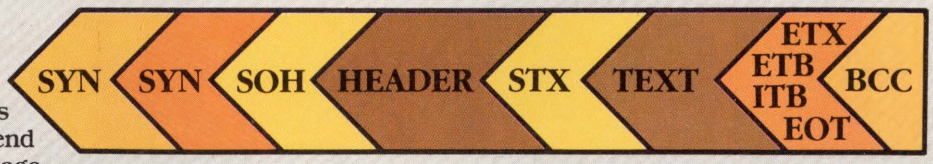
Control characters are used at the beginning (SYN and header fields) and end of the message. But in many non-text data transfers, control-like characters are included in the text (information) field. To avoid the misinterpretation this can cause, BISYNC has a special transparent mode.



This is activated by inserting a data link escape character (DLE) in front of the control character that begins the text field (STX). It signals the receiver to ignore all control characters until another DLE/xxx sequence is received. BISYNC's transparent mode is one of the reasons for its complexity.

Another key BISYNC feature is the Block Check Character field which is used to check for errors. The transmitter generates and sends a BCC at the end of each transmission. During receipt of the message, the receiver accumulates its own BCC and compares the two. If they match, the message is correct. If not, it's re-sent.

You'll find a comprehensive discussion of the BCC and transparent mode as well as other important BISYNC features in Signetics' Datacomm Kit #2.



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Our 2653 implements parity and cyclic redundancy checks as required by BISYNC. It recognizes BISYNC control and graphic characters, and automatically includes or excludes them from the BCC as required. Like the 2661, it supports transparent and non-transparent modes. And it easily interfaces with any bus-oriented micro-computer system.

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For complete information on these circuits and an in-depth report on BISYNC, send in the coupon for the Signetics Datacomm Information Kit #2. Or call (408) 746-2136 for immediate assistance. Sooner or later, you'll be glad you did.

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CD11/81

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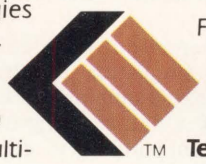
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LETTERS TO THE EDITOR

To the Editor:

Mr Terence M. Davis's article describing the technical aspects of storage and raster displays, "Powerful graphics tool combines refresh and storage capabilities," (July 1981, pp 105-108), gave excellent insight into the dynamic graphics (refresh) option on the 4054.

In the section "Storage and refresh—best of both worlds," Mr Davis states, "The best choice combines two of these elements to create a bright but non-storing graphic display." All storage tubes users will readily acknowledge that DVST displays are not as bright as raster or vector refresh displays. Moreover, for all of "these reasons," faster writing speed and lower beam current, the refresh images on DVSTs are dimmer still.

Mr Davis completely neglected vector refresh, the most versatile, high resolution display technology. Vector refresh terminals can generate high resolution (4096 x 4096 viewable) displays while maintaining the brightness of raster technology and are also extremely adept at dynamic displays. Such features as depth queuing, selective erase, true zoom and pan, and dynamic focus and variable intensity on a single vector suit the vector refresh displays best for many applications.

Jack Dmoch, Marketing Support Mgr
Vector Automation, Inc
Village of Cross Keys
Baltimore, MD 21210

To the Editor:

The vertical, or longitudinal, parity bit approach described in Lee Edwards's article, "Low cost alternative to Hamming codes corrects memory errors," (July 1981, pp 143-148), is indeed a very good one.

Unfortunately, there is a minor hitch to this idea. The problem is this: U.S. Patent 3,887,901 "Longitudinal Parity Generator for Mainframe Memories," issued to Harry W. Moore III for Sperry Rand Corp on June 3, 1975. Mr Edwards's device, in essence, is identical to the device described in that patent. To use the device described in the July 1981 article would, I believe, require a licensing agreement with Sperry Rand Corp, New York, NY.

Harry W. Moore III, Program Mgr
Borg-Warner Electronics
Borg-Warner Corp
702 S Aurora St
Ithaca, NY 14850

The Author Replies:

The patent Mr Moore refers to describes longitudinal parity and a single register to represent a check character for an entire memory, and describes only error detection. Longitudinal parity is not a novel idea; it has been used since the 50s for magnetic tape error detection.

The circuitry and method of the July CD article provide a method for as many longitudinal parity blocks as desired; in addition to the error detection capability, it provides the ability to correct soft failures in the memory.

In December 1980, NCR Corp applied for a patent on the method and apparatus described in the article. At that time Mr Moore's patent was reviewed and not found to be in conflict with NCR's application.

Lee Edwards
NCR Corp
1200 Greenville Rd
Easley, SC 29640

To the Editor:

I take great exception to many of the statements in Douglas Raymond's article, "In-circuit testing comes of age," (Aug 1981, pp 117-124. Card-edge functional testing is still a very viable and cost-effective way to test digital PC boards. A class of functional tester uses the comparison technique to verify a good board and isolate the defective node on a bad board. This method of functional testing is not bound by many of the limitations presented in the article.

These comparison testers do not need a software simulation to achieve the 98% yield. Programming can be as easy as assigning a data type (gray code or pseudorandom patterns) to stimulate the input pins. Comparison and signature analysis of the outputs make the diagnostics very powerful and comprehensive. Test rates can run well into the megahertz region, allowing an interactive and native test.

Ron Steiner, Technical Services Mgr
John Fluke Mfg Co, Inc.
PO Box 930
W 75 Century Rd
Paramus, NJ 07652

The Author Replies:

A comparison tester compares the state of the board under test to the state of a reference board. The tester provides the same stimulus signals to both boards, checking that the board under test acts just like the reference board.

Comparison testers such as those manufactured by Mr Steiner's company offer straightforward solutions to some of the traditional problems of functional testing. For example, software simulation is not strictly necessary because the tester has access to an actual copy of a board known to be good. Thoroughness of the exercise program is checked by manual fault injection rather than by software fault simulation.

Comparison testers equipped with flying window comparators can also detect out-of-tolerance analog signals. Software based card-edge testers can do this only with expensive added instruments and integration software.

Good-board logic comparison, flying analog comparison, and hardware fault emulation are elegant, effective approaches that allow quick formulation of go/no-go board tests.

The ultimate purpose of high volume production ATE, however, is to generate unambiguous rework instructions so that the repair operators will know how to fix the failed boards.

Functional testing diagnoses faults by a process of elimination. In-circuit testing takes the direct approach, inspecting individual components. This method provides unambiguous rework messages, since the tester focuses itself on one component at a time. No manual probing is required, and no "fault tree" need be prepared. In-circuit also provides a more thorough test, as every component is inspected, whether or not it could have caused a functional test to fail.

The article's purpose is to explain recent developments in the evolution of in-circuit testing. I didn't have space to discuss the relative merits of all the different card-edge approaches, and I regret any inconvenience my omission has caused.

Douglas W. Raymond, Project Mgr
Plantronics/Zehntel
2625 Shadelands Dr
Walnut Creek, CA 94598

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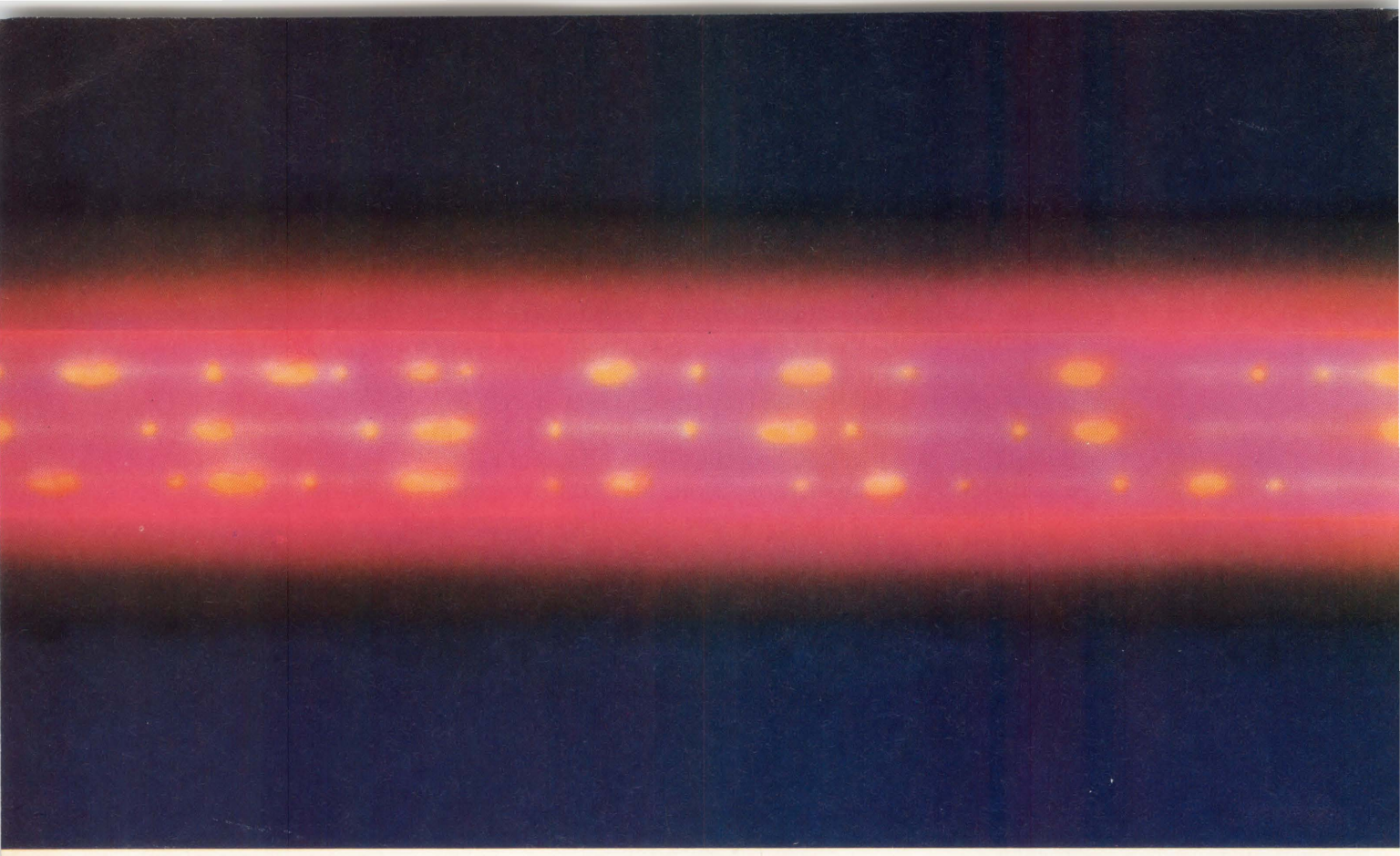
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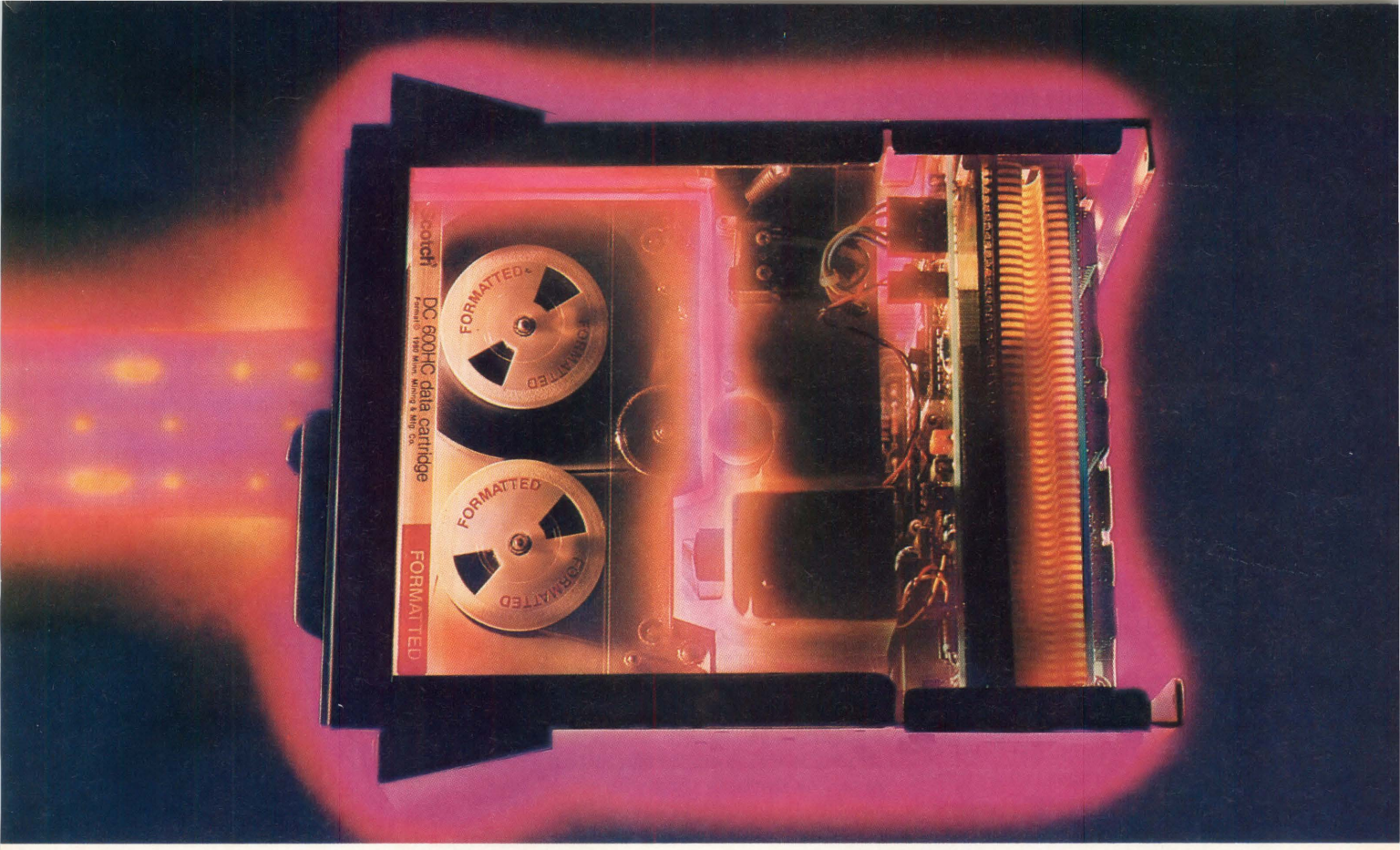
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CIRCLE 13 ON INQUIRY CARD

CONTROL & AUTOMATION

Low cost, lightweight robot performs industrial functions

A self-contained industrial robot provides high performance at a cost of under $10,000. Capable of continuous 90°/s sweep in either direction, the jointed arm provides eight digital inputs and outputs that link with machine or industrial control network. A network of microcomputers under direction of a 16-bit CPU provides closed loop control of all robot movements.

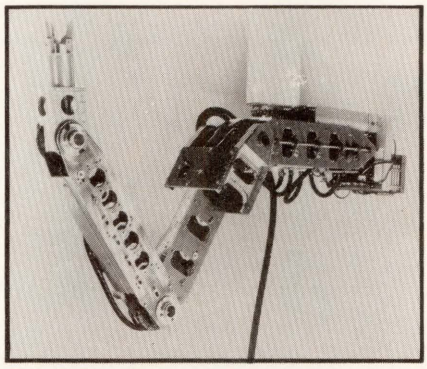
This, first of a family from International Robomation/Intelligence, combines advantages from several technologies to achieve speed and strength in a lightweight, 200 lb (91 kg) low cost design. Aerospace construction techniques achieve maximum strength and lifting power with minimal size and weight. An internal network of control microcomputers, directed by a Motorola 68000 CPU, provides a hierarchical industrial control system for closed loop control of all movements. Digital air servo motors supply motive power for precise point to point positioning of the unit's jointed arm.

Operational features. The arm comes with five standard axes for body, shoulder, and elbow sweep as well as wrist roll and pitch. Each axis has its own internal digital air servo motor, and a dedicated microprocessor to control motion. A 5-stage chain-driven reduction drive set within each axis housing generates leverage. One of the five axes acts as a horizontal drive, the other four are linked end to end to supply shoulder, elbow, and wrist pitch and wrist roll.

The horizontal axis is capable of continuous sweep in either clockwise or counterclockwise direction at a speed of 90°/s. The shoulder module can sweep a maximum of 180° vertically at 60°/s. Elbow sweep is a maximum of 210° at 60°/s. Wrist roll is continuous in either clockwise or counterclockwise direction at 120°/s. Wrist pitch may be 210° max, at the same speed.

The robot is intended for applications where the maximum weight to be lifted is 50 lb (23 kg). With a 50-lb load at the end of the 60″ (152-cm) arm, stress on the gear chain at the shoulder is approximately 1000 lb (454 kg). The chain system is designed to withstand tensile stress up to 10,000 lb (4536 kg).

The simplicity of the air servo motors—and their fast response time under digital control—permits the use of a dithering or pulsed air technique that provides precise, almost friction-free movement of the robot axis modules. To overcome the effects of friction and gravity in arm movement, the air is pulsed to the motor rather than applied at constant pressure. Although it is generated in pulses, by the time the motion works its way through the reduction gears, it appears to be continuous.



Industrial robot. International Robomation's robot (without skins) combines high strength aluminum alloy structures with 5-stage chain-driven reduction drives to supply high strength in lightweight package for heavy duty industrial applications. Network of microcomputers under direction of 16-bit CPU provides closed loop control of all movements

Each axis is equipped with a notched wheel that has optical sensors on it to produce a quadrature square wave, much like a digital encoder. This provides feedback for an A and B track so that motion resolution at the end of the arm is approximately 0.001″ (0.025 mm); however, the system has a repeatability specification of 0.000025″ (6 μm). By using the dithering technique with this precise closed loop feedback, motion is more precise and can be varied under computer control. For even finer control, the differential dithering technique of alternating forward and reverse pulses can be used.

Computer control. The entire robot is controlled by a hierarchy of microcomputers, with a Motorola 68000 16-bit processor as the overall manager. Each axis has its own control computer and a seventh CPU is employed as a safety control. The 68000 has a realtime operating system and a realtime executive for handling both foreground and background tasks. Users may program the robot in hand commands, Macro Assembly, FORTRAN, or Pascal languages. Eight digital inputs and outputs allow users to interface it with their own machine sensors. Additional analog and digital I/O is optional.

Each of the five axis control computers shares 256 bytes of memory with the 68000; thus each can monitor the whole system. All data transfers for closed loop control are made rapidly via direct memory address rather than as I/O transfers.

A portable handheld programmer is used to program the robot. The robot's coordinate system is based on axis angles; users may also work in standard Cartesian coordinates for X, Y, Z, and space planes. X, Y, and Z axes take the user to the end of the wrist plate. The wrist provides pitch and roll, and a hand or other tool attached to the end of the arm provides yaw. The robot thus can be programmed manually in a jog mode in either Cartesian or axis angle formats, simply by stepping it through its motions.

Once the robot goes online, the 68000 maintains points selected by the user. It also maintains the contouring mode which includes velocity control from point to point. In contouring mode, the 68000 allows each axis to approach each point on the fly rather than reaching a point and stopping. This creates a contour rather than a jerky motion.

The 68000 maintains a number of error status messages relative to each axis to monitor pressure and location. A separate safety program works with the safety computer to make sure all elements are functioning properly. The 68000 also handles optimizing routines so that the robot runs energy efficiently. Finally, the CPU provides central control over all pulsed outputs. These are located in specific memory locations and are output to a bank of electronic clocks at the axis control computers, which, in turn, control the pulses going to each motor. This high level architecture ensures that all pulses occur concurrently to synchronize all robot activities. **International Robomation/Intelligence**, 6353 El Camino Real, Carlsbad, CA 92008.

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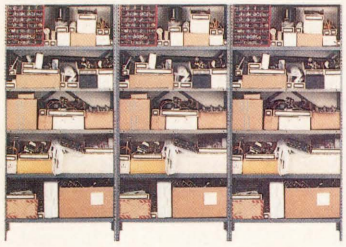


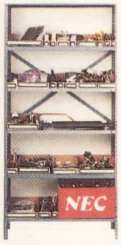
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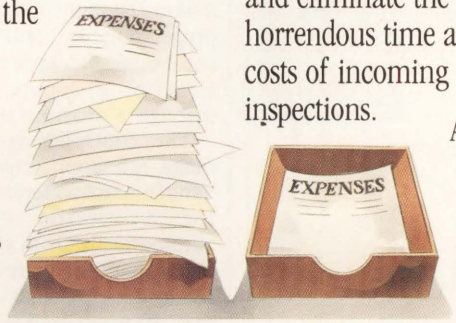




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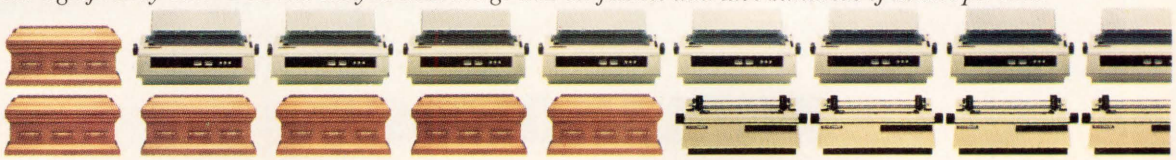
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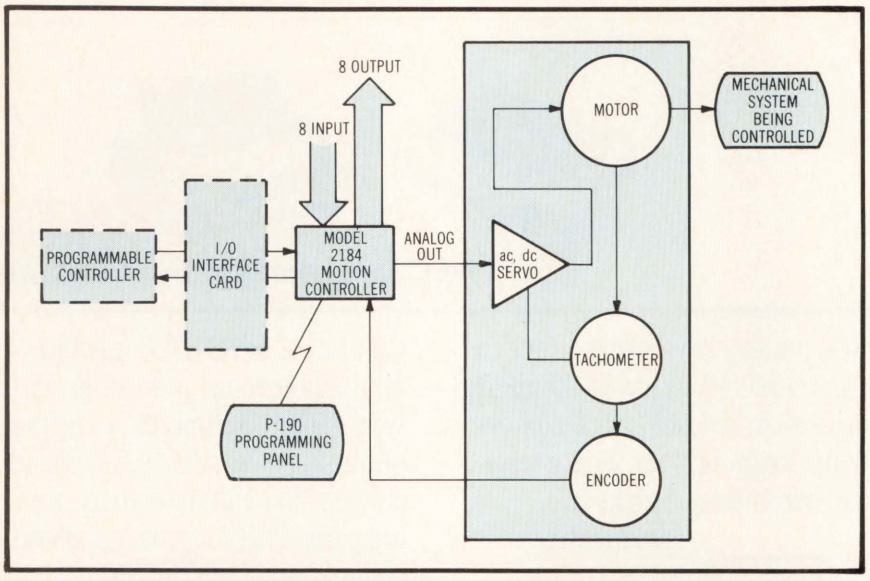
Other printers' DOA rate: more than 5%.



CIRCLE 14 ON INQUIRY CARD

CONTROL & AUTOMATION

Servo controller adds speed, accuracy to programmable controller



Motion control system. Operating with servo drive and incremental encoder to complete position loop, model 2184 serves as brains of system, controlling speed, direction, acceleration, and position according to preprogrammed instructions stored in memory

Ruggedness, programmability, and maintainability of a programmable controller are combined with the speed, precision, and accuracy essential for efficient motion control in a state of the art servo controller. Model 2184, developed by Gould Inc's Modicon Div, combines a high speed central processor, battery backed memory, power supply, and a servo interface in a compact package that supplies the speed necessary to effectively handle motion control.

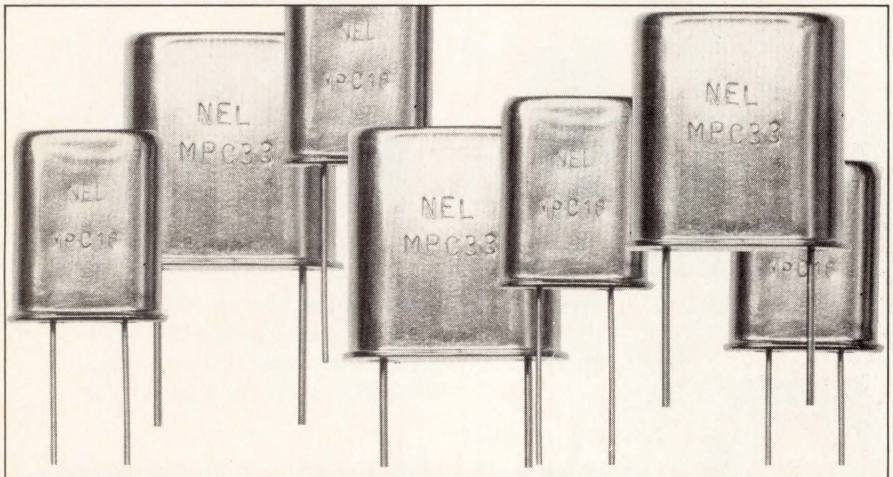
The controller handles eight discrete input and eight discrete outputs which can be gauges and switches or other parts of the control system. As information is fed back to the controller from these points, it responds immediately, adjusting its position commands as necessary.

Operating in either English or metric units, it provides precision point to point motion control for a single axis device and can control the position of either the machine element or the work itself. The unit is programmed through a standard P190 CRT programmer using an English language prompting approach. Large memory and a powerful command repertoire enable it to handle virtually all motor control operations from programs stored in memory.

The controller always concentrates on the machine motion being controlled; it can instantaneously adjust position commands according to the errors it senses. As shown in the drawing, the servomotor shaft typically is coupled to a tachometer and then an incremental encoder, which feeds signals to the internal processor. The processor decodes these signals and uses this information to update and modify motor velocity commands.

Continuous control, moving rapidly from one step to the next in complex profile programs and reacting appropriately to a variety of input data, makes the controller much faster than a programmable controller which uses a sequential scan-type mode, checking the status of all inputs and then scanning through a program one step at a time.

The controller is useful in a wide range of applications and can even handle many different action procedures for a specific machine, moving automatically from one job to the next. Programming or revising motion profiles is done through a P190 CRT programmer. Prompts lead the operator through entry of the functions to be performed, motor speed, and direction. Programs can be stored either in battery-backed memory or on cassette tapes, allowing the user to create as many profiles as needed for a machine without running out of storage. Program revision can be done while the production system is running. *(continued on page 37)*



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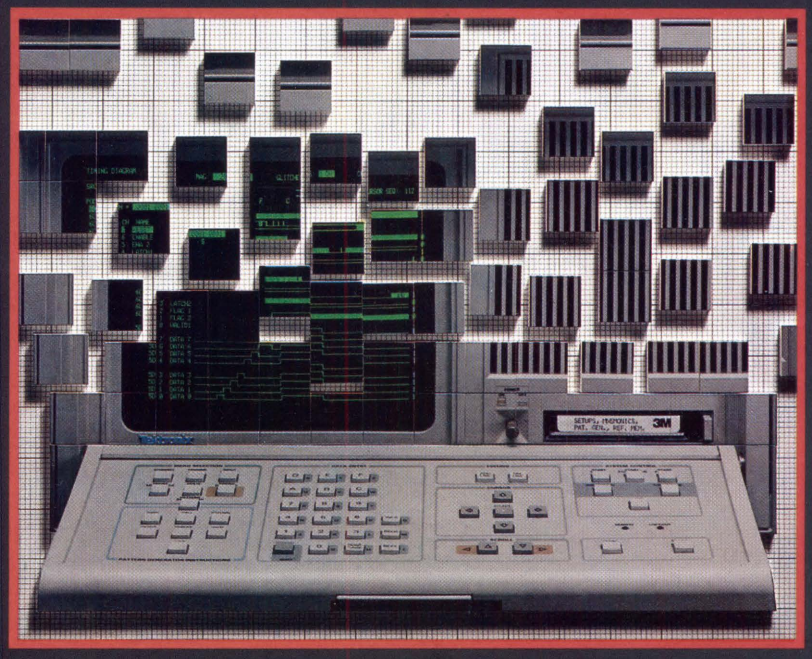
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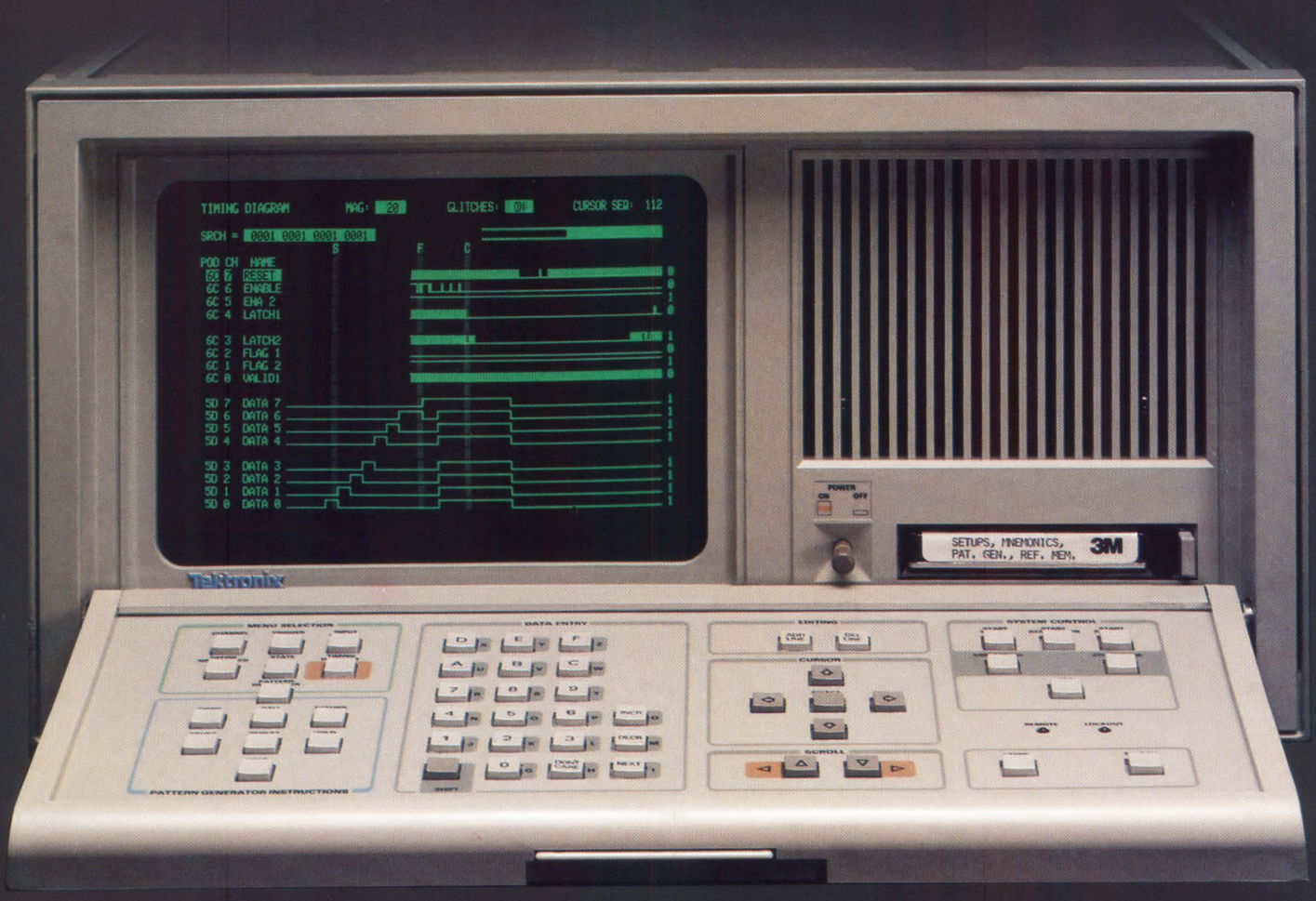
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TEK DAS 9100 DIGITAL ANALYSIS SYSTEM

Digital Analysis System.

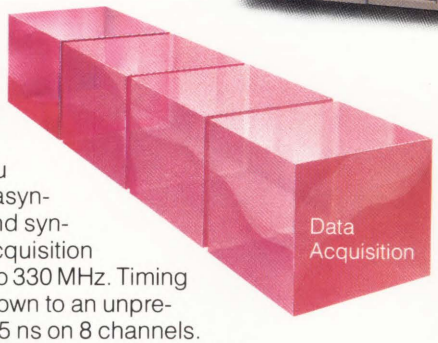
A new concept in logic analysis.

It's the one you've been waiting for. A unified, yet configurable and upgradable logic analysis system. With unparalleled flexibility and performance.

All from a single instrument.

Modularity is the key. Selectable, plug-in card modules and a powerful mainframe let you tailor the exact logic analyzer you need. With asynchronous and synchronous acquisition speeds up to 330 MHz. Timing resolution down to an unprecedented 1.5 ns on 8 channels. And data widths from 16 channels at 330 MHz, to 104 channels at 25 MHz.









But that's not all, because now you can also *link pattern generation with data acquisition.* A powerful combination never before available in a single instrument. One that makes debugging digital systems far simpler than previously possible. Pattern generation provides stimulus data widths up to 80 channels at 25 MHz.

Need I/O capability? There's an option that adds RS-232, GPIB and hard copy interface. And another for a built-in DC-100 magnetic tape drive system.

Select your own width and speed combination, for data acquisition.

DAS 9100 gives you four different data acquisition modules to use as building blocks. Each has its own data width and maximum speed: 32 channels at 25 MHz; 8 channels at 100 MHz with glitch memory; and two modules with 4 channels at 330 MHz. Modules can be combined to give you the performance you need.

Need to go faster? The four channel modules also operate in a two channel mode, with timing resolution to 1.5 ns. All modules can operate either synchronously or asynchronously at full system speed. And the 32 channel module can be used to arm the trigger on those with higher acquisition rates. Plus *modules can be added or changed, as your needs change.*

To back it all up, there's powerful triggering, programmable reference memory and multiple clocks. *Plus glitch triggering,* with a separate glitch memory for unambiguous glitch detection, and our unique, new "arms mode" allows timing correlation between synchronous and asynchronous data.

DAS 9100 integrates the power of pattern generation with data acquisition.

At last, you can have a tool that covers your digital system debugging needs. By combining pattern generation and data acquisition modules, you can stimulate your prototype while simultaneously analyzing its operation. Allowing you to enter a whole new dimension of design analysis and verification.

Pattern generation capability is built around a 16 channel, 25 MHz module. Through additional expansion modules, you can raise the total to 80 channels while maintaining full system speed. The pattern generator allows interaction with the prototype through data strobe outputs and external control inputs, including an interrupt line.

The DAS 9100 lets you start debugging hardware even before your software is available. Pattern generation makes it all possible.

With plenty of room for mainframe options to fit your application.

A powerful I/O option adds RS-232, GPIB and hard copy interface for *full remote programmability.* A built-in magnetic tape drive using DC-100 cartridges is also available, so you can save whole or partial instrument setups for recall.

DAS 9100's easy-to-use keyboard and menus tie it all together.

Operation of your DAS 9100 is simple and straightforward. Selectable menus help you set up trigger conditions, select data formats and define voltage thresholds. You can even define your own mnemonics to fit the data under test.

Please send me more information on the DAS 9100

Name _____

Title _____

Address _____

City _____ State _____ Zip _____

Phone _____

Send to the Tektronix address listed on the back.

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Circle 140 for literature.
Circle 141 for sales contact.

TEK DAS 9100 DIGITAL ANALYSIS SYSTEM

FLEXIBLE SOLUTIONS FOR A FUTURE OF CHANGE

SPECIFICATIONS

DAS 9100 Summary

Modules Available

Data Acquisition Modules:
91A32, 91A08, 91A04, 91AE04 Expander
Pattern Generation Modules:
91P16, 91P32 Expander

DAS 9109 Mainframe

Includes 9" CRT, keyboard, controller, one modular power supply, trigger-timebase, space for six add-on card modules

Options Available:

Opt. 1 Tape Drive, for DC100 tape cartridges
Opt. 2 RS232, GPIB and hard copy interface,
Opt. 3 Additional Power Supply
Opt. 4 Two additional Power Supplies
Opt. 5 Rackmount Hardware

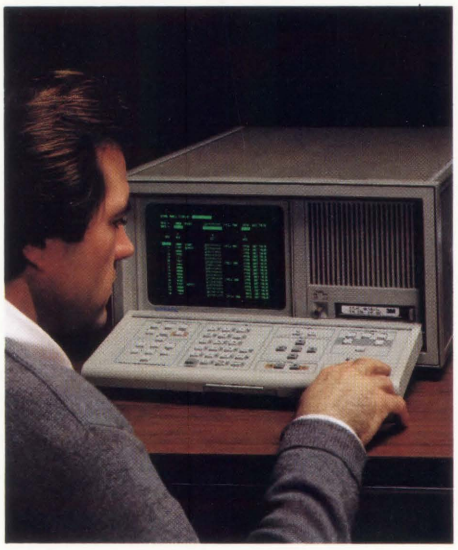
DATA Acquisition Summary

State Table Display

- HEX, Binary, Octal
- User Definable mnemonics
- Search mode
- Multi-speed time aligned data
- Reference memory with editing
- Reference memory compare with data masking and programmable compare window

Timing Diagram Display

- 16 channels simultaneous display
- Programmable selection of channels displayed
- 16 user defineable trace labels
- Horizontal magnification, 1x to 10,000x
- Cursor position & decode
- Multi-speed time aligned data
- Glitch display
- Search mode
- Memory display window





Acquisition Modules

Characteristic	*91A32	91A08	91A04 & 91AE04 Full Channel Mode	91A04 & 91AE04 High Resolution Mode
Number of Channels per Module	32	8	4	2
Resolution/ Clock Freq.	40 ns/25 MHz	10 ns/100 MHz	3 ns/330 MHz	1.5 ns/330 MHz
Modules Per System	3	4	1	3
Channels Per System	96	32	16	8
Memory Depth	512	512	2048	4096
Triggering	**nA→B ≠C	1 level plus arms mode	1 level plus arms mode	
Multiple Clocks	3	With 91A32	With 91A32	
Synchronous	Yes	Yes	Yes	No
Asynchronous	Yes	Yes	Yes	
Glitch Triggering	No	Yes	1.5 nanosecond resolution sampling	
Qualifiers Per Board	2	1	0	
Set-up Times Hold Times	29 ns/0 ns	9 ns/0 ns	2 ns/0 ns	
Number of Probes	4	1	1	

*Data and clock thresholds selected independently
**Any number of occurrences of word A, followed by various logical combinations of word B, reset if word C occurs.
Note: The 91A04 is a master card, channel expansion requires one or more 91AE04s.



DAS 9100 Pattern Generator Major Capabilities

Instruction Steps	254
Instruction Set	Count, Repeat Hold, Go To, Call, Return, Halt
Word Width	16, 48, 80 channels
Max Clock Speed	25 MHz
Programmable Radix	Yes Bin, Oct, Hex
Single Step Mode	Yes
Labels	Yes 32
Subroutine Nesting	Yes 16 Deep
Looping	Yes
Independently Programmable Strobes	Yes 2, 6, or 10
Bus Simulation Capability	Yes
User Definable Output Swings	Yes
Output Types	Patterns, Strobes (1 per probe) Clock
Tri-State Outputs	Yes
Hold Output	Yes
External Interupt	Yes
Internal or External Clock	Yes
Store Program on Mag. Tape	Yes
External Control	Yes



Options Summary

Option 1 DC-100 Tape Drive

- Stores 6 full instrument set-ups or 30 different reference memory patterns
- Directory Space for 32 files

Option 2 RS232, GPIB and Hard Copy Interface

RS232

- Selectable Baud Rates: 300, 600, 1200, 2400, 4800, 9600
- Master/Slave Operation, Full Duplex, Asynchronous

GPIB

- Talker/Listener Only
- Selectable Address
- Selectable Controller Type, EOI or (LF or EOI)

Composite Video Output

- Hardcopy Interface
- Video Monitor Interface

Other Characteristics

- Overall Dimensions — Length-23.5 in./ 59.7 cm, Width-17 in/43.2 cm, Height-9.5 in./24.1 cm.
- Weight — without accessories, 48 pounds/ 105.8 KG
- Voltage Input —
  LO LINE-90 V to 132 V rms
  HI LINE-180 V to 264 V rms
- Line Frequency — 48 to 63 Hz
- Power — 1000 VA, Maximum
- Temperature Range
  Operating 0°C to +50°C (+32° to +122°F)
  Storage −40°C to +65°C (−40° to +149°F)
- Altitude
  Operating — 10,000 ft, maximum
  Storage — 50,000 ft, maximum

DAS 9100 System Configurations

	DAS 9101	DAS 9102	DAS 9103	DAS 9104
Modules Included:				
91A32		1	1	2
91A08	2		1	2
91P16		1	1	1
Options Included			3	1, 4
Total Acquisition Channels:	16	32	40	80
At 100 MHz:	16		8	16
Total Pattern Generation Channels		16	16	16
Available Slots for future expansion	4	4	3	1

U.S.A., Asia, Australia, Central & South America, Japan
Tektronix, Inc., P.O. Box 4828, Portland, OR 97208, Phone: 800 547-6711, Oregon only 800 452-6773, Telex: 910-467-8708, Cable: TEKTRONIX

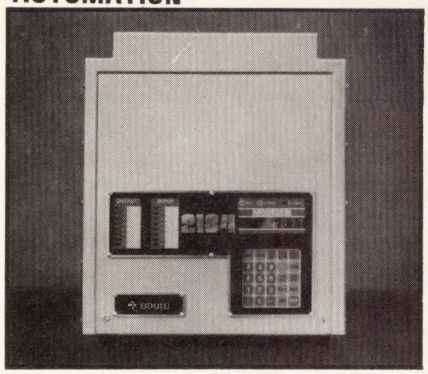
Europe, Africa, Middle East Tektronix International, Inc., European Marketing Centre, Postbox 827, 1180 AV Amstelveen, The Netherlands, Telex: 18312

Canada, Tektronix Canada Inc., P.O. Box 6500, Barrie, Ontario L4M 4V3, Phone: 705 737-2700

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57AX-4832 8/81



Servo controller. In model 2184, Gould's Modicon division has provided programmable controller with speed and precision necessary to effectively handle motion control

Maintenance of the machine is simplified by modular design. If a failure occurs in a circuit board, the board can be changed, keeping downtime to a minimum. Maximum uptime is ensured by online diagnostics that check all circuits and programs on a regular basis. Any error occurrence is indicated on the system's display panel. Battery backed memory prevents loss of programs if a brownout or power failure occurs. **Gould Inc, Modicon Div,** 1280 E Big Beaver Rd, Suite B, Troy, MI 48084
Circle 241 on Inquiry Card

Available right now – and for under $6000! PrintaColor IS8001, the world's first low-cost color ink jet printer. All the advantages of hard-copy color graphics. And at a price you can afford!

One thin dime – and two minutes time! Fast, quiet and cost efficient. Just 10¢ per copy! Typewriter-size desktop unit uses ordinary fanfold paper. And continuous copy printing, unattended.

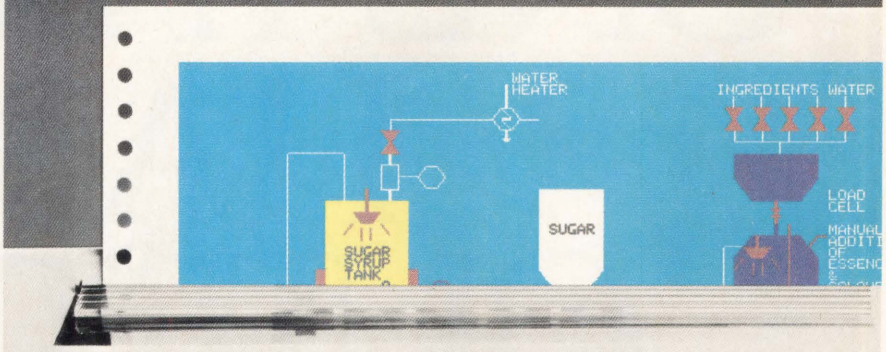
What you see is what you get! Now expand the advantages of color graphics to color hard copy. PrintaColor's innovative overlay system gives you the high quality of color ink jet printing without the high cost. From the display screen to the desk or conference table – graphics in color – quickly, quietly, efficiently, and now affordably!

Call or write for the name of your nearest representative.

Now – hard copy in color for one thin dime

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PrintaColor Corporation P.O. Box 52 Norcross, Georgia 30091 404/448-2675

CIRCLE 16 ON INQUIRY CARD

CAD system with 23″ monochromatic display eases PC board design

Based on a dual-processor architecture, System 60 allows the presentation of 13 PC board levels with varying *intensity on a 23″* (58-cm) monochromatic display. The pan area can be programmed to the exact dimensions of a board up to 218 in² (1406 cm²). Users design through interactive prompting. Aids such as numerically controlled drill tapes, component outlines, silkscreen, and soldermasks are standard.

Manufactured by Nicolet CAD Corp, the PC CAD system is a dual-processor design consisting of a proprietary 32-bit, high-speed CPU with a 128-bit instruction word and a 1k writable control store which is responsible for graphics data manipulation. A DEC LSI-11 16-bit minicomputer functions as a distributed peripheral processor. Also included are: 750k bytes of memory, expandable to 2M bytes; a portable system operator console with integral joystick; and dual 512k-byte capacity 8″ (20-cm) floppy disc drives. Ports are provided to interface external pen plotters, photoplotters, magnetic tape, perforated tape, and hardcopy peripherals. An RS-232-C communications interface and modem is included for computer diagnostics.

System functions and data entry are controlled via a full ASCII keyboard with more than 40 function select keys to interact with the microcode driven operator prompts. These prompts are displayed on the screen at the beginning and end of each design step. Video display cursors are positioned by use of either the tablet cursor, joystick control, or directional buttons on the console. By using these controls, zoom and pan functions are instantaneous. Keystrokes are minimized by grouping together functions such as DIPs, pads, and doglegs. Definition of line widths, pad sizes, and other design parameters can be entered by using the portable console either at the design station or at the digitizing tablet.

A 36 x 48″ (91- x 122-cm) digitizing tablet on a motorized base is available in either a backlit or nonbacklit design. The tablet has 0.001″ (0.025-mm) resolution and 0.005″ (0.127-mm) accuracy across its active area, and provides a means of converting designer layouts into digital data.

All software required for system operation, such as the company's operating system package and special purpose programs, are included. A macro assembler creates and links bit-slice microcode. An object library permits the user to develop a personal set of graphics objects to be used throughout a design. Additional programs are provided for optimizing photoplotter and NC output, as well as for formatting and copying diskettes. **Nicolet CAD Corp,** 2450 Whitman Rd, Concord, CA 94518.



Circle 242 on Inquiry Card

SINCE 1976, ONE FAMILY HAS QUIETLY CONTROLLED THE WORLD.

Think about it for a minute.

There are all kinds of microcontrollers on the market today. Handling literally billions of control functions all over the world. In everything from toys to terminals to satellites.

But when it comes to performance, flexibility, and quality, there's one family that's taken control right from the very beginning. And set all the standards.

Our 8048 family of microcontrollers.

Because ever since we introduced the 8048 five years ago, it's quietly established itself as the World Standard in every way.

With more customers, more design wins, and more second sources than any other microcontroller. All of which makes our 8048 family a very attractive choice. No matter what you're designing.

Because of the obvious benefits of our learning curve. High volume, lower cost, higher reliability.

Because of the worldwide acceptance of the 8048 architecture. So you can look forward to a long life. And so you can hit the ground running with new applications, cutting both development costs and time to market.

Because the 8048 family is still in the earlier stages of its life cycle. Which means you'll be able to grow right along with it, whether you're upgrading from 4-bit or looking for an easy path for future expansion.

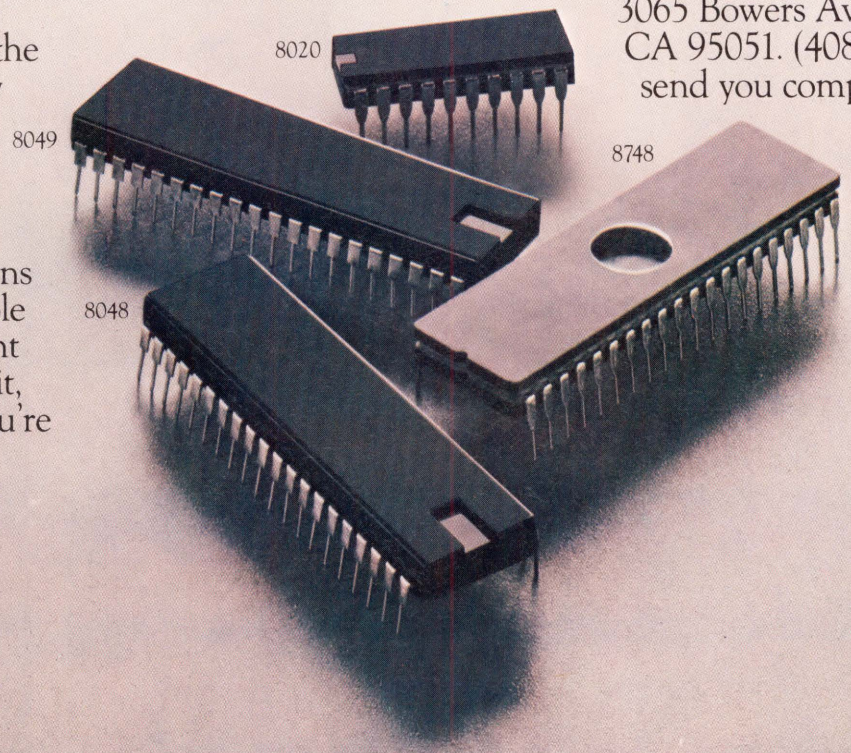
And because we give you pin-compatible EPROM versions for even faster design cycles. Plus a complete package of hardware and software development support. A whole variety of products based on the 8048 architecture, to fit your exact application. And a huge network of factory and field applications engineers to give you the support you need.

With all this going for us, it's easy to see why the 8048 has become the world's best-selling 8-bit microcontroller. And we're fully committed to keeping it that way. You can count on us to deliver the volume you need. When and where you need it.

We'd like to tell you more. About applications. About customer training. And about all the 8048 family. Including our new high-performance 8051. Our new 8749 and 8751 EPROM microcontrollers. And our brand new low-power CHMOS versions, too.

Just get in touch with your local Intel distributor. Or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. (408) 987-8080. We'll send you complete information.

And help you quietly take control of a nice big share of your own market.



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CIRCLE 17 ON INQUIRY CARD

Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Alliance, Almac/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey Industrial Components, Pioneer, L.A. Varah, Wyle Distribution Group, Zentronics.


OEM 8775

STC's new 8775 single spindle disk drive incorporates an ANSI standard SMD interface. As an added plus, this 673 Mbyte disk already has a proven track record even before introduction. That's because it's a single spindle version of STC's double density Winchester disk drive — the dual spindle 8650. This 1.2 gigabyte disk has chalked up an outstanding performance record with over 13,000 units installed.

We've used the same head disk assembly, same electronics, all the same performance proven parts in the new 8775. Added to these same components is a new microprocessor controlled maintenance facility. All at a competitive price.

Also consider STC's total OEM logistics system. This means excellent parts availability, service, customer interface assistance and documentation. Training is available at our facility or yours. Our established logistics system gives you the confidence you demand from a quality OEM supplier.

Now is the time to integrate the STC 8775 into your systems. STC has the proven manufacturing capacity required for volume production of these high performance disk drives. Not just a promise — fact! STC can meet your needs and **will** deliver. For complete details, call (303) 673-4066. Or, write Storage Technology Peripherals Corporation, MD-3N, P.O. Box 399, Louisville, Colorado 80027. In Europe, write Storage Technology Ltd., 2 Rubastic Road, Southall, Middlesex, UB2 5LL, England. Telephone 571-0062.

STC's 673 Mbyte OEM Disk

ANNOUNCEMENT



STORAGE TECHNOLOGY PERIPHERALS CORPORATION

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0244 S-80 11/81

CIRCLE 18 ON INQUIRY CARD

WITH OUR DISK INTERFACE, HAVE THIS

Used to be, upgrading a single disk drive meant sinking a heap of money and man-hours into system redesign.

The interfaces were that incompatible.

Not anymore. Now, with the help of our SA1400 intelligent controllers, every Shugart low cost drive has one common interface. Our new SASI™ (Shugart Associates System Interface).

Design it into your system once—then reap the benefits for generations to come.

Add data storage. Beef up your product line. Upgrade or modify. All virtually at will, without the fuss and colossal cost of traditional hardware or software changes.

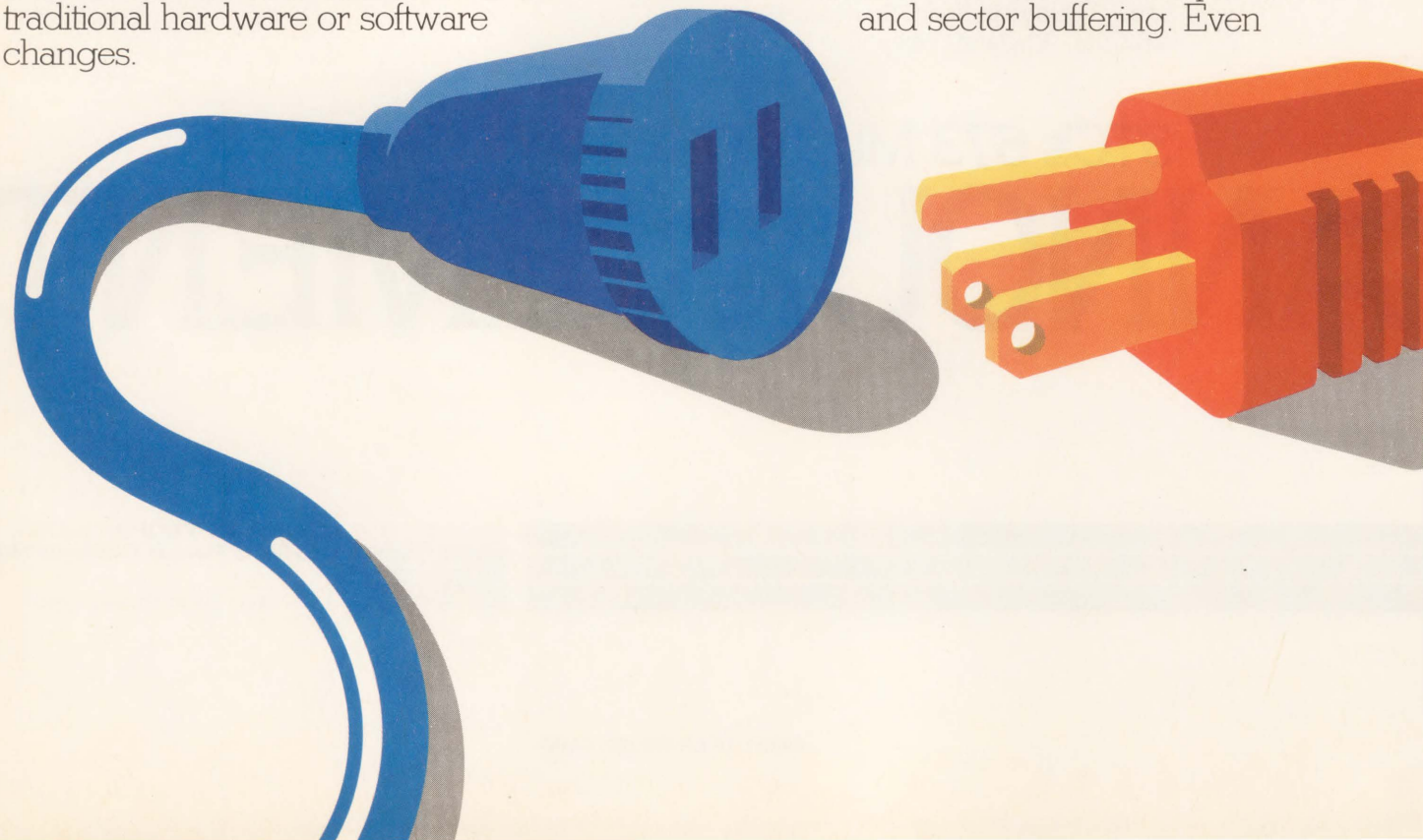
Fact is, thanks to SASI our 96-TPI Minifloppy™ looks the same to your system as our 14-inch Winchester. Same status lines. Same controls. Same commands.

But don't forget, at the heart of our new standard interface is something remarkable in itself.

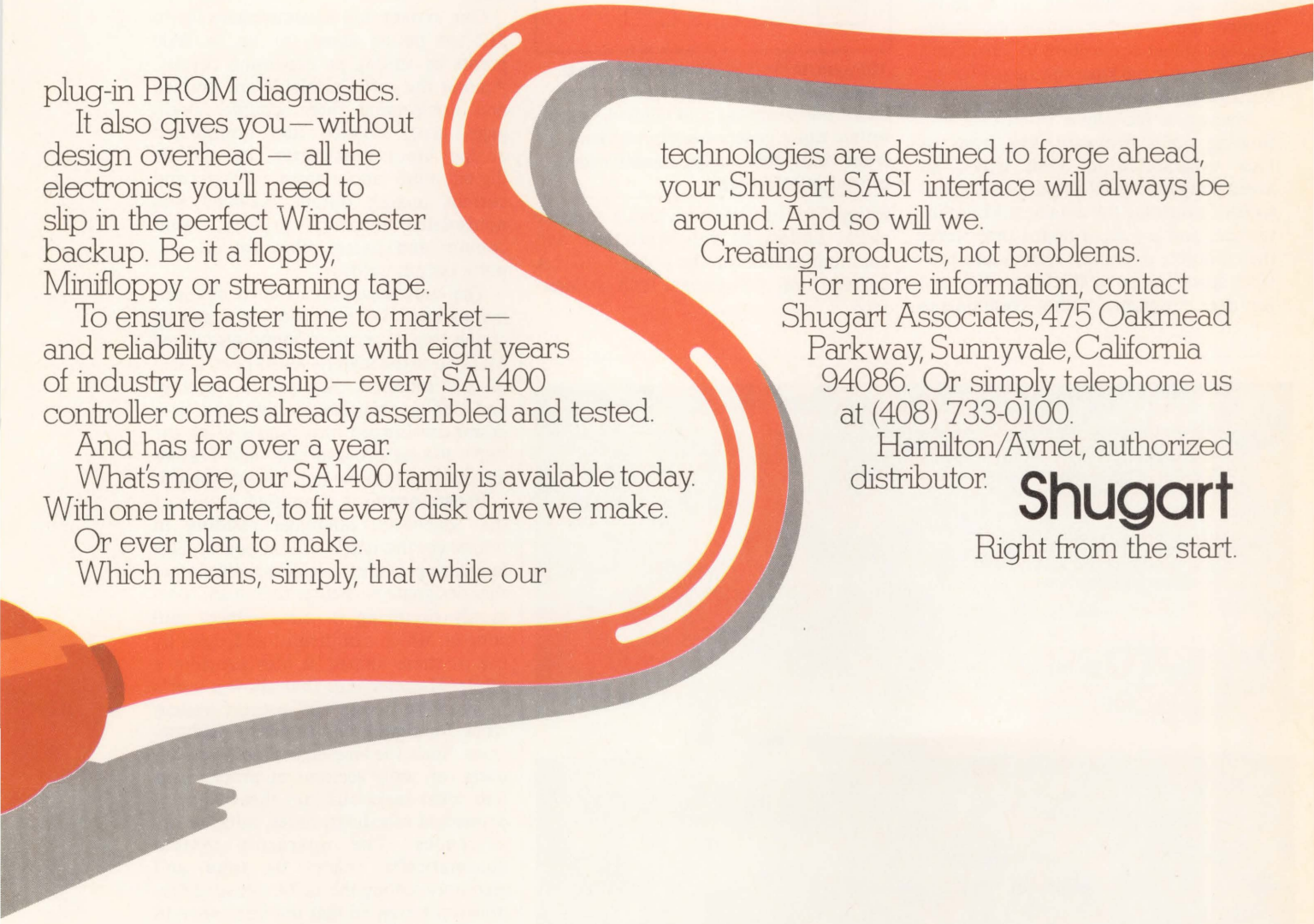
A Shugart SA1400 series controller.

It performs all the automatic, high performance functions that your CPU shouldn't have to handle.

Like error detection and correction, implied search and verify, and overlapped seek. Then there's data separation and sector buffering. Even



STANDARD YOU WILL NEVER PROBLEM.



plug-in PROM diagnostics.

It also gives you—without design overhead— all the electronics you'll need to slip in the perfect Winchester backup. Be it a floppy, Minifloppy or streaming tape.

To ensure faster time to market—and reliability consistent with eight years of industry leadership—every SA1400 controller comes already assembled and tested.

And has for over a year.

What's more, our SA1400 family is available today. With one interface, to fit every disk drive we make.

Or ever plan to make.

Which means, simply, that while our technologies are destined to forge ahead, your Shugart SASI interface will always be around. And so will we.

Creating products, not problems.

For more information, contact Shugart Associates, 475 Oakmead Parkway, Sunnyvale, California 94086. Or simply telephone us at (408) 733-0100.

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Shugart

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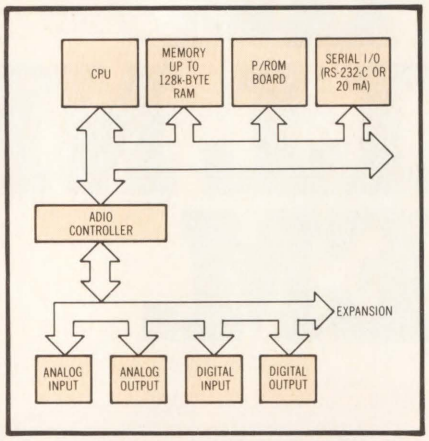
CIRCLE 19 ON INQUIRY CARD

CONTROL & AUTOMATION

P/ROM based control system operates in harsh environments

Storing user and system software in nonvolatile P/ROM, the Macsym 10 eliminates the single most common cause of system failure—moving parts. Reliability of the unit is further promoted by rugged packaging, operation over the 5 to 50 °C temperature range, and dust immunity. According to William L. Miller, product line manager for Analog Devices, Inc, "No other system is available which combines the power and performance of a 16-bit minicomputer with realtime multitasking, and direct connection to sensor and actuators in a package optimized for industrial applications."

Macsym 10 includes a 16-bit CPU with floating point firmware, 96k bytes of RAM expandable to 128k bytes, an analog/digital input/output (ADIO) controller to manage the data acquisition interface, and a P/ROM board that stores the complete operating system and provides space for up to 40k bytes of P/ROM for user programs. Other components integral to the system include a realtime clock, battery backup protection, and communications via the RS-232-C, 20-mA current loop, or optional IEEE 488 interface.



Macsym 10 system architecture. Dual buses used in Analog Device's P/ROM based measurement and control system isolate noise generating digital elements from vulnerable analog signals with central interface unit

The CPU's dual bus architecture supplies high noise immunity and accuracy at a reasonable cost. High speed digital logic elements, generating potentially troublesome electrical noise, are separated from low level analog inputs and other vulnerable analog signals by a central interface unit. This ADIO controller is a key to low cost signal conditioning. It manages the data acquisition interface and isolates the digital bus shared by CPU, memory, and other peripherals from the low noise analog bus.

One system will accommodate up to 512 I/O points alone, or up to 8000 points by adding an expansion chassis. Among the cards available are isolated and nonisolated thermocouple, strain gage, RTD, isolated and nonisolated analog input multiplexer, ac and dc digital input and output, voltage and current analog output, isolated and nonisolated interrupt priority, event counter and pacer, relay output, and pulse output cards.

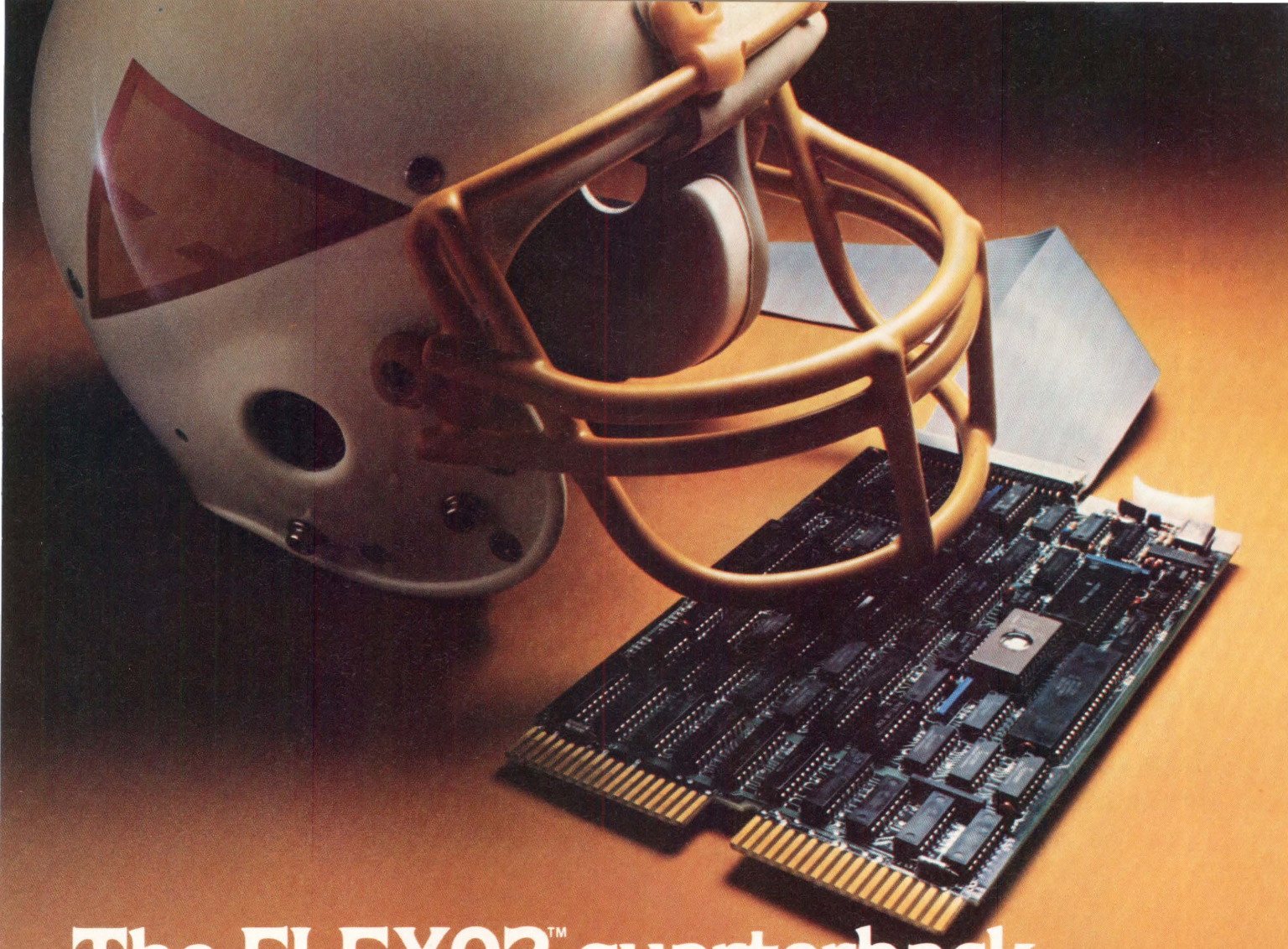
The unit serves as its own development system. Users develop programs by connecting a CRT to a floppy disc based Macsym 10 through its RS-232 port. Using the CRT terminal, they type in, develop, and debug programs. Completed programs are burned into P/ROM using the PRP01 P/ROM programmer, and P/ROMs are inserted into the unit's P/ROM board.

Programming is simplified by use of the MacBASIC language residing in P/ROM on the unit's P/ROM board. This language provides special variable names that designate particular functions, commonly occurring in measurement and control, which can then be addressed by use of these names. It also provides a group of commands that allow a user's program to access and use the system clock for timing and timekeeping functions. Since the language is multitasking, users can write sections of processes as individual tasks and run them with independent schedules, times, rates, or occurrences. The operating system automatically shares its time and resources among the tasks, in user determined priority, so that the tasks seem to be running simultaneously.

Macsym 10 is priced at $12,300 for a system with 96k bytes of RAM and space for 32k bytes of user P/ROM. A system with 128k bytes of RAM and space for 40k bytes of user P/ROM costs $13,400. **Analog Devices, Inc**, Rte 1 Industrial Pk, PO Box 280, Norwood, MA 02062.
Circle 243 on Inquiry Card

Shrouded Headers from the full line of Great Jumper Systems
• Eight sizes, straight and right angle, 10 to 50 contacts
• Selective gold and nickel-silver contacts
• High profile latches (.575 in.), low profile latches (.425 in.), and no-latch options
• Black polyester thermoplastic body, UL-rated 94 V-O
• .100 x .100 in. dual row center spacing, .025 in. diameter posts
• .115 in. and .175 in. solder-tail lengths
• 3, 10, and 20 day deliveries
Call now, toll free, 1-800-321-7075, for full line catalog, design support, samples and orders. Local reps nationwide.
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EXCELLENCE
in Shrouded Headers

CIRCLE 20 ON INQUIRY CARD



The FLEX02™ quarterback. Best stats in the RX02 league.

The FLEX02, dual-width, floppy disk controller is undoubtedly star quarterback material. Carrying out a carefully designed game plan, this AED veteran always calls the right play at the right time, to keep your data flowing smoothly with never a fumble or an interception. And it's part of AED's seasoned line-up of DEC-compatible controller/emulators.

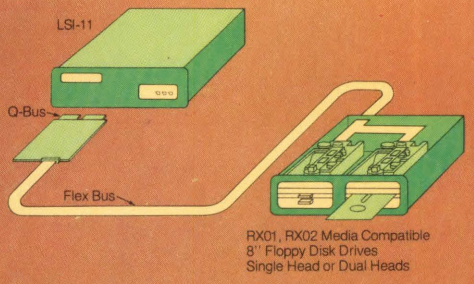
Among FLEX's unique talents is the ability to handle the ball 20% to 70% faster than its DEC counterpart. Another, is its ability to handle dual-headed, double-density disk plays... a feature no other quarterback in the RX02 league can provide. Fully suited, the FLEX02 comes in two packages: two 8" single or dual-head floppies, one dual-width controller card, and power supply, **or** one 23MB, 8" Winchester (not available from DEC), plus one 8" floppy, a dual-width controller board, WINC™ interface, formatter, and power supply in a 5¼" DEC look-alike cabinet. Individual controller boards are also available. Whether you have RSX-11/M, RT-11V3A/B, I.A.S., CTS500 or CTS310 centering the ball, the FLEX02 is completely CPU transparent. And designed to take care of DEC software modifications with microcode changes only.

All this at half the DEC price, and with 30-day delivery.

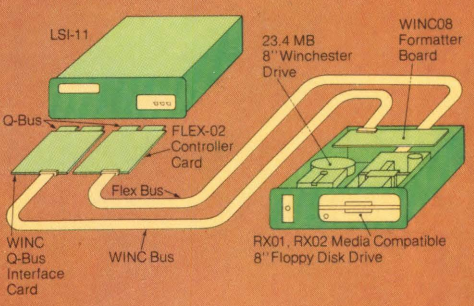
Upgrade your RX02 team today! Send for complete FLEX stats—or call our Marketing Department for the sales office nearest you.

Advanced Electronics Design, Inc., 440 Potrero Ave. Sunnyvale, California 94086. Phone 408-733-3555. Telex 357-498.

Standard FLEX02 Configuration



For LSI-11 Users—FLEX02 with WINC08



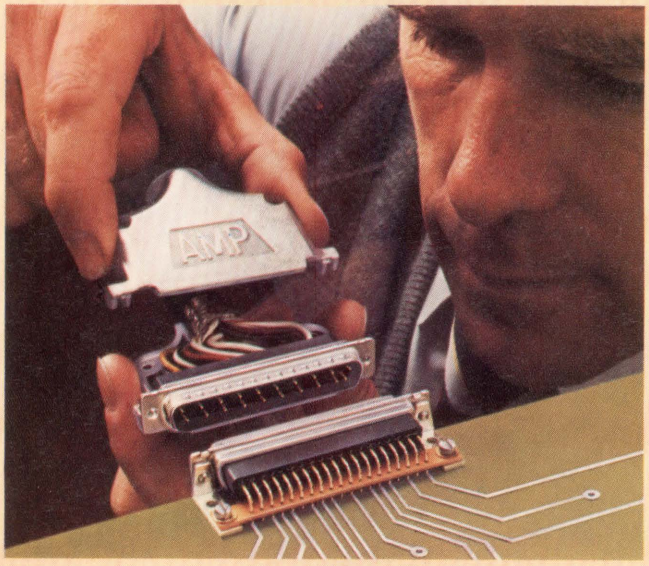
™Trademark of Advanced Electronics Design, Inc.

Cover yourself with our shielded connectors.

They are the cost-effective way to reduce your equipment's electromagnetic emissions, and help you comply with the new FCC emissions regulations.

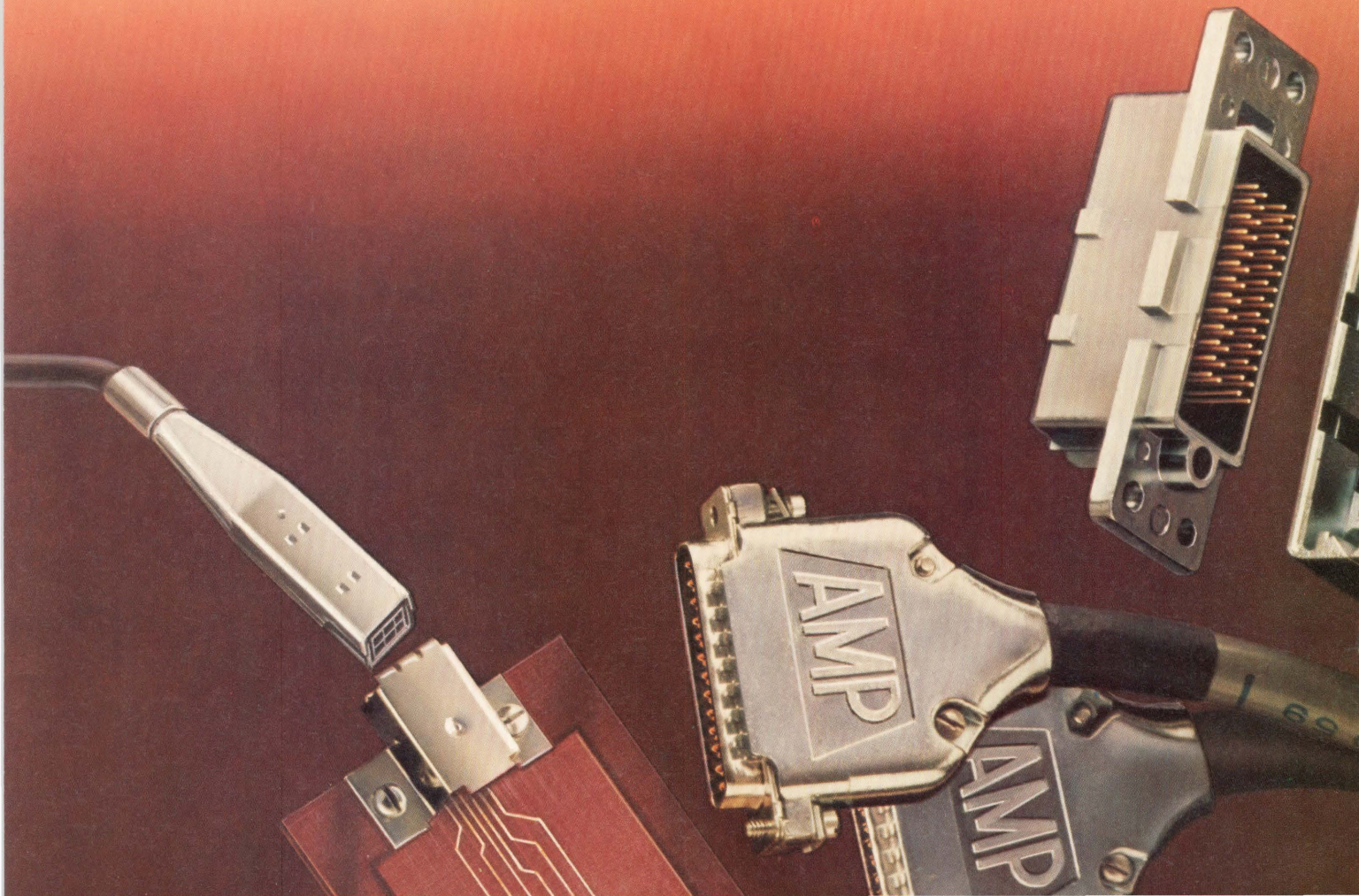
Choose from a wide range of interface styles, all AMP proven designs with compact, easy-to-assemble shields.

Our AMPMODU MT connector offers mass termination savings in .100" centerline post/receptacle format. AMPLIMITE connectors mate with similar subminiature D designs.

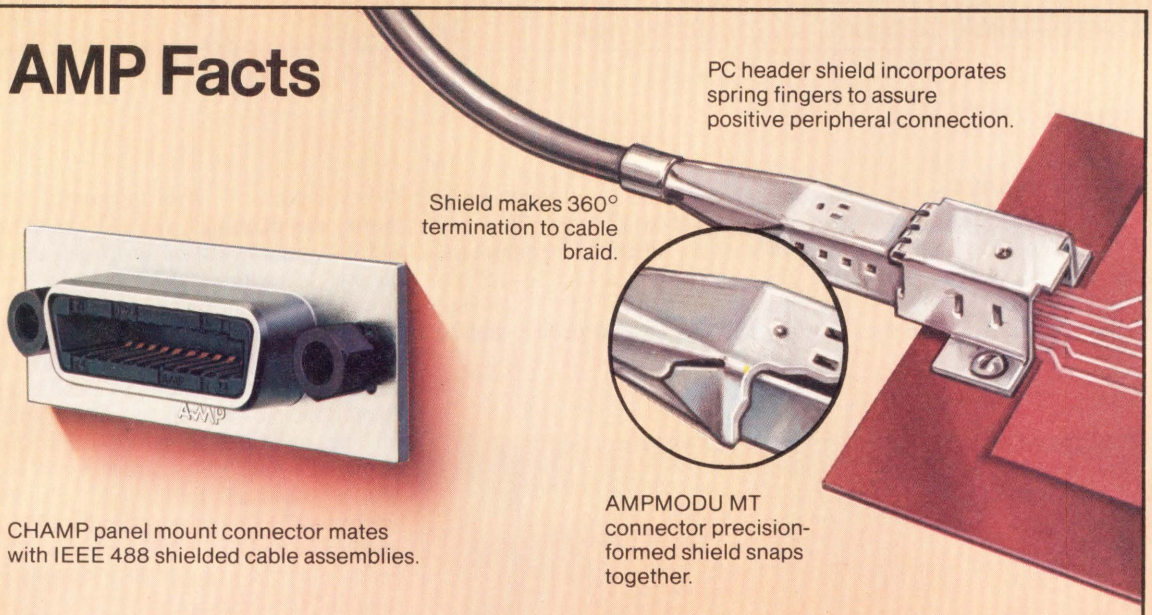


If you prefer a circular connector, our shielded version offers a positive one-turn locking ring. And for high pin counts, the CR Series gives you zero insertion force mating.

You couldn't ask for better protection.



AMP Facts



PC header shield incorporates spring fingers to assure positive peripheral connection.

Shield makes 360° termination to cable braid.

CHAMP panel mount connector mates with IEEE 488 shielded cable assemblies.

AMPMODU MT connector precision-formed shield snaps together.

For more information, call the AMP Shielded Connector Desk at (717) 780-8400.

AMP Incorporated, Harrisburg, PA 17105

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AMP means productivity.

CIRCLE NUMBER 10



MICROPROCESSORS/ MICROCOMPUTERS

Desktop computer allows users to develop and display graphics

A completely integrated stand-alone desktop system, Advantage offers minicomputer-grade graphics capabilities for under $4000. Additional features incorporated into the system are built around a 4-MHz Z80A® and 64k bytes of RAM by North Star Computers, Inc. The unit features a 12″ (30-cm) bit-mapped CRT display, 5.25″ (13.34-cm) high capacity floppy disc drives, and an 87-key Selectric® style keyboard. Bar charts, pie diagrams, plotted graphics, and 3-D visuals can be produced using the system's additional 20k bytes of RAM to support the bit mapping feature.

Central to the system's capabilities is the 12″ (30-cm) bit-mapped CRT display screen that allows users to develop and display their own graphics. The display can be operated as a 1920-character display (24 lines x 80 characters) or as a 240 x 640-pixel bit-mapped display, where each pixel is controlled by 1 bit in the display-dedicated 20k-byte RAM. The Z80A CPU controls full graphics capabilities of the system.

In addition to the main CPU, the unit contains a 2k-byte bootstrap P/ROM and an auxiliary Intel 8035 microprocessor that controls the keyboard and floppy discs. The n-key rollover keyboard contains 49 standard typewriter keys, 9 symbol or control keys, a 14-key numeric/cursor control pad, and 15 programmable function keys.

Six slots in the chassis accept plug-in option cards that provide a parallel interface for either printer or hard disc, RS-232-C serial port, or high speed floating point arithmetic with up to 14-digit precision.

Also offered for the 18.8 x 20 x 12.5″ (47.6 x 51 x 31.8-cm) unit are proprietary application software modules. These include an operating system called Application Software Program (ASP) that manages system resources and provides an Indexed Sequential Access Method (ISAM) and Random File Management system interface for the application software packages. These packages include the accounting application software package (ACCPAC™), Northword word processing package, Mail Manager mailing list processor, and InfoManager data manager. ACCPAC and the other modules are written in the C programming language. An application development system (ADS) is available for developers who require modification of existing modules or need facilities to develop their own application modules.

Graphics DOS (G-DOS) is a proprietary floppy disc operating system. Developed for the system, G-DOS permits a user or application program to issue commands for maintaining and using diskette based files or for using the optional floating point board and serial printer. It also provides a user friendly operator interface and supports the company's proprietary Graphics BASIC.

(continued on page 52)



Don't get shot down by the FCC!
Call Dayton T. Brown, Inc.

The FCC rules and regulations are specific about the correct method of conducting a test program. The incorrect approach to your FCC testing can lead to poor results and added cost. You do not have to take any chances.

At Dayton T. Brown, Inc. we perform FCC testing in accordance with the rules and regulations.

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Dayton T. Brown, Inc., delivers test results you can rely on. We have the distinction of providing the test data for some of the first units ever certified by the FCC to meet part 15, subpart J, for digital electronic products, the new requirement!

To be sure call Dayton T. Brown, Inc., to perform your FCC engineering and testing. We have been assisting manufacturers to meet government regulations for more than 30 years. We can help you too!

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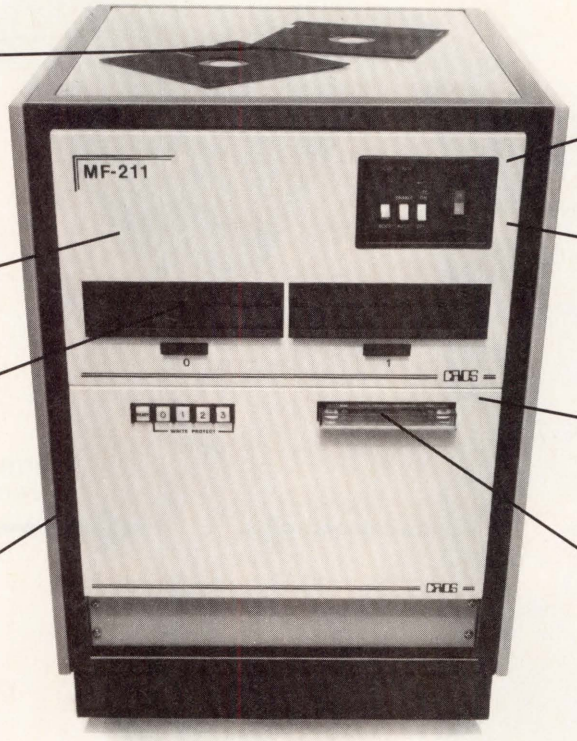
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Church Street
Bohemia, L.I., New York 11716
Tel: 516-589-6300

For a free poster of this ad, send us your business card, attention, FCC

CIRCLE 22 ON INQUIRY CARD

$--,---?

See Us At COMPEX'81



UNIX-compatible Idris operating system, or DEC-licensed RT11V4

LSI-11/23 central processor with 128 kbytes of memory

Chassis with eight-quad-slot backplane and power supply

Floppy disk controller, hard disk controller, and quad serial interface

Dual double-density floppy disk drives

20.8 megabyte Winchester hard disk (equivalent to four RL01s)

30-inch-high, office-style enclosure, including cabling

Optional cartridge tape backup

Guess Again.

The price tag on this remarkably potent LSI-11/23-based system is just $16,000. That's well below the combined list price of its components and probably a lot less than you'd expect to pay. And this is only one of a whole series of 11/23 and 11/2 configurations we're offering right now at special complete-system prices.

You don't have to give up security for low cost, either. These are carefully integrated and fully DEC-software-compatible systems, backed up by a free 90-day warranty, our very efficient and economical module exchange service policy, a complete documentation package, and our eight years' experience building DEC-compatible systems.

For more information on these and all our other DEC-compatible products, just call. Or mail us the coupon below.

CD11

Send me more information on your DEC-compatible systems.

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Charles River Data Systems, Inc.
4 Tech Circle, Natick, MA 01760/(617) 655-1800

CHARLES RIVER DATA SYSTEMS

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CIRCLE 23 ON INQUIRY CARD

'Tight-grip' Contacts



TEST RESULTS

Test	Procedure	Results
Corrosive Atmophere	Ammonium Polysulfide Nitric Acid	Final R_C=9.3 m Ω Final R_C=8.4 m Ω
Salt Spray	MIL-STD-1344, Method 1001	No Damage R_C=11.7 m Ω
Humidity	MIL-STD-1344, Method 1002	No Damage R_C=14.8 m Ω
Thermal Shock	MIL-STD-1344, Method 1003	No Damage R_C=11.7 m Ω
Mechanical Shock	MIL-STD-1344, Method 2004	No Discontinuity
Vibration	MIL-STD-1344, Method 2005	No Discontinuity
Socket Durability	500 mating/ unmating cycles	Initial R_C=11.8 m Ω Final R_C=11.8 m Ω
Temperature Life	MIL-STD-1344, Method 1005, 1000 hours	Insulation Resistance $> 5x10^9$ Ω Initial R_C=11.1 m Ω Final R_C=14.9 m Ω

PRODUCTS TESTED: IDS-26-G30 and IDH-26-S1-G30

Unique RN "tight-grip" contact clamps cable firmly for gas-tight reliability (microphoto above). Total normal force is applied directly against cable. Vector arrows show normal force is maximized to clamp conductors tightly. No chance for gas penetration or corrosive buildup…even in hostile environments. And a special cut-out evenly distributes stress for long spring life and maximum reliability.

...assure gas-tight reliability

in RN IDC flat cable system

Robinson Nugent's unique contact design (microphoto shown at left) offers consistent, long-term dependability in your IDC flat cable interconect system. Test prove conclusively that RN "tight-grip" contacts maintain low contact resistance—even in corrosive atmospheres or under severe vibration. Plugs, sockets, edge cord and transition connectors all provide the same low electrical resistance and gas-tight reliability—for a highly reliable, trouble-free flat cable system.

Simple, one-piece connector design allows high speed assembly using IDC tooling already in place. Fewer pieces mean reduced inventory. And you get assured compatability of cable, connectors and headers...because RN supplies them all.

Call or write today for the new Robinson Nugent IDC Flat Cable System catalog—complete with all specifications and technical details.





RN® ROBINSON NUGENT, INC.

800 East Eighth Street, New Albany, Indiana 47150 • Phone: (812) 945-0211—TWX: 810-540-4082

CIRCLE 24 ON INQUIRY CARD

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Mate, yer needs to call upon Reticon® to 'elp you out ...



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Non-Contact Measurement, Process Control, Pattern Recognition, Solid State, Image Sensor Cameras and Camera Sensor Components.

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EG&G RETICON

345 Potrero Avenue, Sunnyvale, CA 94086

MICROPROCESSORS/ MICROCOMPUTERS

Graphics CP/M is a compatible enhancement of CP/M, the industry standard operating system for developing and executing programs on floppy disc based Z80 systems. Graphics CP/M is a superset of CP/M that allows users to take full advantage of the extensive graphics capabilities of the system and to run all CP/M compatible software on the system. FORTRAN and COBOL are both offered under CP/M. **North Star Computers, Inc**, 14440 Catalina St, San Leandro, CA 94577.

Circle 244 on Inquiry Card

SOFTWARE

Scientific and business graphics software run on latest terminals

The DISSPLA® scientific and TELL-A-GRAF® business computer graphics software systems, both offered by ISSCO®, have been interfaced to recently announced Tektronix and Hewlett-Packard graphics display terminals. The Tektronix terminals are members of the 4110 series, which includes the TEK 4112 raster scan monochrome display unit and the TEK 4114 computer display terminal with a direct view storage tube. The software package also interfaces to the HP2623A, a unit combining display and an optional built-in graphics printer.

With the addition of interfaces for these two terminals, the company's software systems now provide a standard interface to over 55 types of graphics equipment such as terminals and plotters. Customized interfaces are also available.

The scientific/engineering oriented system uses a set of FORTRAN subroutines to produce graphic output and requires users to have a working knowledge of programming language. The business system is based on English language commands.

A broad range of software support services is offered, including pre-installation, installation, and post-installation services. Users can also subscribe to a maintenance and update service including phone-in consulting and problem analysis. **ISSCO**, 4186 Sorrento Valley Blvd, San Diego, CA 92121.

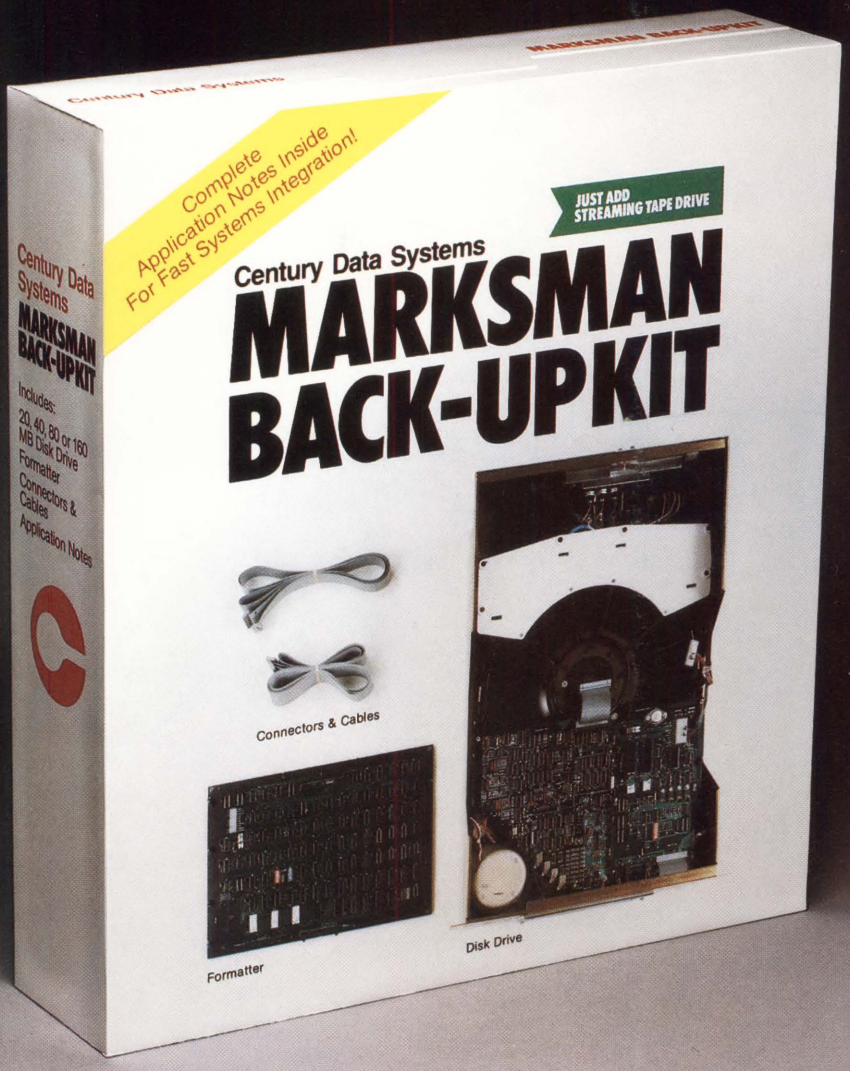
Circle 245 on Inquiry Card

CIRCLE 25 ON INQUIRY CARD

Century Data Systems
A Xerox Company

Drives for the 80's

Finally, an off-the-shelf answer to Winchester back-up.



Introducing the Intelligent Marksman Back-Up package. And the solution to the chronic problem of Winchester back-up.

And what a solution it is. Our new formatter is specially designed to control 20, 40, 80 or 160 MB Marksman Winchesters—and the Archive Sidewinder, Cipher Quarterback, or DEI Streamer ¼-inch tape drive for back-up.

A simple host adapter and software I/O drivers are all you need to tie into word and data processors utilizing interfaces such as S-100 or Multibus, and running operating system environments such as CP/M, MP/M, UNIX and others.

If that isn't enough, just one formatter will control two Marksman Winchesters, providing a system with a storage potential of 320 MB, in a minimum of space.

Continued on next page

Century Marksman drives: Because it's a jungle out there.

In the world outside the computer room, computer data faces constant danger.

The people out there smoke cigarettes and spill coffee. They raise dust and trip over power cords and do everything else no one would do inside the computer room.

Earlier generation disk drives just can't protect data from that kind of abuse.

But Winchesters can. A Winchester's sealed design makes it the perfect choice for any outside-the-computer-room application: Word and data processing, computer graphics, networked data storage, data entry, computerized numerical control and any other hostile environmental applications you can think of.

But ruggedness isn't the only advantage you get with a Winchester. There's also the massive storage capacities ranging up to hundreds of megabytes per drive. Which means you can build in a system's capacity to grow.



And finally, there's the Century Data Marksman Winchester. It combines all of these advantages with the lowest cost per megabyte in the industry.

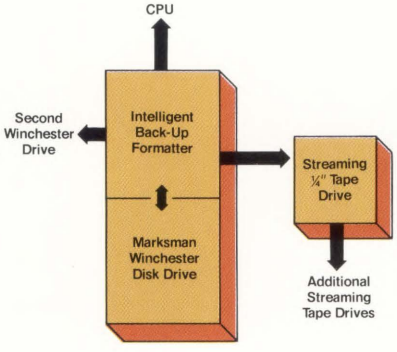
So before you send any system out into the world beyond the computer room, be sure it's equipped with a Century Marksman Winchester.

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back-up. *Continued from first page*

A storage system independent of the CPU.

But back-up isn't nearly all our new formatter offers. You also get an independent data storage package that doesn't tie up valuable CPU time.

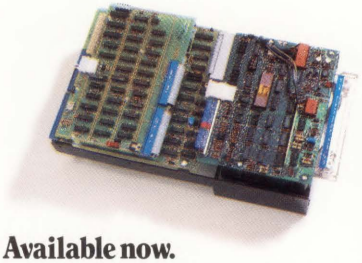


The formatter permits independent communication among all its interconnects: From disk to tape. Tape to disk. Or either drive to and from the CPU.

Which means operators can continue to use the CPU during back-up, and even interrupt the Winchester-tape intercommunication to pull out or insert data from the disk. Without specifically shutting down and restarting the back-up functions.

The advantages of streaming tape.

Compatibility with streaming tape back-up is another big plus of the new Century formatter. As a removable media, ¼-inch streaming tape is ideal for archiving data. It's also a low-cost, high-performance, no-maintenance tape option perfectly matched to the speed and capacity of a Winchester.



Available now.

Best of all, our new formatter isn't just a promise of something to come. It's available now, right along with our full line of Marksman Winchesters and full application notes.

So if you're an OEM, systems integrator or distributor, let's get together soon. And get the problem of Winchester back-up off your back once and for all.

Sidewinder is a trademark of Archive Corp.; Quarterback is a trademark of Cipher Data Products; Streamer is a trademark of Data Electronics Inc.; CP/M and MP/M are registered trademarks of Digital Research, Inc.; Unix is a trademark of Bell Laboratories; and Multibus is a trademark of Intel.

Century Winchesters don't crash, they land.

You've heard of crashed disks before. But you've probably never heard of one in a Winchester.

That's because Winchesters rarely crash. And at Century Data, we take special pains to make sure of it.

In addition to the standard protection of disk lubrication and feather-light heads, we've designed a unique braking system and special head landing zones where no data is stored.

During a power failure or reduction, the brakes automatically slow the disk in seconds rather than minutes. And the head is programmed to seek out it's special data-free landing zones.

The combination not only prevents crashes, it virtually insures the data's integrity even if the landing is a little bumpy.

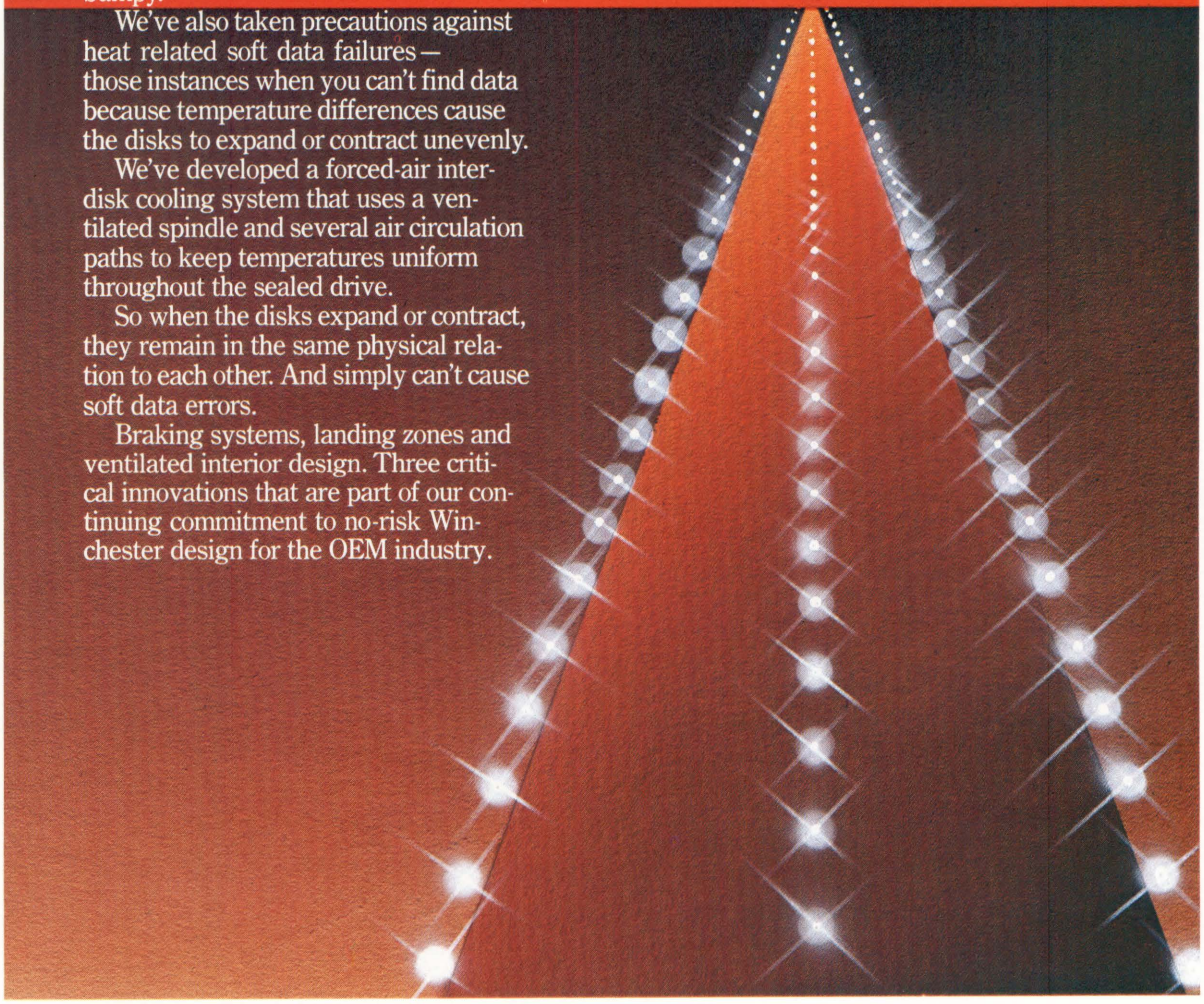


We've also taken precautions against heat related soft data failures—those instances when you can't find data because temperature differences cause the disks to expand or contract unevenly.

We've developed a forced-air inter-disk cooling system that uses a ventilated spindle and several air circulation paths to keep temperatures uniform throughout the sealed drive.

So when the disks expand or contract, they remain in the same physical relation to each other. And simply can't cause soft data errors.

Braking systems, landing zones and ventilated interior design. Three critical innovations that are part of our continuing commitment to no-risk Winchester design for the OEM industry.



Q: Why have you chosen Trident removable-pack drives for Japan, Mr. Kato?

A: Because of Century's design and commitment to quality.

Mr. Atts Kato is U.S. Manager for NELCO, the electronics subsidiary of Nissho Iwai—one of the largest international trading companies in Japan. The following is excerpted from an interview with Mr. Kato:

Q: After reviewing other manufacturers of removable-pack drives, what has brought you to Century?

A: Frankly, I've never seen such advanced facilities as Century's.

I've been involved in the computer business for twenty years, and have visited many U.S. computer companies. Century Data facilities for engineering, manufacturing and testing all indicate a serious commitment to disk drives.

This was a very important factor for me in selecting a manufacturer—one that can make hundreds of drives like Century has done for me.

Q: How are these drives being used in Japan?

A: We often sell the Trident drives to OEMs and systems houses, but we have other large end-users that buy quite a few. For example, Tokyo Electric Power, which is the largest utilities company in the world, and many Japanese broadcasting companies.

You see, the Japanese market situation is very similar to that of the U.S. Removable-pack drives are seen as having many desirable features, particularly storage capacity and removability. Winchesters are just now seen as becoming a good product to integrate into systems.

We see our disk business changing to Winchesters over the next few years, and this was another key reason why Century capabilities were so important to us.

As our demand for Winchesters grows, we will look upon Century to fill this need—particularly with their new products becoming available now and in the near future.

NELCO covers the entire Japanese computer market, offering individual components as well as totally integrated systems with extensive technical support capabilities for both hardware and software. And NELCO has chosen Trident removable-disk drives from Century Data Systems.



Now media compatible.

Our 300 MB Trident now provides full plug and media compatibility with other SMD-interface removable-pack disk drives. Now, Tridents can be integrated into systems without losing access to existing disk libraries.

If you would like to find out more about our proven drives and these attractive features, contact us at our address below, or feel free to give us a call.

For the full Story of the Century, please indicate the information you want, and we'll send it right away.

- ☐ Intelligent Marksman Backup Package
- ☐ Marksman Winchester Disk Drives
- ☐ Trident Removable-Pack Disk Drives
- ☐ I would like an evaluation unit of the above.

Name_____ Title_____

Company_____

Street_____

City/State_____ Zip_____

Phone (_____)_____

Send to: Century Data Systems, 1270 N. Kraemer Blvd., Anaheim, CA 92806

CD

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DATA COMMUNICATIONS

Processors, workstations, interface chip, and personal computer local network aim at the office environment

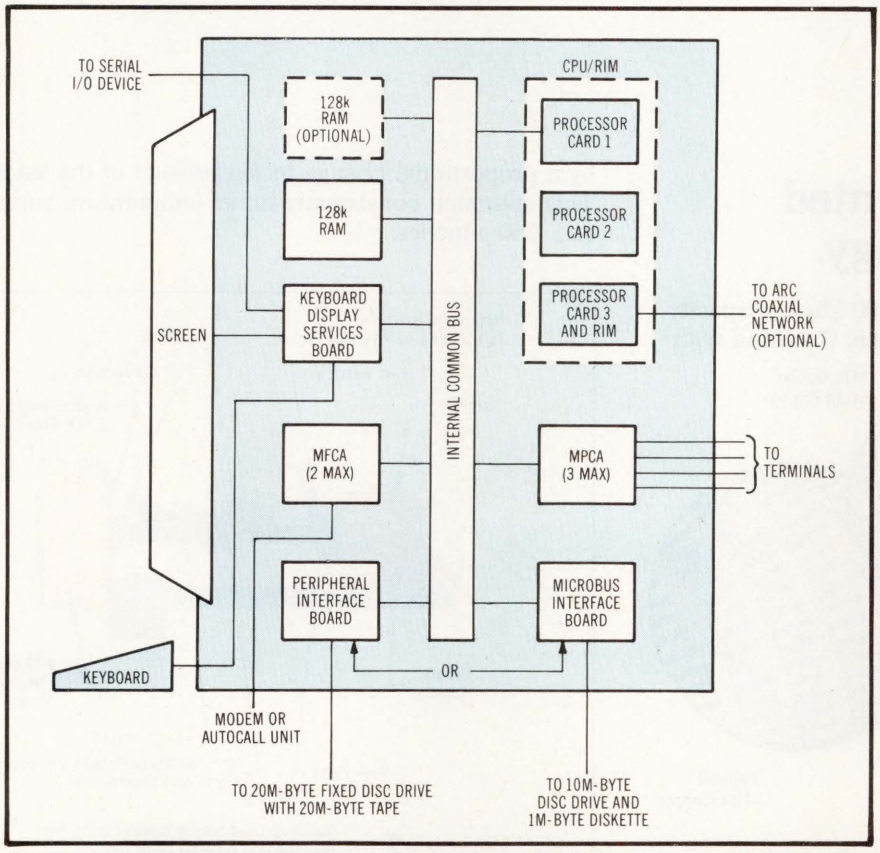


Fig 1 8602 processor configuration. Optional multiport communications adapter (MPCA) handles four asynchronous RS-232-C serial ports. Multifunction communications adapter (MFCA) accommodates serial synchronous or asynchronous communications channel, reverse channel, RS-232-C or RS-422/423 compatible, RS-366 or -366A autocall unit

In a recent multifaceted joint announcement, two major Texas firms launched an assault on the office of the future market with a variety of products and a cooperative venture. Products include a 20M-byte hard disc and streaming tape subsystem, a family of processors and workstations, and a local network interface chip from Datapoint Corp. Concurrently, Tandy Corp/Radio Shack announced that it would use ARCNET, the local network component of Datapoint's Attached Resource Computer (ARC™) system as an economical medium for a high speed network of its TRS-80® model II microcomputers.

Hard disc system. Designed and manufactured by Datapoint, the 9301 is a fixed media thin film minidisc system that can store 20M bytes on a stack of 5.25″ (13.34-cm) platters. It also incorporates a 20M-byte cartridge tape drive, an intelligent controller, and power supply in a 21.9 x 24.0 x 7.5″ (55.6- x 61.0- x 19.1-cm) desktop cabinet.

The integrated 0.25″ (0.56-cm) tape cartridge can be used for system backup or for transferring data from one system to another. The read head uses a proprietary technique that automatically aligns the head to each tape and compensates for variations in head alignment among different machines.

In the disc drive unit, a film coating on the discs protects stored data against mechanical damage. An error correction code detects and corrects hardware errors without disturbing user operations. Data management and control functions are handled by the disc controller. It transfers data from disc to tape and vice versa without processor or operator intervention. The controller can back up the contents of an entire 20M-byte disc in about 12 min with the tape moving at 56.3″ (143 cm)/s. Up to four 20M-byte extension disc drives are available for a maximum system storage of 100M bytes.

Processor series. First in a new family of processors and workstations, the 8600 business computer is a full-function workstation that can perform in word processing, data processing, and electronic mail applications. It is fully compatible with the ARC local network and can also be used as a standalone system. The 8600 series can run on both the company's DOS and the new Resource Management System™ (RMS). In an ARC configuration where both operating systems are available, either can be selected via the keyboard.

Designed to be user friendly, the 8600 has a 12″ (30-cm) diagonal screen that provides a 5.4 x 8.9″ (13.7- x 22.6-cm) viewing area. Characters are displayed in an amber shade against a dark brown background in 24-line x 80-col format. Characters are 7 x 9 dot matrix, and screen intensity can be controlled from the keyboard to any of 16 levels. The keyboard is connected to the processor by a 1-m flexible coiled cable, and an optional tilt/rotate base allows adjustment for operator viewing convenience.

Basic 8600 memory is 128k bytes expandable to 256k. The memory consists of 16k-bit MOS dynamic chips and includes parity. Disc data are transferred over DMA paths using gate array technology. A Resource Interface Module (RIM) chip has been developed to handle the protocol required to interface to the ARC network; it replaces the separate boxes or circuit boards previously used for that purpose. The custom 40-pin LSI package is built directly into the 8600 central processor. The CPU itself is implemented on three boards: a control board, an ALU, and the third for the RIM, system ROM, and other functions (Fig 1).

High level languages such as DATABUS®, DATASHARE®, COBOL, FORTRAN and BASIC-Plus, as well as office applications such as word processing and electronic message services are supported. The 8600 uses an expanded 6600-class instruction set, and throughput is about the same as that of the 6000-series processors.

There are four configurations of the processor series. Basic system 8601, designed as an applications processor in an ARC network, has 128k or 256k memory, an RS-232-C serial port for printer or terminal, and is priced at $7500. More versatile 8602 at $10,950 has the same memory capabilities but can be enhanced by adding integral multiport communications adapters with four ports each for terminal support, and

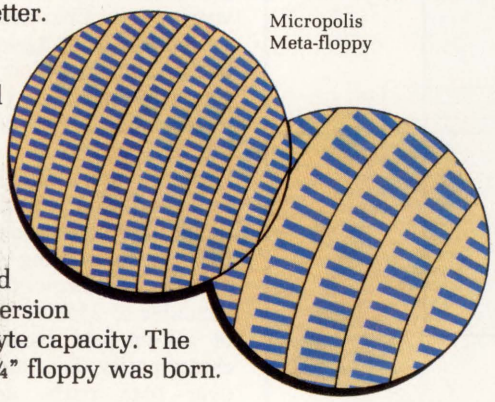
(continued on page 60)

CIRCLE 26 ON INQUIRY CARD

Some plain 96/100 TPI

FACT: We invented 1 megabyte technology.

When the mini-floppy, with less than 100 kbytes capacity was introduced in 1976, we had a choice. Go along with the rest or do better. We chose to do better. Within a year we doubled both bit density and tracks per inch, resulting in a single sided floppy with 0.5 million bytes and a double sided version with one megabyte capacity. The high capacity 5¼" floppy was born.



Micropolis Meta-floppy

Typical Mini-floppy

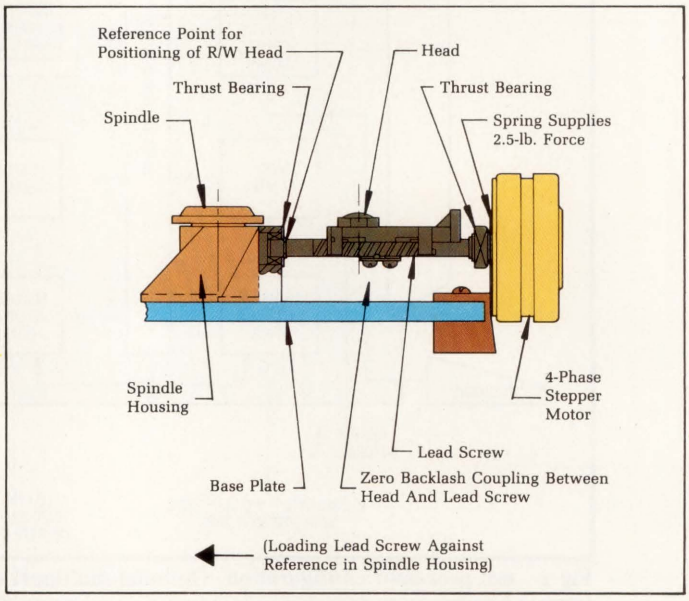
FACT: It took solid engineering to do this.

To quadruple capacity, yet keep interchangeability at the highest level, was no easy task. It took solid, innovative engineering at all levels. The result:

• **Disk Centering Mechanism** - In our drive, the center of the diskette fits over a profiled spindle and is clamped into place while the spindle rotates to assist centering. This technique assures precise centering to within 250 μ-inches and eliminates disk crunching problems.

• **Head Positioning Accuracy** - A precision ground stainless steel leadscrew with metal follower provides more precise positioning than the run-out sensitive pulley and belt approach used by others. Use of a four phase stepper motor and four steps per track averages the effects of all stator and rotor poles, resulting in ± 83 μ-inches positional accuracy.

• **Temperature Compensation** - Our temperature compensation loop includes only the diskette, pre-loaded leadscrew and spindle housing. The baseplate is specifically excluded since its expansion is compensated by a proportional change in the preload of the leadscrew. This approach consistently limits temperature variations to ± 250 μ-inches.



• **Balance Between Speed & Accuracy** – We chose 10ms track-to-track positioning and 380 kbps transfer rate as an optimum balance between speed on one hand, and accuracy and interchangeability on the other.

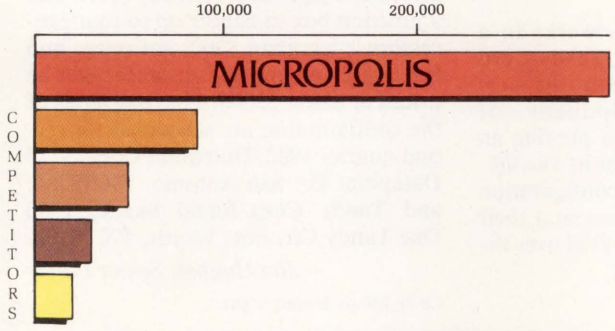
• **Silent Operation** - In band type drives an annoying chatter results from the head's travel from track to track. Our precision stainless mechanism eliminates this noisy irritation.

FACT: Our drives really work.

While others are still learning, our 96/100 TPI drives are operating reliably in systems all over the world. So well, in fact, that we're extending the warranty to 12 months on new OEM agreements. Design and process controls learned years ago, coupled with effective quality control, assures drives ready to work in your system.

facts about 5¼" floppies

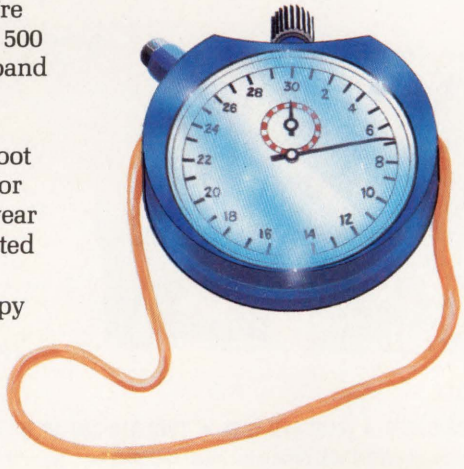
FACT: We've delivered more 96/100 TPI drives to OEM's than all others.



To date we've delivered over 200,000 double track density drives; more than all of our competitors combined. Hundreds of manufacturers of successful small business systems have selected Micropolis drives for their cost effectiveness and proven reliability.

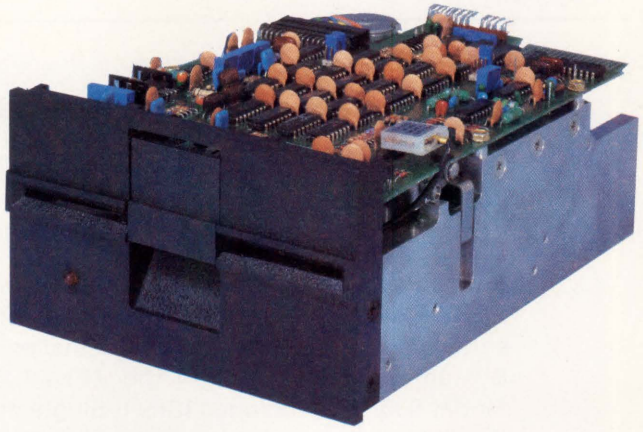
FACT: We're producing more than one each minute.

If you need high performance floppies on time, and in quantity, come to Micropolis. We're producing over 500 a day... and expand ing. Expansion includes a new 60,000 square foot plant planned for occupancy by year end and dedicated completely to 96/100 TPI floppy production.



FACT: We've invented again - A 2 megabyte 5¼ inch floppy.

At NCC we introduced a new 2 megabyte floppy, made possible by again doubling density to 12,000 bits per inch. Micropolis' Model 1117 has 6ms track to track positioning, 500 kbps transfer rate and a host of features including a "chassis within a chassis" for unparalleled electrical shielding and resistance to mounting effect. Industry standard mounting and bezel permit easy introduction into existing systems.



So you win both ways with Micropolis. If you need 96/100 TPI floppies now, order our field proven 1015/1016 series. If you're working on a new system, design in our 2 megabyte Model 1117, the high performance "chassis within a chassis" floppy.

For more information phone us or write on your letterhead.

MICROPOLIS™

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Positions available for talented people.

DATA COMMUNICATIONS

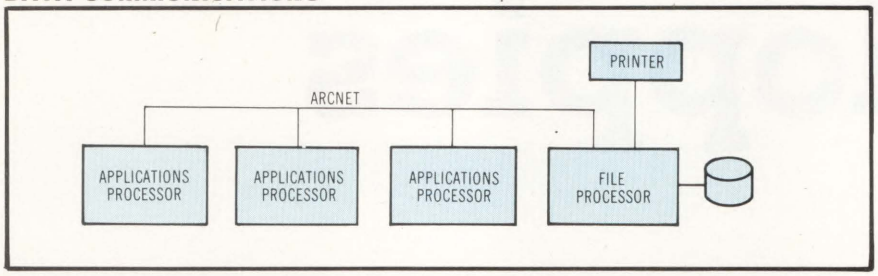


Fig 2 Microcomputer network. System can grow as required in small increments to 255 stations max. Multiple TRS-80s on network can access common data bases and share use of peripherals. Network is transparent to user

multifunction communications adapters for supporting a broad range of communications protocols plus programmable baud rates from 110 to 56k. The 8620 system ($28,500) consists of the 8602 processor and 10M-byte 9310 cartridge disc drive with a 1411 1M-byte diskette drive for backup. It can support up to four 9310 drives for 40M-byte storage capacity. The 8630 system ($33,500) is based on the 8602 and includes the 9301 20M-byte fixed disc and tape system described earlier that can be expanded to system storage of 100M bytes. Both 8620 and 8630 systems can run under control of RMS operating system either standalone or as RMS ARC data resource processors. Lease, rental, and maintenance contracts are available.

Local microcomputer network. In a concurrent announcement, Tandy Corp said that it would use ARCNET, the local coaxial network component of Datapoint's ARC system, to provide an economical local medium for its TRS-80® model II computers. The configuration permits up to 255 computers and their peripherals to be interconnected over the 2.5M-bit/s network (Fig 2).

Datapoint ARCNET protocols and software and an LSI network interface component will implement the low cost common resource system. Bisynchronous communications software packages are available to permit linking the microcomputer network to IBM, DEC, and other mainframes. Compatible applications software, 8.4M-byte hard disc storage, and dot matrix or letter quality printers are available for the system.

Each computer added to the network requires an interface card that fits into an existing card slot in the TRS-80 model II. Other necessary elements are RG-62 coaxial cable and connectors, and a junction box. The interface card is priced at $400; cable is about $1/ft, and a junction box to handle up to four processors is less than $200. An active hub for larger systems and distances will be priced at about $2000. First deliveries of the configuration are scheduled for second quarter 1982. **Datapoint Corp,** 9725 Datapoint Dr, San Antonio, TX 78284; and **Tandy Corp/Radio Shack,** 1800 One Tandy Ctr, Fort Worth, TX 76102.

—Jim Hughes, Senior Editor

Circle 246 on Inquiry Card

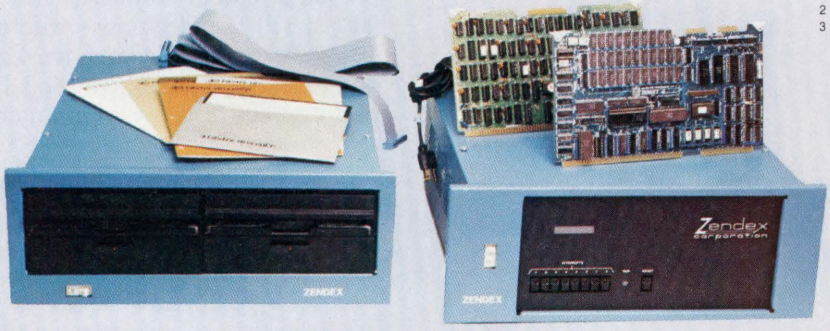
THE ZENDEX[1] MODEL 835 DEVELOPMENT SYSTEM

"High Performance At A Low Price"

Plug compatibility. That's what the ZENDEX Line offers you. Any board or software that works on your Intel[2] Intellec[2] System will also work in the ZENDEX Model 835. That includes ISIS-II Single or Double Density, In-Circuit-Emulators, and Universal PROM Programmers.

The Model 835 System includes a cabinet with two Shugart SA801R Drives, and a CPU cabinet that utilizes the powerful ZX-85 SBC CPU, ZX-200A MMFM & FM Diskette Controller, and parallel IO Interfaces for CRT, TTY, LPT & UPP. CP/M[3] Operating Systems included.

1 — TM ZENDEX Corp.
2 — TM INTEL Corp.
3 — TM Digital Research



Zendex® corporation

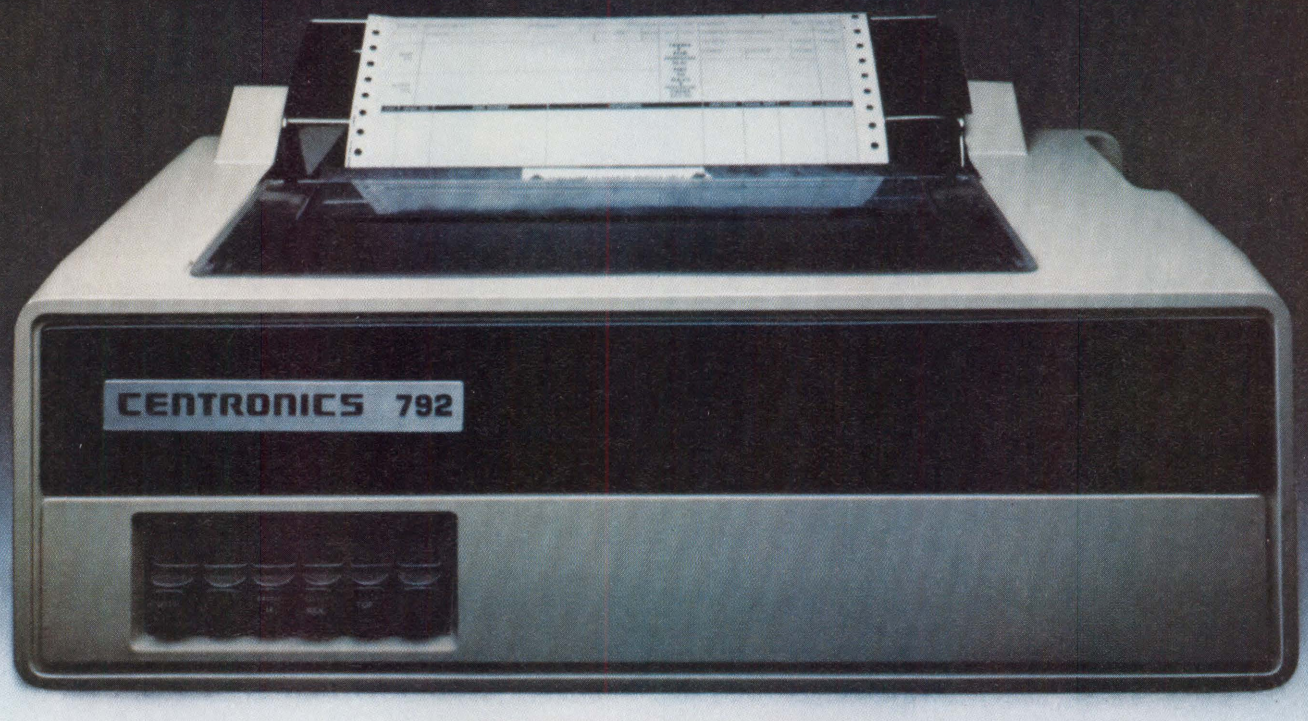
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CIRCLE 27 ON INQUIRY CARD

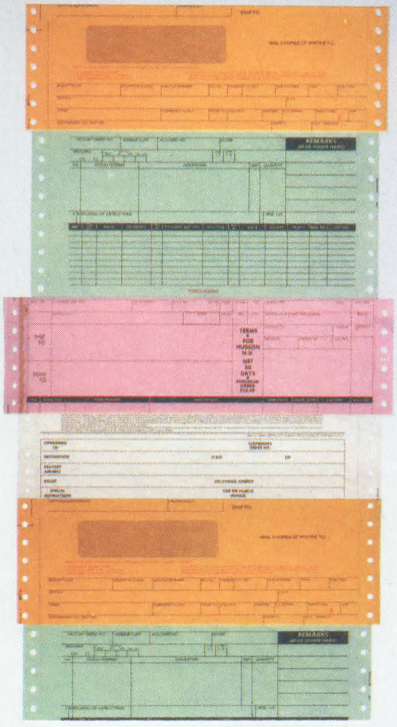
DEMAND PERFORMANCE.



The Centronics 792. It's the only true demand document printer available today and the choice of OEM's and end-users with a critical need for high performance in multipart document applications. For example: Bills of lading. Hotel invoices. Car rental contracts. Purchase Order and Work Order forms. Ticketing. And here's why no competitive printer can match it.

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CENTRONICS® PRINTERS

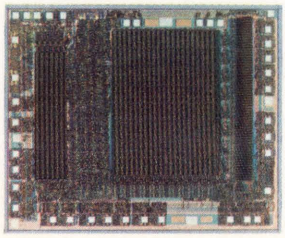
Centronics Data Computer Corp.
One Wall Street, Hudson, New Hampshire 03051
Tel. (603) 883-0111

CIRCLE 28 ON INQUIRY CARD

8-Bit Microcomputer Benchmarks

Processor	TMS7000	Z8	8051	6801
Clock Rate (MHz)	8	8	12	4
Binary Addition (μs)	4	3	6	13
BCD Addition (μs)	6	12	12	22
Block Move (μs)	1112	1785	3307	4584
Table Search (μs)	283	544	326	645
Binary to BCD (μs)	184	236	229	650
BCD to Binary (μs)	55	63	46	130
Bit I/O (μs)	13	15	10	33
Total (μs)	1657	2658	3936	6077
Relative Performance	1.00	0.62	0.42	0.27





Setting new VLSI standards in cost, performance, and flexibility with unique chip design and rich instruction set . . .

TMS7000

TI's new 8-bit microcomputer family. Best benchmarks in the business. And it costs less, too.

TMS7000. The newest, most cost-effective system solution for 8-bit microcomputer applications. Applications like computer peripherals, telecommunications, industrial control, automotive, appliances, toys and games and more. Here's how:

High speed

Check the benchmark comparison of the TMS7000 vs. competitive 8-bit microcomputers. See how the powerful instruction set, variety of addressing modes, and unique architecture maximize throughput while minimizing memory requirements. Containing the usual byte-oriented instructions, the TMS7000 instruction set also offers multiplication, double precision arithmetic, single and multiple bit testing, as well as BCD arithmetic.

Chip design innovation

At the very heart of our 8-bit chip is TI's newly developed Strip Chip Architecture Topology (SCAT). It's a unique memory-like array-structured chip, integrating architecture and layout. SCAT establishes separate, easily accessible control and data paths that interconnect the active elements without taking up valuable chip space.

Smaller chips ... lower costs

The significantly smaller chip size of the TMS7000 family means significantly lower costs. And lower prices. It also means a unique ability to add new family members quickly and easily — by simply inserting new areas on the chip for additional memory capacity or functions. For example: EPROM, CMOS, communications devices and more, are on the way right now.

Required Memory Space

Benchmark	TMS7000	Z8	8051	6801
Binary Addition	4	4	7	6
BCD Addition	5	14	14	14
Block Move	10	20	33	27
Table Search	11	17	20	14
Binary to BCD	16	19	23	30
BCD to Binary	47	82	50	66
Bit I/O	15	16	17	23
Total (Bytes)	108	172	164	180
Relative Efficiency	1.00	0.63	0.66	0.60

First microprogrammable 8-bit

Because SCAT replaces most of the random logic with a microprogrammable control ROM (CROM) which can be altered, the standard instruction set can be customized for those applications that require unique performance, memory or I/O features.

Affordable flexibility

The unique architecture of the TMS7000 family allows us to offer you features that cover a wide range of applications with ease and economy.

- Choice of on-chip ROM configurations; the 2K TMS7020; the 4K TMS7040; and the "ROMless" TMS7000. All with 128 bytes of RAM.
- Five memory expansion modes offer memory addressability to 64K for increased configuration flexibility. The 32 I/O pins may be traded-off for easy interface to a wide range of external memory or peripheral devices to satisfy a variety of user requirements.
- Nine addressing modes enhance the inherent flexibility of an already powerful instruction set.
- On-chip clock and prescaler with capture latch simplify real-time control.

And now, a word about support

AMPL* systems — hardware and software development tools that maximize software productivity for all TI microcomputers and microprocessors — also support the TMS7000 family and include real-time, in-circuit emulation.

An evaluation module to support software debug and system prototyping is also available. Customer training is offered on a regional basis through TI's Regional Technology Centers.

From the world's leader in microcomputers

With the introduction of the TMS7000 family, TI becomes the only manufacturer to offer 4, 8 and 16-bit single-chip microcomputer solutions for all your applications. And, TI has shipped over 60 million single-chip microcomputers, more than any other manufacturer.

First TMS7000 family product offerings are the NMOS TMS7000, TMS7020 and the TMS7040.

For price and delivery information about any new TMS7000 family member, or for a free brochure, contact the TI distributor or sales office nearest you. For more details, write to Texas Instruments Incorporated, P.O. Box 202129, Dallas, Texas 75220.

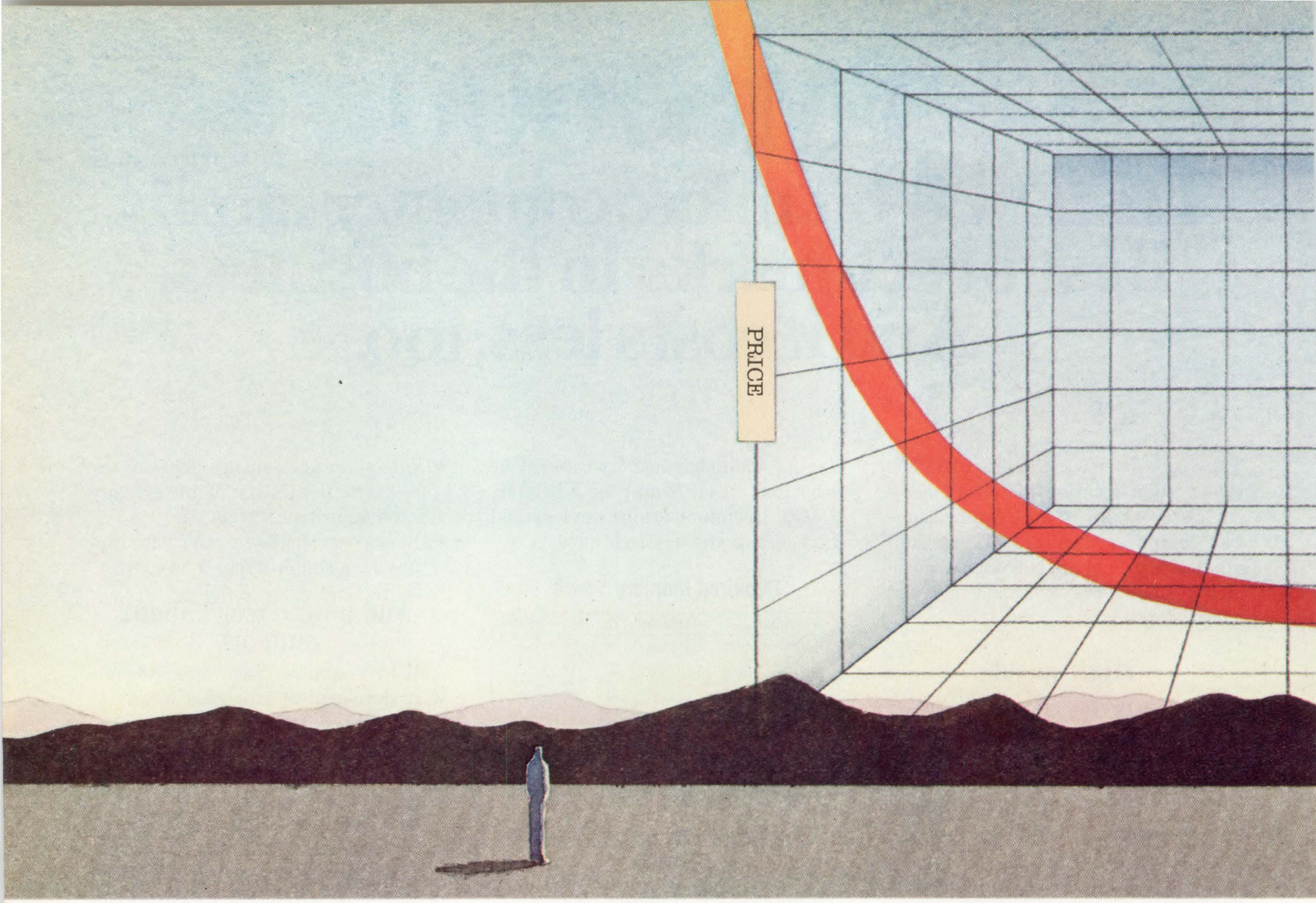
Texas Instruments invented the integrated circuit, microprocessor and microcomputer. Being first is our tradition.

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85683

CIRCLE 29 ON INQUIRY CARD



How to break the 8- without

It's not as hard as you think. Forget complex designs. And two-year waits.

All you do is get your hands on the Intel 8088.

And then leave the other 8-bit systems standing in your tracks. Without breaking the bank.

Because the 8088 gives you two to five times the performance of other 8-bit processors. For a whole lot less.

In fact, at $14.10 for 100 pieces, 75% less than last year. (Because high volume shipments are already pushing the 8088 down a super fast price curve.)

And about 20% less than you'd pay for a Z80 or MC6809 system.

For some simple reasons.

The 8088 runs at full speed with slower speed memories than you need for other 8-bit microprocessors.

And about 1/3 less memory at that. Thanks to its powerful instruction set that helps you reduce the size of assembly language programs.

Which together with the 8088's library of high level software (Pascal, CP/M, Basic and Fortran) should help you cut the other part of system costs. The part that's larger than hardware.

But even though you're paying less, you'll be getting more.

Like 1-megabyte addressing.

Extra power for 16-bit number crunching.

And faster string processing.

Fact is, our recent benchmarks show the 8088 runs circles around a Z80A, Z80B or MC6809 when it comes to terminal and small business applications.

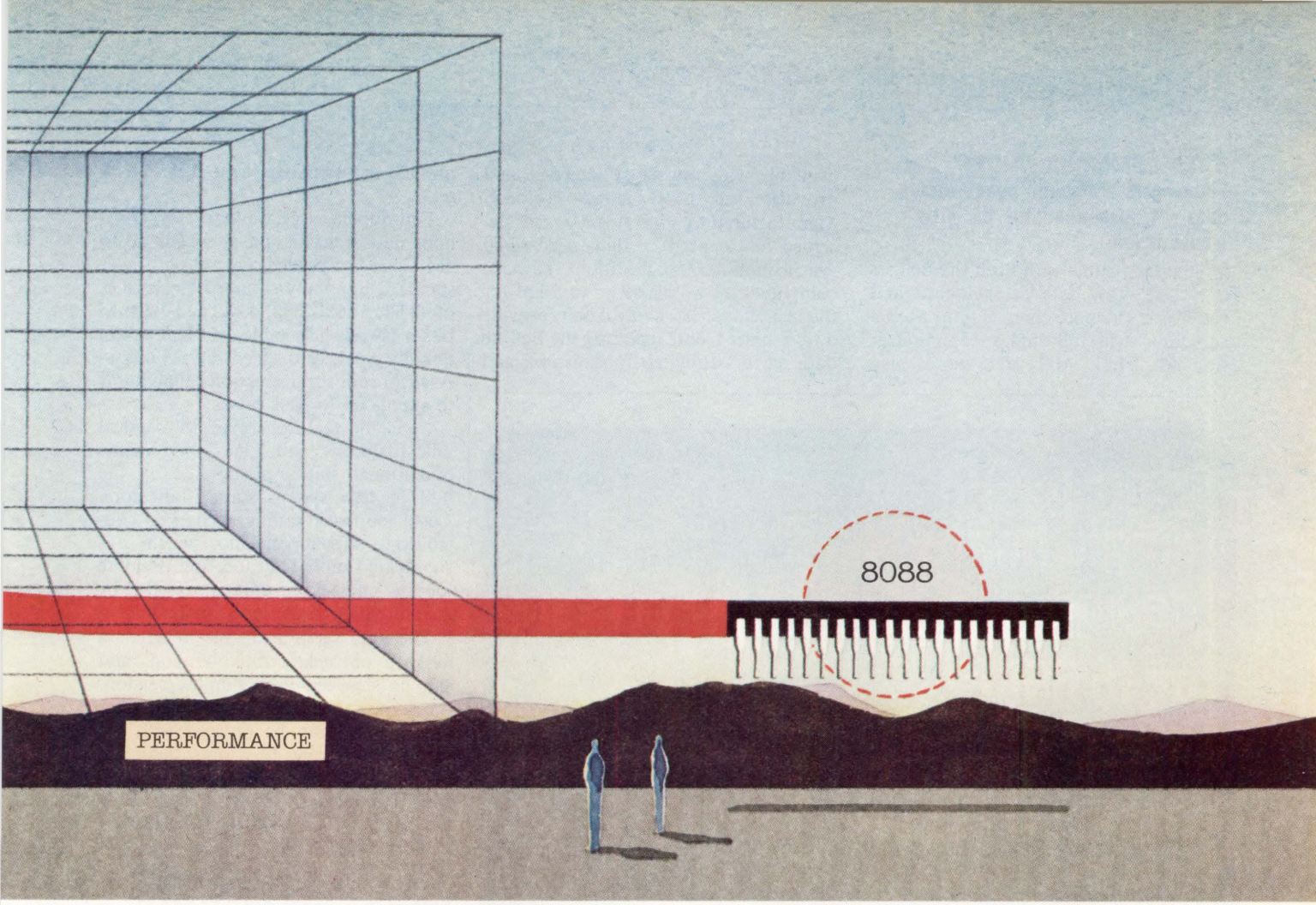
But don't think you have to stop there. With any of our iAPX 88 multiprocessor configurations, you can give performance an added boost—and still keep the cost and simplicity of an 8-bit system.

For 100 times the throughput on number crunching, just choose the iAPX 88/20 system.

Relative Performance

	Intel 8088 (5 MHz)	*Zilog Z80B (6 MHz)*	*Motorola MC6809 (2MHz)*
Computer Graphics	*1.0*	*0.1*	*0.05*
16-bit Multiply	*1.0*	*0.17*	*0.5*
Block Move	*1.0*	*0.75*	*0.49*

Full details of these benchmarks available in the iAPX 88 Book.



bit performance barrier going broke.

It combines the power of the 8088 with our 8087 numeric coprocessor.

Or if you're worried about getting bound up in I/O. Don't. Select our iAPX 88/11 system that speeds I/O processing three to five times by putting an 8088 together with an 8089 I/O processor.

Then there's the fact if you ever decide to make the jump to 16 bits, you won't have to jump. The 8088 is 100% software compatible with our 8086.

Because we don't think you should have to sell out your future to get the best deal on price/performance today.

And to put you in the right frame of mind, we're ready to make you an offer.

Just clip this coupon and send it with $5 to Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. (Or call 408-987-8080.)

We'll send you the book on how to design iAPX 88 systems and a coupon good for one free 8088.

Everything you need to start breaking through barriers—without going broke.

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intel® delivers solutions

CIRCLE 30 ON INQUIRY CARD

DATA COMMUNICATIONS

Fiber optic wideband synchronous data set accommodates 5M-bit/s transmission

Plug compatible with both the Bell 306 (CCITT V.35) data set standard and the IBM 3274 remote channel unit, Model ODS-306+ is a full-duplex communication set. The 5-MHz data set is also available with the RS-422 interface and provides full handshaking protocol. Manufactured by PHALO/O.S.D., it is designed to: be used in high speed serial synchronous communications between computers; be a link of up to 5 km for the IBM remote 3274 control unit; provide a fiber optic front, replacing the Bell 306 data set in T-1 digital transmission; and provide an alternative to the Bell 303 data set.

Full-duplex, serial-binary synchronous data transmission at speeds up to 5M bits/s is provided. Operation is over standard internally supplied clock rates of 40.8k, 57.6k, 230k, 460k, and 1.344 M bits/s (switch-selectable), as well as externally clocked to speeds of 5M bits/s. Asynchronous transmission capability is to speeds up to 300k bits/s.

Constant monitoring of the optical link (data set and fiber optic cable) operational status is supplied by the built-in LED system status indicators. Local loopback testing of data is controlled by a front panel loop switch, thus supplying simple fault location. Remote loopback testing of data is provided by enabling the remote loop command.

The data set is available in either a desktop or rackmounted version, and can be supplied in a simplex version, transmitter or receiver. A complete fiber optic system can be ordered with the data set, including fiber optic cable cut to length and terminated at each end with connectors. **PHALO/O.S.D.**, 9240 Deering Ave, Chatsworth, CA 91311.

Circle 247 on Inquiry Card

Software package permits VAX-11 access to U.K. public packet-switched networks

Latest product introduction in its Packetnet™ software program, VAX-11 PSI, from Digital Equipment Corp enables VAX-11 computer systems to communicate with other systems connected to the United Kingdom's PSS public packet-switched network. It is the first implementation of the X.25 packet-switched network protocol for this family of superminicomputers. VAX-11 computers running application programs under the VAX/VMS operating system can transmit data and control information between computers via VAX-11 PSI.

Implementation of the CCITT X.3, X.28, and X.29 recommendations by the software package allows terminals to communicate with VAX-11 computers. These recommendations define the packet assembly/disassembly (PAD) interface, terminal/PAD interface, and PAD/computer interface respectively. With X.29 implementation, packets of data can be converted into a form that terminals can accommodate, and data from terminals can be converted into packets. Implementation is embedded into the host VAX-11 system.

The software package supports X.25 V.24 at the hardware level, symmetric

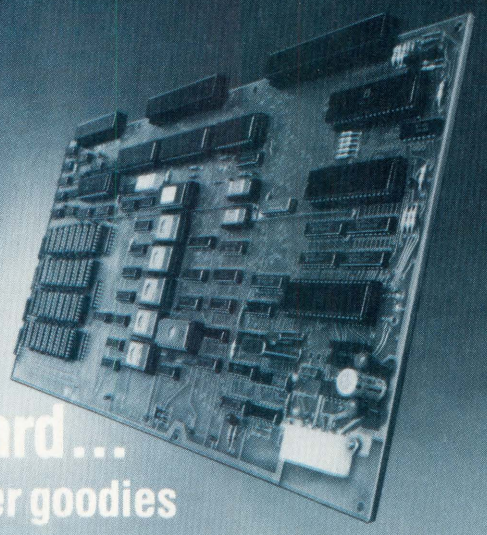
(continued on page 70)

Z-80 based single board design

up to 65Kb. of memory

DMA on board...

plus a lot of other goodies



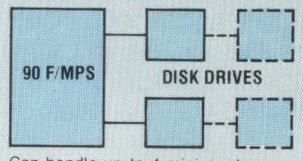
90 MPS
Single Board Computer

Feature for feature our 90MPS has the most sought after major system components available on any 8-bit computer, for increased profits and greater system reliability — including:

- Single board design
- *Z-80A microprocessor
- 4 MHz. operation
- Up to 65 Kb. dynamic memory
- DMA on board
- Up to 14Kb. uvePROM with programmer
- Selectable baud rates
- Up to 8-bit programmable I/O ports
- Up to three serial ports
- Powerful prom-resident system monitor
- **CP/M desk operating system optional

*Z-80A — registered trademark of Zilog, Inc.
**CP/M — registered trademark of Digital Research

with floppy disk storage . . .
DISK DRIVE EXPANSION



Can handle up to 4 mini or standard floppy disk drives

The **90 F/MPS** includes a multi-density floppy disk controller with DMA based disk access, data scanning and multi-track transfers.

all this technology and price too!

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CIRCLE 31 ON INQUIRY CARD

Wouldn't it be great if every kind of keyboard had our kind of performance?





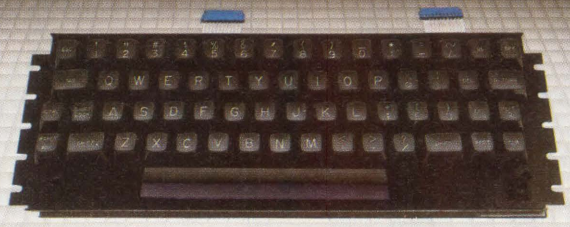
SC Series Capacitance Membrane Keyboard



KD Series Touch Panel Keyboard



SD Series Hall Effect Keyboard



CT Series Contact Membrane Keyboard

Now they do.

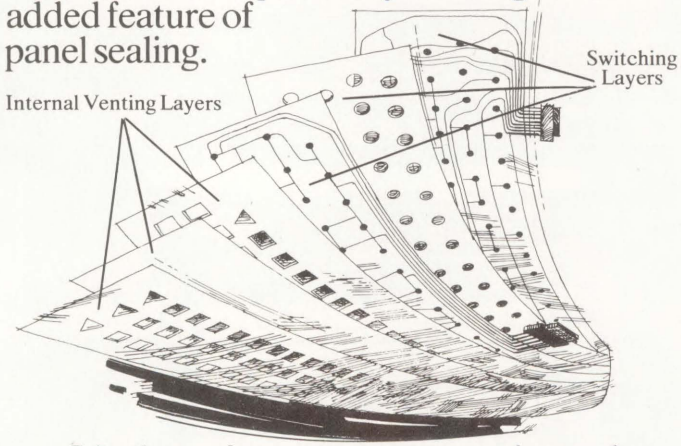
Until now, getting a keyboard at the price you needed could have meant giving up the kind of performance you wanted.

But not anymore.

Because, with the introduction of three new membrane keyboards, MICRO SWITCH has become the world's only full-line supplier of reliable keyboards. We offer a high-performance and cost-effective solution for virtually any application.

Now, in addition to our time-proven Hall effect offerings, you can specify MICRO SWITCH SC Series full-travel capacitance membrane or CT Series contact membrane keyboards, and KD Series touch panel membrane keyboards.

Whatever type of seal you need, all you have to do is ask. The capacitance membrane units are the world's only capacitance keyboards with all the benefits of membrane sealing. And we're the first to solve the venting problems associated with previous membrane designs. Both our capacitance membranes and contact membranes are internally vented to maintain their seal while preventing switch collapse due to air pressure or temperature changes. And for especially severe environments, the touch panel keyboards give the added feature of panel sealing.



It's those features, among others, that make these new keyboards more reliable than other capacitance and hard-contact designs.

And because all three new keyboards have been designed with traditional MICRO SWITCH quality and reliability, each carries a 1% Acceptable Quality Level and 2-year warranty.

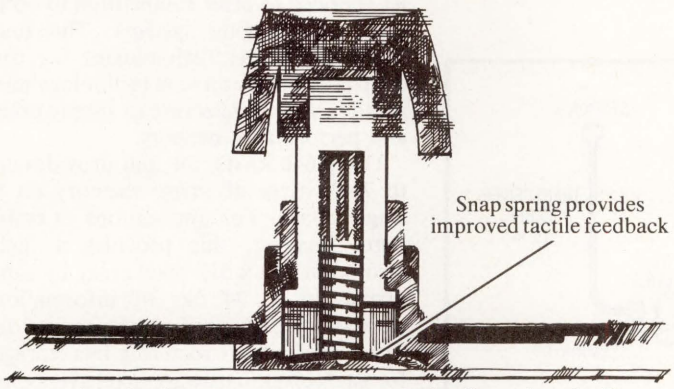
Now any combination of keyboard features you can name can have the MICRO SWITCH name on it.

Now your keyboard specifications are only limited by what you want. Not by what you can get.

Our full-travel series, for example, are available in a wide variety of keyboard configurations, with a choice of over 40,000 legends.

Because legends are screened on our touch panel designs, the graphic possibilities are endless. And, we can combine full-travel and touch panel actuation in a single assembly, featuring either capacitive or hard contact technology.

We make it easier to comply with European standards, because our full-travel membrane designs are available in low-profile versions to meet world requirements.



And, the actuator module for the full-travel membrane keyboards helps achieve new levels of tactile feedback and operator satisfaction.

So you can come to MICRO SWITCH for the keyboard technology, travel, actuation, sealing, appearance, profile, electronics, and special features you need.

And get them all – backed with the experience and full application support that's been a MICRO SWITCH tradition.

Being able to design a keyboard to fit any application is important. But doing it to fit any operator is imperative.

It's important to understand that half of any keyboard application is a human being. There's probably no keyboard manufacturer who understands that better than MICRO SWITCH.

Our unique human factors research – an intensive, on-going program for over 20 years – has given us the tools to develop industry standards for key speeds and multi-key rollover; tactile, visual, and audible feedback; and various keytop shapes, spacing, configurations and travel. We're continually improving the man/machine interface.

This human factors research is part of



what makes our keyboards unique. And it's part of every keyboard we make.

Instead of resting on our laurels, we're relying on our research.

Being able to add state-of-the-art capacitance membrane, contact membrane, and touch panel keyboard types to our Hall effect offerings is the result of extensive planning, research and testing.

But it's only the beginning.

Each of these keyboard types will be continually subjected to the refinements growing from our human factors research, customer feedback, and our unmatched R&D facilities which include backup by our Honeywell corporate facilities.

Also, every keyboard customer benefits from a manufacturing capability that stands unmatched: it's large enough to handle the most extensive order; responsive enough to give the modest order the same kind of intensive, individualized and quality-conscious attention.

All of these efforts are to make sure that, as your keyboard needs change and grow, you'll always have the choice of a progressive alternative with one unchanging feature: the MICRO SWITCH name. With all the performance that name implies.

For more information on our keyboard technologies, call 815-235-6600. Or write, MICRO SWITCH, the Keyboard Consultants, Freeport, IL 61032.

MICRO SWITCH
a Honeywell Division

CIRCLE 32 ON INQUIRY CARD

DATA COMMUNICATIONS

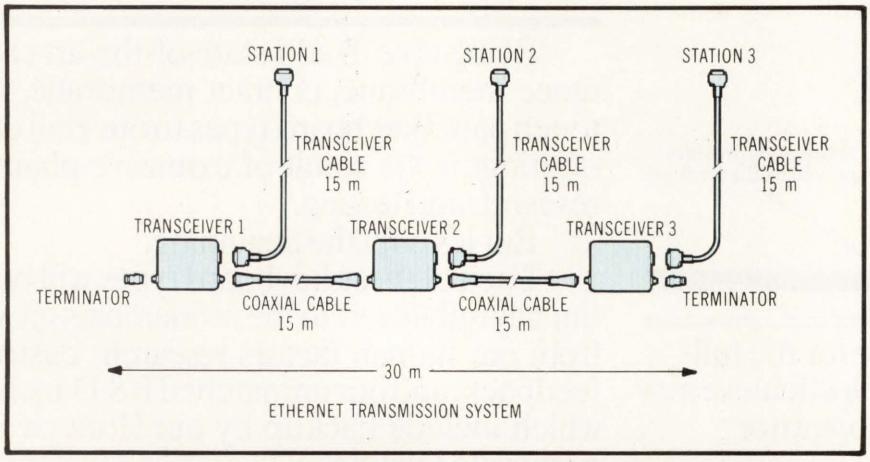
link access procedure B (LAPB) variant of the X.25 frame level protocol, and X.25 packet level protocol over 4-wire synchronous full-duplex lines at 2400, 4800, and 9600 bits/s. VAX-11 systems and other systems connected to the PSS network can communicate over both permanent virtual and switched virtual circuits (PVCs and SVCs).

X.25 user interface of the package allows programs that are written in a VAX-11 native language (MACRO, FORTRAN, or BASIC) to exchange data with programs in other systems on the PSS network. This user interface furnishes all X.25 protocol functions including setting up and clearing calls, sending and receiving data, sending interrupt messages, receiving unsolicited messages, error control, and status reporting.

The VAX-11 PSI software package is available through license at $5000. Packetnet is an ongoing program for providing X.25 products for the company's 16-, 32-, and 36-bit computer families. Currently available Packetnet Program software packages include products for Transpac (France) and Datapac (Canada). Additional products are being developed for Germany, the Netherlands, and the U.S. **Digital Equipment Corp,** Maynard, MA 01754.

Circle 248 on Inquiry Card

Starter package helps designers evaluate and implement Ethernet



Ethernet transceiver starter package. Three transceivers are connected by 2 sections of 50-Ω coaxial cable. Remaining 2 transceiver connectors are terminated by 50-Ω resistive terminators. Units are interfaced to their data link controller subsystems using three 15-m transceiver cables included with package

Ethernet™ transceiver starter package includes an exclusive designer's guide plus a set of three transceivers with required interconnect cables and terminators. The package, from 3Com Corp, also contains a summary of, as well as the full DEC/Intel/Xerox Ethernet specification. The aim of the product is to aid system designers in evaluating and implementing the Ethernet local computer network.

Design of the line driver/line receiver circuits that link the transceivers and controllers is discussed in the guide, as are other parts and functions of the Ethernet system. The shape of the 10M-bit/s waveforms as they propagate through the system are also described. The guide delineates important factors in each part of the network. According to a company spokesperson, the most important transceiver transmission factors are average dc level, symmetry, and rise time. Key factor in reception is the extent of phase jitter in the presence of noise and signal attenuation. A quick test procedure for determining the health of the network and its subsystems is also included as part of the documentation.

Each starter package contains three model 3C100 Ethernet transceivers. These units carry data between the data link controller and the 50-Ω network coaxial cable after specified transmission signal conversions. The transceivers meet or exceed the specifications set forth in Version 1.0 of the Ethernet document issued in Sept 1980. They are housed in rugged, electrically insulated enclosures that can be installed above ceilings, under raised floors, or in cable trays. The transceivers measure 5 x 4 x 1.5″ (12.7 x 10 x 3.8 cm).

The package also contains three 3C110 transceiver cables; two 15-m, 50-Ω, PVC-jacketed coaxial Ethernet cables; two 50-Ω terminators; the designer's guide, and specification documents and summary. The transceiver starter package is priced, for the U.S. only, at $2600 and is available immediately. **3Com Corp,** 1390 Shorebird Way, Mountain View, CA 94043.

Circle 249 on Inquiry Card

INTERFACE

Graphics controller offers dual mode image array selection

Offering users a choice between 512 x 512 and 1024 x 1024 resolution, the Model One raster scan graphics controller is priced to offer competition to both CAD and imaging systems. The first product of Raster Technologies, Inc, the controller builds on VLSI technology and an advanced architecture to supply price and performance benefits.

Using 64k RAMS, the unit provides up to 768k bytes of image memory on a single board. For applications in computer imaging, this provides a high resolution 512 x 512 pixel array by supplying up to 24 bits of information storage for each pixel on the screen. In those applications requiring less storage for each pixel, hardware pixel averaging gives users up to 6 bits of storage for each of 1024 x 1024 points.

While some other 512 x 512 systems can display a partial view, or window into a 1k image array, this machine offers full screen 1k x 1k array. According to Louis Doctor, president and co-founder of Raster, "The Model One is unique because it gives a window or an entire full screen 1k display on a standard video monitor." The unit can be switched via software commands from 512 x 512 to 1024 x 1024 addressable points. This dual mode image array selection permits users to perform both imaging and full screen line drawing tasks on the same display monitor.

Performance of the unit derives from a 16-bit Z8000 microprocessor used as the central processor; a high speed hardware vector processor serves to offload iterative line generation commands from the processor. Additional performance can be attained with the optional direct pixel memory access (DPMA) port that has bandwidth up to 3.75M bytes/s. Also optional is an overlay plane for alphanumeric data. Hardware pan and

(continued on page 72)



UNTIL NOW, LOCAL AREA NETWORKS WEREN'T REALLY A FACT. EVEN IN FANTASY.

Local area networking is an idea whose time has come. Almost. Massive investments of time and talent have created the concept – and the cable – to connect the network's stations. But so far only lip service has been paid to the interconnection of incompatible devices.

Some companies seem to believe the problem will eventually solve itself. Others feel that by ignoring it, it may go away. Still other companies, motivated largely by self-interest, have set out to create proprietary networking systems.

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Interlan is a new company that believes local area networking is not just desirable, it's inevitable.

That's why we have produced the hardware and software technology needed to connect almost any make of computer to today's networks. And we're already developing the equipment to make full use of tomorrow's networks.

For OEM's, Interlan means that compatibility – and more value – can be built directly into products, simply and inexpensively.

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At Interlan, we see the growth of networking as a tremendous business opportunity. But we also see it as our responsibility to turn tomorrow's ideas into hardworking realities. And we will.

To find out how Interlan can make local area networking a reality for you today, call or write.

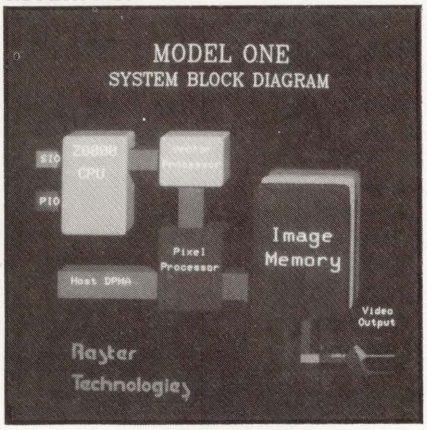
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CIRCLE 33 ON INQUIRY CARD

INTERFACE



Raster scan graphics controller. Using 64k RAMs, Raster Technologies' Model One controller can stuff 786k bytes of image memory on single board, and can switch resolution from 24 to 6 bits/pixel on software command. High speed hardware vector processor offloads iterative line generation commands from Z8000 central processor

zoom functions (1X, 2X, 4X, and 8X) are standard. Interactive devices supported include crosshairs, digitizer, joystick, function buttons, and trackball.

The unit offers a command set with high level software interfaces to user application programs in FORTRAN. Because the controller connects to the user's alphanumeric terminal and responds to calls from user application programs, training is simplified.

Addition of applications is eased by software development and diagnostic aids provided within the system. Debugging is facilitated by a command stream translator that tells the user exactly what commands are being transmitted to the controller from the host. Another aid—instant replay—is a diagnostic mode that analyzes commands that have been erroneously executed.

In its basic tabletop configuration, the controller connects to an existing system as an interactive or output-only device. The unit supports (and is available with) popular display monitors and other graphics peripherals. Single unit prices start at $10,800, with OEM discounts available. **Raster Technologies, Inc**, 110 Eighth St, Troy, NY 12181.

Circle 250 on Inquiry Card

Analog output interface provides 488 bus control

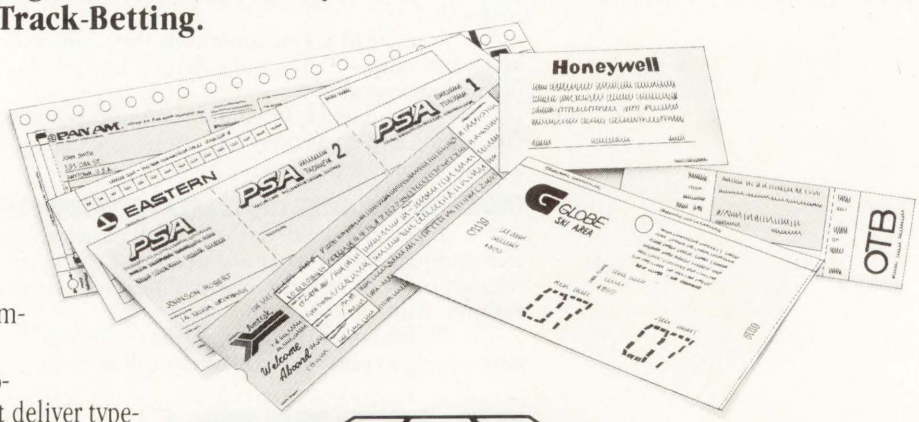
Model 4871 is a general purpose coupler that provides IEEE 488 bus control of analog devices. The device, manufactured by ICS Electronics Corp, can operate as a listener or a talker. Most functions are software programmable. There are four analog output channels with two more as options and three separate, user-selectable output signal ranges available per channel: 0 to 10 V, −10 to 10 V, or −4 to −20 mA. The analog output channels are isolated from the IEEE 488 bus as well as from the 4871's internal logic. This structure provides a low noise environment for system applications. The device functions are shown in the Figure.

Besides a self-test upon turn on, the device features three modes of automatic calibration. The Internal Auto-Cal mode provides zero and full-scale calibration of the dc output of each analog channel. The onboard microcomputer automatically computes and stores the required offset and scale factors to provide the correct zero and

(continued on page 76)

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CIRCLE 34 ON INQUIRY CARD

X.25

WHAT CAN IT DO FOR YOU? SEND FOR OUR BOOK AND FIND OUT.

DCA can now support X.25 through our powerful new master network processor, the System 355. This means that the 355 not only gives you packet-switching capabilities, it gives you *the industry's least expensive X.25 gateway.*

To get the complete story, send for our book *An Introduction to X.25 Gateway.* Here's part of what you'll find out:

DCA's X.25 support can lower your communications costs:

1. *By giving you low-cost access to public packet-switched networks.* This means that your network can talk to national and international packet-switched networks such as Tymnet, Telenet and Datapac, greatly reducing your modem, telephone connections and host port costs.

2. *By letting many users communicate inexpensively with a packet-mode host computer.* One 355 with an X.25 interface can be used to link up to any host computer with X.25 capabilities. Instead of having one cable, one mux port and one host port per user, many users can share one cable and one DCA X.25 interface.

3. *By letting you use a public network to access remote areas while still using a cost-effective private network for the bulk of your data.* This means you can communicate with areas that have only a few users per location without purchasing additional expensive hardware. The public network can also be used as backup for the private network.

The X.25 interface gives you the capability to use a public packet-switched network for those few times you may need to access remote areas.
You can access the public network over one physical link, and greatly reduce the number of lines, modems and host ports you would otherwise need.

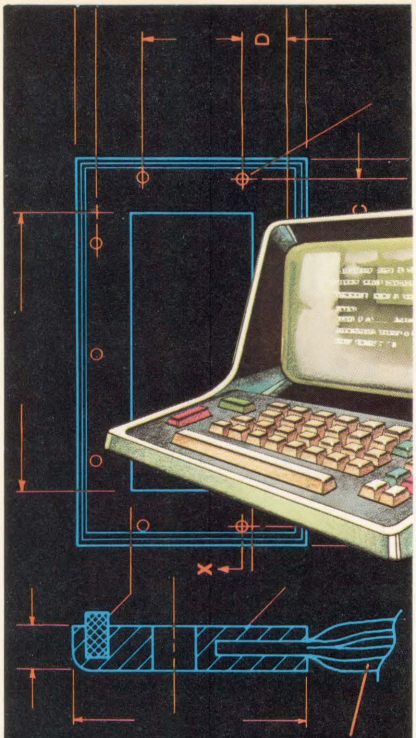
DCA meets Levels 1, 2 and 3 for X.25, and allows non-packet mode terminals to access the X.25 link.

If you already know the benefits of X.25, here's what you need to know about DCA. We meet all the CCITT specifications for levels 1, 2 and 3, obeying standards for X.3, X.28 and X.29. Plus, less intelligent terminals which do not operate in the packet mode can use X.25 through the mediation of the X.3 packet assembler/disassembler (PAD).

If you're interested in lowering your communications costs and providing optimum network growth at minimum expense, learn more about the System 355 and X.25, the trend for the 80's in data communications. The System 355 and other DCA products are part of our concept of INA, Integrated Network Architecture (INA). INA is our way of expanding your network with all our modular and compatible data communications "building blocks."

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Our EMC air panels cool interference without heating up the processor.

When the cooling ports on a word processor were emitting electromagnetic interference (EMI), Spectrum Control, Inc. was called in. Spectrum is a full-service company that provides professional electromagnetic compatibility (EMC) testing, consulting, design and manufacturing. Our experts solved this problem with shielded air cooling and filtration panels*, cooling the word processor with dust-free air while eliminating interference.

Spectrum also designs and manufactures EMI/RFI suppression filters, capacitors, shielded viewing windows, gaskets and many other custom and standard EMC control devices. Our computer database contains over 57,000 product variations to help us solve any EMC problem you may have at any stage of your system's development. And our testing facilities include a completely equipped Anechoic Chamber and open field sites.**

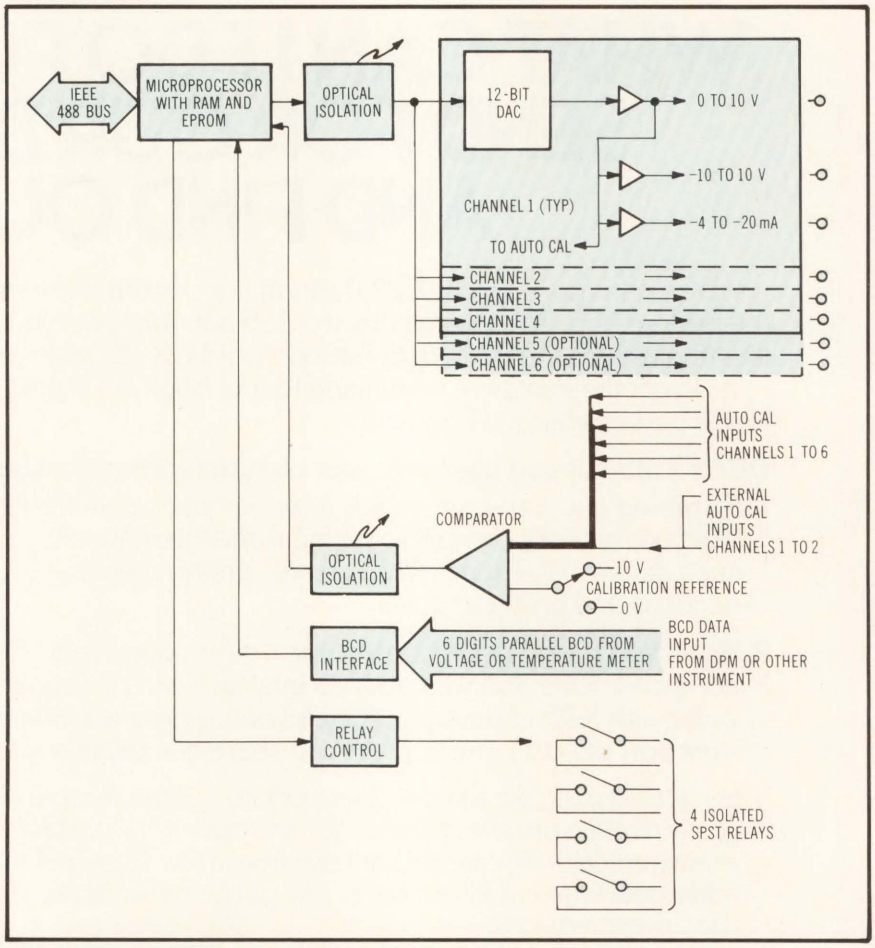
So contact us about your EMI problems. Write: Spectrum Control, Inc., 8061 Avonia Rd., Fairview, PA 16415. Or call: 814-474-1571.

*See Engineering Bulletin 27-0027-39 (part # 57-3038-20507-57). **Spectrum's testing facilities meet all FCC, VDE, CISPR, CSA and MIL-STD 461 A/B requirements.

SPECTRUM CONTROL INC.

Making technology compatible with technology.

INTERFACE



Functional block diagram of 4871 analog output interface. General purpose coupler device provides IEEE 488 bus controlled dc analog outputs

full-scale values. These factors, applied to the desired value as programmed from the system bus controller, cause the 4871 to generate the correct analog output value. Internal Auto-Cal is performed automatically at turn on.

The second mode of automatic calibration, External Auto-Cal, works like the first mode, except that the desired value is read at the output of the externally connected device that generates it. Thus, both the external device and the 4871 are automatically compensated for any offset and full-scale errors that may exist. This mode is software selectable, and is available only in channels 1 and 2.

In the third mode, called Software Auto-Cal, automatic calibration offset and scale factor values are sent to the 4871 from the bus controller; they enter an equation in the form of $Y = MX + B$, where B and M are the offset and scale factor values, respectively, X is a programmed value, and Y is the required output parameter. For example, assume that a frequency output of 10,000 Hz is generated for a 9.5-V input and a frequency output of 0 exists at 0.15-V input. By programming scale factor (M) to 0.935 and offset (B) to 0.15, the frequency will go from 0 to 10,000 Hz as the input is programmed from 0 to 10.00 V, greatly simplifying programming.

The coupler can be used to interface power supplies, X-Y plotters, and strip/chart recorders to the IEEE 488 bus. Four auxiliary relays provide on/off control for plotter pen positioning, chart recorder motors, and power control for auxiliary devices powered from the bus. **ICS Electronics Corp**, 1620 Zanker Rd, San Jose, CA 95112.

Circle 251 on Inquiry Card

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At $1990* in quantity one, Digi-Data's Model 2516 KSR 200 cps printer terminal is the best buy in the business. Our closest rival offers 25% less printing speed for almost 20% higher cost. And the rest are even further behind.

Digi-Data's clean design has produced a smaller unit that weighs less and uses less power. And the 2516's four modular assemblies deliver long term reliability through design simplicity. For Read-Only applications, our Model 2511 gives you the same printing performance without the keyboard at a quantity one price of $1550.

Digi-Data's record of computer peripheral value leadership began with our extensive line of reel-to-reel mag tape drives and related formatting and interface electronics. Now we offer cartridge tape drives too. And we've still got the best OEM prices in the industry.

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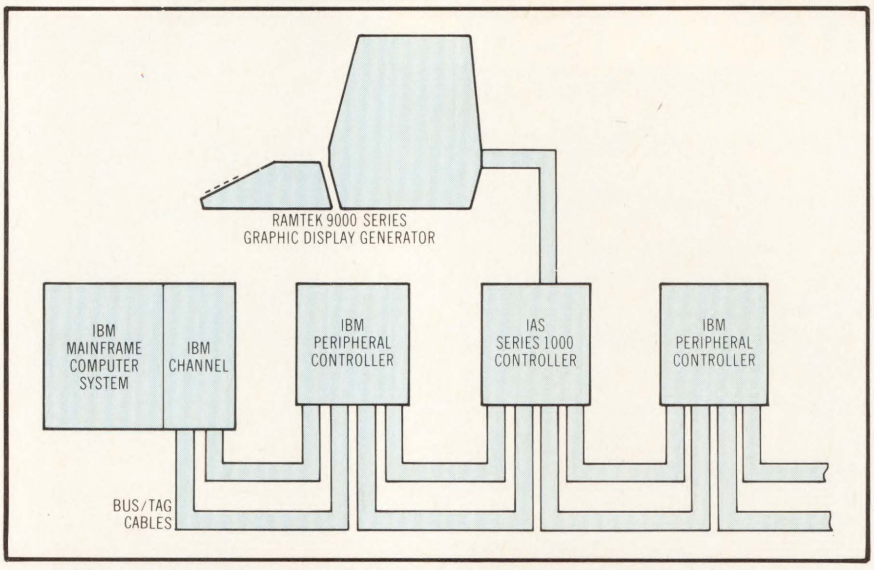
CIRCLE 36 ON INQUIRY CARD

INTERFACE

Online controller interfaces Ramtek 9000 to IBM mainframes

International Applied Systems, Inc, recently announced a color graphic display system for IBM mainframe computers. The system consists of an IAS model 1010 IBM online controller, a Ramtek 9000 series graphic display generator, and an optional INTAGRAF™ and ANSI/SIGGRAPH core compatible graphics package. The controller provides direct online capability for operating Ramtek 9000 series color graphics display systems with IBM 360/370/4300/3000 series computers. Operating on the IBM block multiplexer, byte multiplexer, or selector channel, it communicates in burst, forced-burst, or byte multiplex mode. It is designed to emulate the IBM 3250 graphics display system, but includes extended capabilities to support the color raster display features available with the Ramtek display systems. Accessories supported include alphanumeric keyboard, lightpen, and graphics tablet.

With a Ramtek 9000 series display, the IAS 1010 is upward compatible from IBM 3250 channel sequences and display buffer programs. While the company's system offers increased performance and extended features, new functions have been incorporated by expanding the original IBM protocols. Thus, existing IBM 3250 system software and application programs can operate with little or no modification. The controller is shown attached to an IBM channel in the Figure.

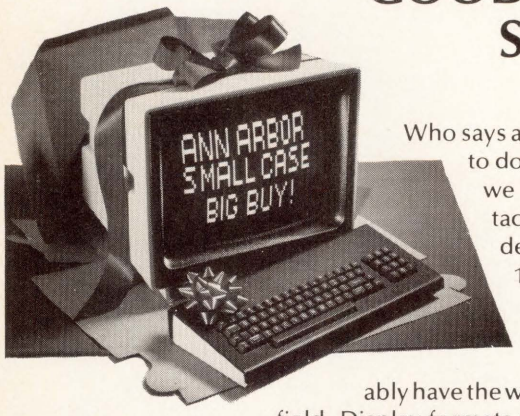


IAS model 1010 IBM online controller attachment. Device emulates IBM 3250 and supports Ramtek 9000 series color graphic displays. Device compatibility is provided by IBM 3250 software and system protocols

The INTAGRAF software provides a device independent graphics system for users wishing to develop their own application programs based on the ANSI/SIGGRAPH standards. It consists of a set of FORTRAN callable subroutines that can be used to develop interactive color graphic application programs. **International Applied Systems, Inc**, 831-H Sierra Vista Ave, Mountain View, CA 94043.

Circle 252 on Inquiry Card

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Who says a CRT terminal has to be big and bulky to do a good job? At Ann Arbor Terminals, we offer a full 15-inch screen *and* detached keyboard as standard on all our desktop terminals. And the case is only 14" wide by 15" high by 13.6" deep. We're known throughout the industry for our high quality and reliability. On top of this, we probably have the widest range of available options in the field. Display formats from 256 to 4800 characters. Foreign language character sets. Special command sets. Custom keyboards. Editing, protected fields and block transmit.

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Tel: (313)663-8000. TWX: 810-223-6033.

ANN ARBOR TERMINALS INC

Raster translator allows 200-point/in plotter to process 100-point/in data

Versatec, a Xerox Co, recently announced a raster data translator that enables 200-point/in printer plotters to draw with 100-point/in resolution data. The system provides faster plotting and a savings in data handling, and can also double the size of a plot. Data translator operates with all of the company's 200-point/in printer/plotters in paper widths of 11, 22, 24, 36, 42, and 72" (28, 56, 61, 91, 107, 183 cm), and film widths of 22, 36, and 42" (56, 91, and 107 cm). It accepts parallel input and provides parallel output. The data translator may be placed on a desktop or mounted in a standard 19" (48-cm) RETMA rack.

When switched to translate mode, incoming raster data are doubled horizontally and vertically in hardware. A smoothing hardware algorithm circuit smoothes duplicated data by adding points to jagged lines. Three buffers

(continued on page 80)

CIRCLE 37 ON INQUIRY CARD

DIGI-DATA SERIES 40

the more OEMs demand of tape systems, the more we deliver.

OEMs are demanding. They want different models for different applications, the highest possible reliability, and value that reflects in their final product. Our Series 40 continues the 17 year Digi-Data tradition of satisfying these OEM requirements.

More Selection

Within our Series 40 family, they can choose from 192 combinations of NRZI, PE and NRZI/PE models with reel sizes from 7 to 10.5 inches and speeds from 12.5 to 75 ips — all featuring a new control block with more functions, such as a density select switch and an optional unit select switch.

More Reliability in a Simpler Package

Microprocessor controlled imbedded formatter improves reliability by reducing chip count as much as 50%. All versions occupy a single board, simplifying cabling and reducing spares requirements, while eliminating the need for separate outrigger housings. Improved transport modularity facilitates field upgrading, particularly data density and tape speed.

More Value

Our low inertia tension arm design provides gentle tape handling that ensures data reliability without the cost, complexity or maintenance problems of vacuum columns. Advanced transport packaging includes a metal frame door and self-aligning rack mounting.

OEMs who interface the PDP-11, Nova, Eclipse or HP-21MX can specify Digi-Data's complete microcomputer based tape systems at a cost savings of 20 to 50%.

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store up to 1024 plot bytes of data. Print data are passed through transparently. I/O port configuration blocks may be switched for TTL or long line I/O.

Raster data translation is useful in seismic, mapping, multiterminal CAD, and remote systems. When plotting complex seismic trace data or maps, reduced data handling requirements and faster plotting speed offset the loss in resolution. In multiterminal CAD systems, lower resolution data can prevent contention problems.

The device can also be used to enlarge small plots that are drawn on a wide plotter. For example, an 11″ (28-cm) wide plot drawn on a V-80 printer/plotter can be translated to a 22″ (56-cm) width when plotted on Versatec 22, 24, 36, 42, or 72″ (56, 61, 91, 107, or 183-cm) wide plotters. This allows use of a narrow format plotter for quick look proofs while reserving the wider plotter for final plots. **Versatec, a Xerox Co**, 2805 Bowers Ave, Santa Clara, CA 95051.

Circle 253 on Inquiry Card



There are other streamers, but the Microstreamer™ gives you completely automatic tape loading.

There's one tape drive family you can buy that totally eliminates the manual handling of tape. With Cipher's Microstreamer, loading and threading of tape reels is totally automatic. All you do is open the door, insert the tape reel and close the door. That's it. The machine threads the tape by itself. No more operator training. Anyone can use it.

That's exciting, but there's more.

In addition to offering you exclusive auto-load features, the Microstreamers also give you these exclusive benefits:

- ☐ choice of 1600 or 1600/3200 selectable recording density
- ☐ higher 25 ips speed for start/stop use
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Catch the excitement!

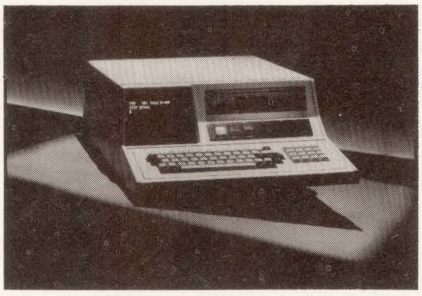
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DEVELOPMENT SYSTEMS

Instrument speeds firmware integration for mixed bit slice/ microprocessor systems



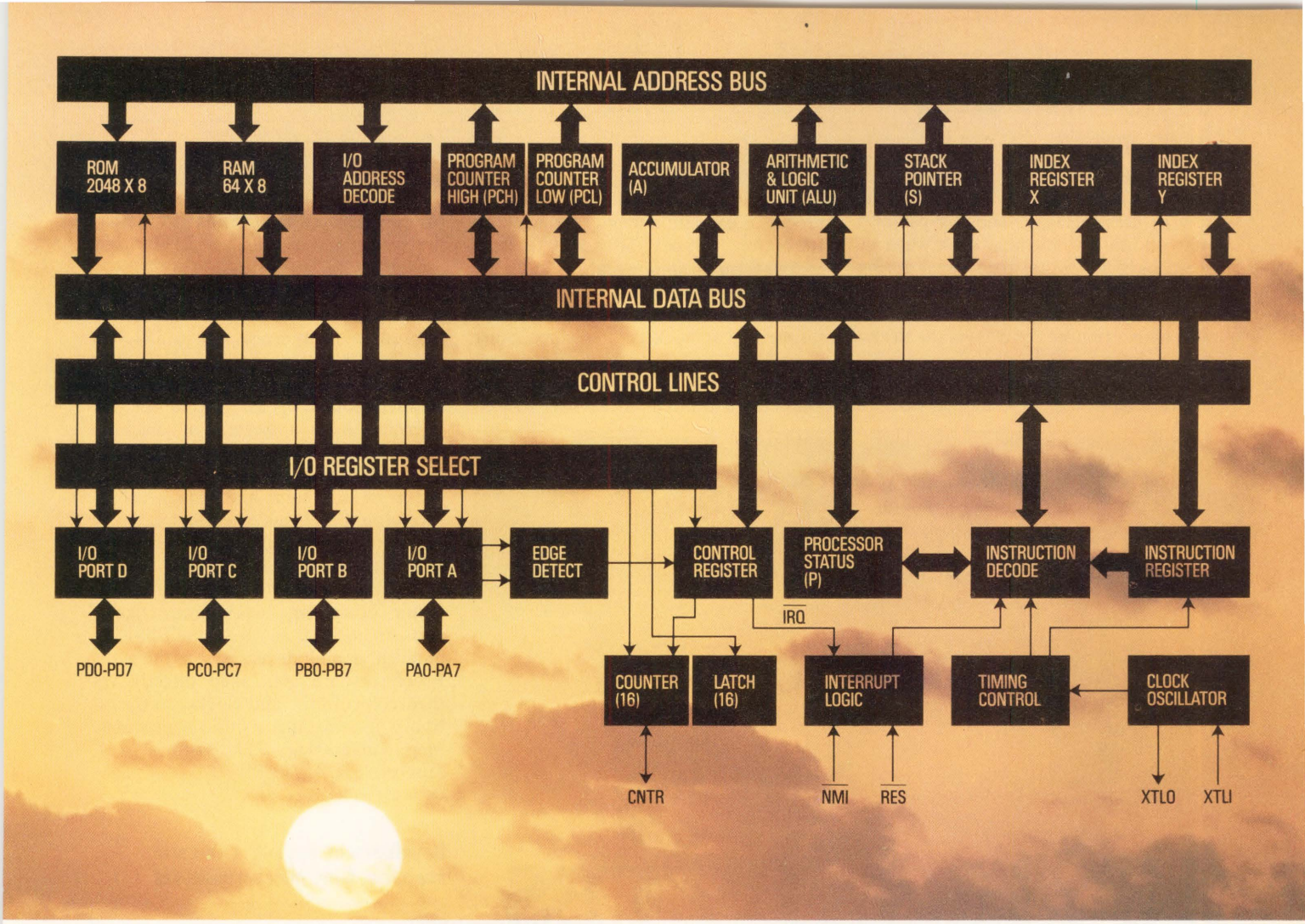
Designed for firmware testing and integration of single- or multiprocessor systems that use microprocessors and bit slice processors, the STEP-4 by Step Engineering uses ROM simulation to eliminate the need for personality modules when selecting different microprocessors. Thus, the same instrument can support all 4-, 8-, and 16-bit microprocessors, as well as bit slice processors without hardware changes. STEP-4 can also simultaneously debug both processors in a bit slice/microprocessor system.

In a mixed system, each processor has its own memory and is controlled separately from STEP-4's front panel. The TRACE option, which captures 250 words by 32 or 80 bits synchronously with respect to system clocks or strobes, is also independent for each processor. Processors can have separate trigger equations or inputs. Inputs and outputs of both processors can be cross-wired for input to either or both trigger equations, and data and commands passed between them can be monitored on both sides of the transfer.

The microprocessor capabilities of the MICRO 816 STEP-4 option are an extension of the STEP-3 bit slice techniques. By replacing ROMs in the target system with STEP-4 ROM simulation modules, and inserting a control module at high order addresses and to six common control signals, STEP-4 leaves the target system intact. MICRO 816 includes 64k bytes of memory that can be configured as 64k

(continued on page 82)

CIRCLE 39 ON INQUIRY CARD



The 6500/1 One-Chip Micro. First, look what it's got. Then, look what it costs.

$10.50 at 1,000. And there's more good news. No masking charge for the on-board 2K x 8 programmable ROM. And, the MOS 6500/1 is available in either 1MHz or 2MHz versions.

Here's what you get. A microcomputer on a chip. The 8-bit NMOS 6502 CPU, software compatible with your existing 6502 programs. Four I/O ports (32 bi-directional lines). One bi-directional counter line. On-board clock. 2048 x 8 ROM. 64 x 8 static RAM. Your choice of a 1MHz or a 2MHz internal clock. 16-bit programmable counter/latch with four modes. +5V supply. And more. All, on a 40-pin DIP. Plastic or ceramic.

Good old 6502. Simple to program. Familiar. Which means you write software in weeks. Instead of months. And, the 6500/1 is the microcomputer on a chip with software compatibility with its host CPU.

Prototyping? Simple. Build your prototype system with PROMs before committing to mask-programmed production. Our 64-pin prototyping part, the 6500/1E emulator includes all 6500/1 interface lines and brings all internal memory address, data and control lines off-chip. There's even a 40-pin configuration in piggy-back EPROM.

Delivery now. 1MHz or 2MHz. Take your pick. Develop your system, provide us with final ROM masking program and we'll have your 6500/1 μC's back to you in five weeks. And yes, there are second sources.

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TLX 730-969

Gentlemen, Please send me complete information on the MOS 6500/1 computer on a chip. ☐ Include data on your line of 6500 support chips.

Name _____

Address _____

City _____ State _____ Zip _____

CIRCLE 40 ON INQUIRY CARD

DEVELOPMENT SYSTEMS

8-bit words or as 32k 16-bit words by the user or user software. The user can also map and disable memory on a word by word basis from the front panel during setup, or from a host program using the computer control interface (CCI). CCI also allows remote control via the STEP-4 RS-232 links, which permits mapping around space reserved for target processor RAM or memory mapped I/O.

In addition to the 64k bytes of microprocessor emulation memory, the MICRO 816 option includes 750 words to store routines for examining and modifying processor and system states and registers. Because access to the system is through ROM sockets, LSI chips other than the processor, such as UARTS, CRT controllers, and I/O ports, can be examined and modified via user written X-STATE and M-STATE routines, thus expanding STEP-4's applications to the entire system rather than just to the processor.

For bit slice processors, two families of writable control stores (WCS) can be stacked to form words up to 192 bits wide and at depths up to 48k. Each WCS has its own address comparator for use as breakpoints or as triggers for the internal logic analyzers or external instruments. One-time execution of desired instructions can be accomplished by the FORCE command, which causes execution of the keyed instruction, or by the JAM command which executes the instruction at the keyed address.

For both types of processors, processor operation, breakpoint, trigger, and trace status are continuously monitored and displayed on the CRT. Processors are controlled directly via their control lines and clocks, so operation is in real time with no wait states. **Step Engineering,** 757 Pastoria Ave, Sunnyvale, CA 94088.

Circle 254 on Inquiry Card



20 MEGABYTES IN JUST 4 MINUTES

THAT'S PERFORMANCE! That's the Archive ***Sidewinder.*** It packs more formatted data—up to 20 Mbytes on a single 450 ft. ¼-inch cartridge—more than any other type of Winchester backup storage system. And with 97% tape efficiency.

The Sidewinder streaming tape drive transfers data at optimum speed, thanks to:

- **Designed-in compatibility with fast-access DMA I/O channels**
- **Ring buffering to insure constant tape motion**
- **Transfer rates up to 90 Kbytes per second**
- **90 or 30 IPS tape speeds**

AND AT THE RIGHT PRICE. The nice part is that you—and your ultimate customer—get all this unbeatable performance at the lowest possible cost of ownership. Lower than with any other type of backup system.

Check out the ***Sidewinder*** for yourself. Call Archive now for more details.

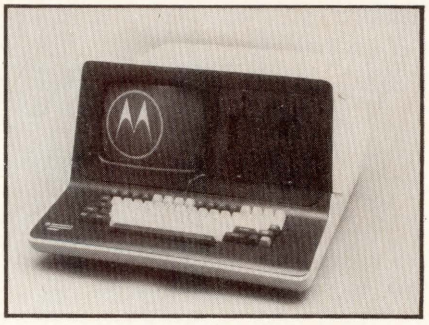
ARCHIVE CORPORATION
3540 Cadillac Avenue
Costa Mesa, CA 92626
(714) 641-0279
Telex 683466, TWX 910-565-2458

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Development system software supports 8-bit microprocessors



Upgraded development system. Additional software supports all of company's 8-bit microprocessors. System also has increased disc storage capacity and improved operating system

An upgrade of the original system introduced over a year ago by Motorola Semiconductor Products Inc, EXORset™ 30A now has software development support for all the company's 8-bit microprocessor families, including M6800, M6801, M6805, and M6809. Other changes include an increase in floppy disc storage capacity, and improvements in the disc operating system, text editor, and BASIC-M™ compiler. The system is designed to lower the costs involved in supporting software development. *(continued on page 84)*

Image processing systems
Modular graphic display systems
Frame buffers–Television monitors

Grinnell has them all, for almost any application: from simple black and white line drawing to full color image processing. Select a packaged system, or configure one "your way."

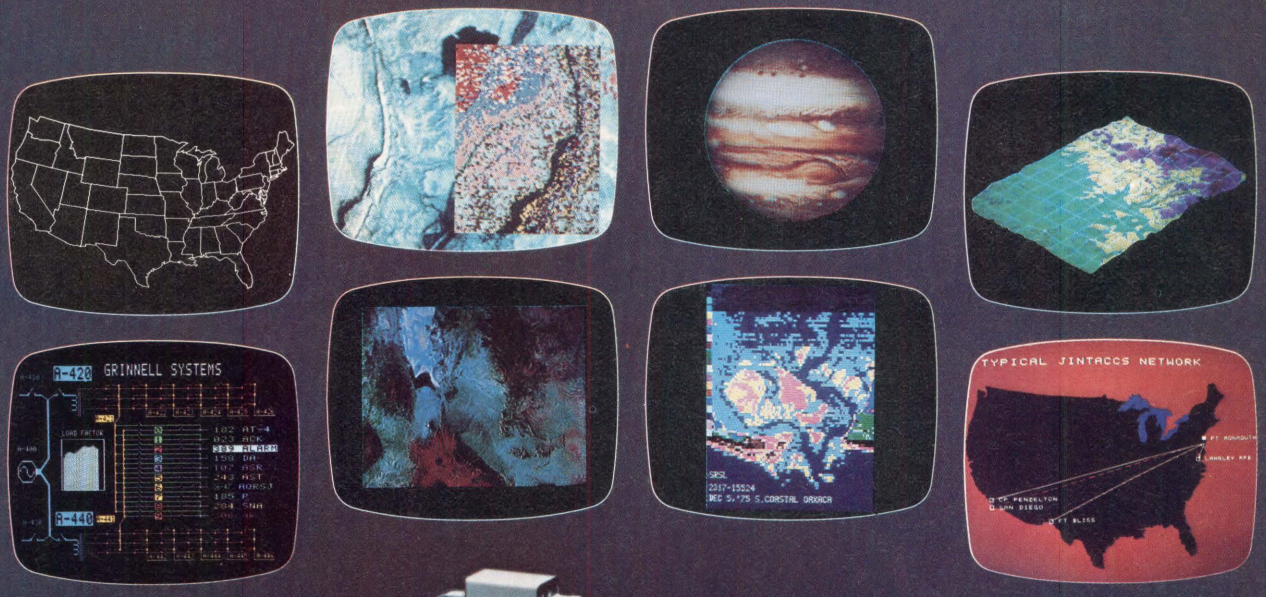
GMR 270 Series: **512 × 512 frame buffers and full color pipeline image processing systems.**

GMR 260 Series: **1024 × 1024 frame buffers for greyscale, black and white, pseudo color and full color.**

GMR 27 Series: **256 × 512 to 1024 × 1024 high speed, modular graphic and image display systems.**

All systems are available in both U.S. and European versions, with plug-compatible interfaces to most minicomputers (including DEC, Data General and PRIME). Proven system designs ensure reliability, and an expanded FORTRAN library and driver package makes operation easy.

So, whether you need a complete system, or just a card set to embed in a larger system, Grinnell has an optimum cost/performance solution. For complete specifications and/or a quotation, call or write today.





GRINNELL SYSTEMS

2159 Bering Drive, San Jose, California 95131 (408) 263-9920 TWX 910-338-2145

CIRCLE 42 ON INQUIRY CARD

DEVELOPMENT SYSTEMS

Man/machine interface consists of a full-size ASCII keyboard plus 16 user assigned function keys. The high resolution 9″ (23-cm) CRT can display 22 lines x 80 chars or 16 lines x 40 chars, and full 320- x 256-dot graphics. A standard Centronics-type parallel printer interface is provided.

Memory is 48k-byte RAM, expandable to 56k by using an optional 8k expansion kit. Twelve EPROM/ROM sockets accept up to 24k bytes of user supplied firmware. Dual double-sided mini-floppy disc drives furnish 328k-byte mass storage. All operations and file management are handled by the XDOS operating system.

A ROM-resident debug monitor package is standard with the system, as are the disc-resident, relocatable macro assemblers, CRT-oriented text editor, linking loader, extended BASIC-M interactive compiler, and self-diagnostic programs. A Pascal compiler producing M6809 object code is an available option.

Based on the new generation 16/8-bit MC6809, the system increases the efficiency of software execution with its expanded instruction set, addressing modes, and architecture. It allows such programming techniques as structured programming, position independent codes, reentrant routines, and realtime operations. These capabilities adapt the microprocessor to high level program development with an extended BASIC-M interactive compiler/interpreter.

Power requirement is 100 W at 100-130/200-250 Vac, 45-100 Hz. Dimensions are 25.2 x 11.0 x 18.3″ (64 x 28 x 46.5 cm) and weight is 49 lb (22 kg). The system is housed in a compact desktop cabinet.

The development system is priced at $6295. This includes the XDOS system diskette, latest version of XDOS software with disc-resident CRT editor, macro assemblers for MC6800/01/09/05, linking loader, and BASIC-M interactive compiler with runtime package. A complete set of hardware and software users' guides is also included.

For those who have the earlier model, software only may be upgraded with an XDOS diskette, available for $350. To upgrade both system hardware and software, an available modification provides new higher capacity disc drives plus changes to internal electronics in addition to the new software. This upgrade requires a return to the factory and costs $2000. **Motorola Semiconductor Products Inc**, PO Box 20912, Phoenix, AZ 85036. Circle 255 on Inquiry Card

Voice development system allows users to program digitized voice vocabularies in real time

Designed for the creation, editing, and management of voice files, the standalone VoiceWare Development System from Centigram Corp allows users to program their own chips in their own vocabularies. Quality voice can be produced at the rate of 4800 bits/s through the proprietary voice digitization method—parametric waveform coding (PWC). In PWC, parameters are calculated on an average of every 50 ms. The method takes advantage of pauses in words and of slowly changing sounds to compress the bit stream. The development system includes a LISA voice synthesizer, a voice digitizer with microphone and tape recorder input, a Multibus (Z80) or Unibus (LSI-11) based computer with dual 500k floppies, or a 500k-byte Winchester, 25-line x 80-character display, and CP/M based menu driven software. An optional MIKE voice recognition system and software package supports voice recognition applications. Touch-tone data entry and retrieval is also an option. The system components are shown in the Figure.

Development system information is organized in "messages." A message is a

(continued on page 86)

— ATC ANNOUNCES —

GRAPHICS 810

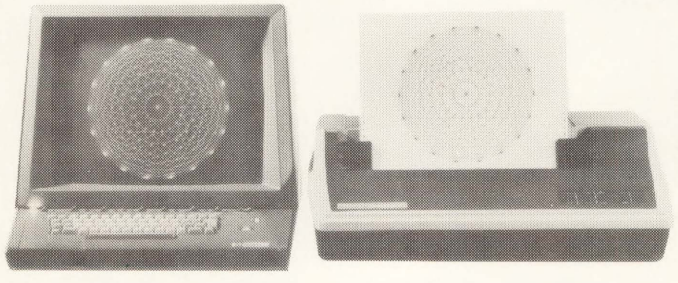
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FOR THE HIGHLY RELIABLE TI*-810 RO PRINTER

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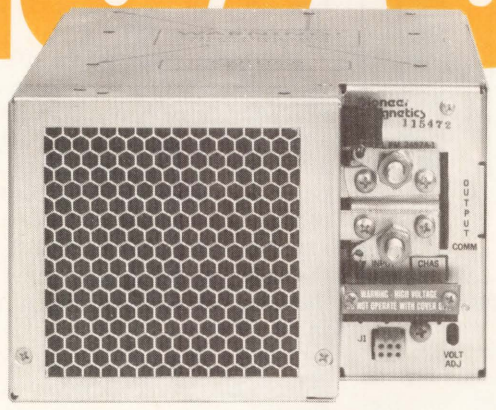
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*TEXAS INSTRUMENTS

CIRCLE 43 ON INQUIRY CARD

Dependable Switchers...

1973 1981



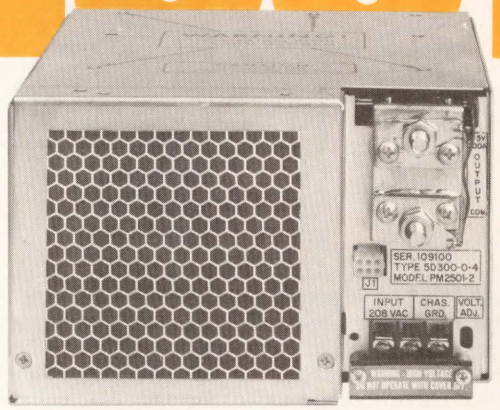
The PM2497
5V@100A/5″x8″x11″

In 1973 Pioneer Magnetics started building a 5VDC @ 100A switching power supply for applications requiring compact and efficient DC power. At the time, commercial switchers were considered state-of-the-art. We solved reliability and delivery problems for our customers that our contemporaries couldn't. As a result, our customers referred to the power supplies as the DEPENDABLES. In fact we're still delivering that same power supply to those same valued customers. We're proud to say that they've depended on us and we've responded by shipping over 100,000 high power switchers. After 8 years our supplies are still out there and running. A continuation of a tradition started in 1958.

STANDARD DC OUTPUT RATINGS.

MODEL	2V	3V	5V	12V	15V	18V	24V	28V	48V	60V	CASE SIZE
PM2496A	100A	60A	50A	30A	25A	22A	16A	13A	8A	6A	5″X8″X11″
PM2497A	200A	100A	100A 120A 150A	60A	50A	45A	33A	27A	16A	12A	5″X8″X11″
PM2500A		200A	200A	85A	70A	60A	45A	40A	24A	19A	5″X8″X11″
PM2498B	400A	300A	200A 300A	120A	100A	90A	66A	54A	32A	25A	5″X16″X11″
PM2501	400A	300A	300A	120A	100A	90A	66A	54A	32A	25A	5″X8″X11″
PM2502	500A	450A	450A	180A	150A	125A	90A	80A	47A	35A	5″X16″X11″

NOTES: 92-138VAC or 184-250VAC single phase, 47 to 63Hz.
DC input available.



The New PM2501
5V@300A/5″x8″x11″

Since 1973, we've been accepting new challenges. Within the same outline as the PM2497, we've developed output ratings of 5V @ 120A, 150A, 200A and now a new 5V @ 300, with full delivered power at 50°C.

The new PM2501 exhibits excellent dynamic response. Proven design concepts enable close control over those parameters that insure reliability. For instance, our unique heat transfer technology results in low component thermal stress, even lower than the PM2497. At three times the power level the PM2501 features an exceptionally high power density package.

Our product line includes switchers that deliver up to 2250 watts in single output and from 375 to 1500 watts in dual through quad output channels. AC or DC input.

Over 100,000 PMI switchers are in the field providing dependable, service free operation. After all, that's why customers have continuously come back to us since 1958.

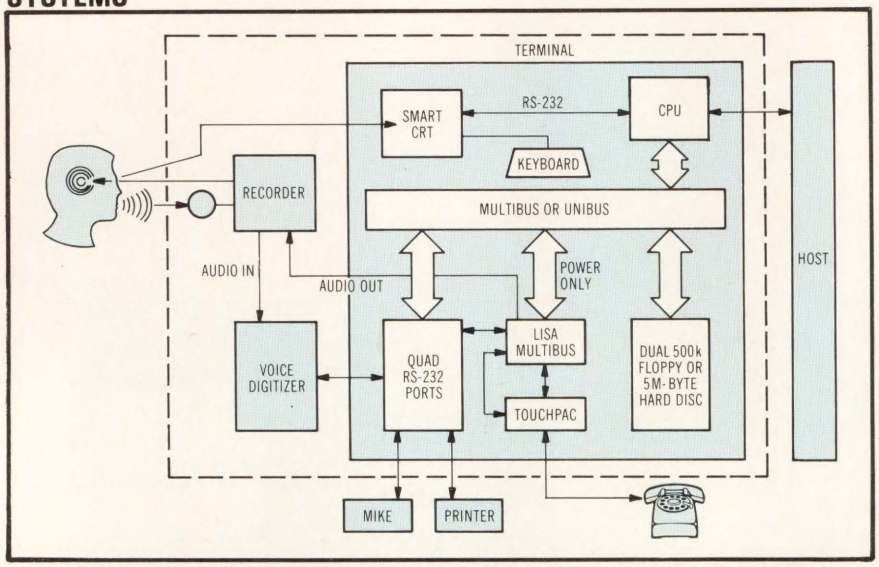
Pioneer Magnetics

THE SWITCHING POWER SUPPLY PEOPLE SINCE 1958

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CIRCLE 44 ON INQUIRY CARD

DEVELOPMENT SYSTEMS



Components of Centigram's VoiceWare development system. System provides realtime speech synthesis and recognition development

few seconds of speech. Each message has three parts: a tag, a descriptor and speech data. The tag is used to identify a message. The descriptor is similar to a software REM and is for the programmer's information. Speech data are the actual sound to be produced. Messages are grouped into libraries. Tags, descriptors, and speech data are saved in separate libraries. While the system is offline, the operator works from a script, speaking each phrase into the microphone. Voice is digitized and stored in the LISA unit's dynamic RAM. The phrase is then recalled for review and editing. Voice data will sound like a recording of the operator's voice. When the operator is satisfied with the phrase, it is assigned a speak code and loaded onto a disc for permanent storage. The host CPU uses the speak code to access the phrase from the disc.

The operator can test the effectiveness of the dialogue by selecting a mode in which the development system emulates a LISA unit alone or in conjunction with a terminal. In this mode, the host computer downloads the LISA load files as though the VoiceWare System were a LISA unit in field operation. After testing the dialogue, the host computer supplies the LISA load files directly to LISA units in the field.

User friendly system operating procedures are based as menus and help directives. With interactive guidance the user can add, delete, play, and update messages.

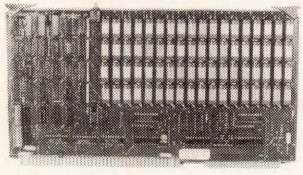
An optional MIKE unit is used to develop speech recognition data. Speech recognition is organized by 3-part "words." Each word has three parts: a tag, a descriptor, and a recognition pattern. MIKE words are also grouped into libraries.

A range of applications for voice is seen by the company, including database entry and inquiry, and computer aided instruction. For example, speech output can be added to a data entry system which informs clerks of an error or tells operators what information to enter next. In a computer aided training program, audio-visual instructions can be included. **Centigram Corp**, 155A Moffett Park Dr, Sunnyvale, CA 94086.

Circle 256 on Inquiry Card

TURN ON YOUR COMPUTER WITH A iMEMORY

WE'LL MAKE YOUR LSI, MOTOROLA AND MULTIBUS SYSTEMS WORK LIKE THEY NEVER WORKED BEFORE.

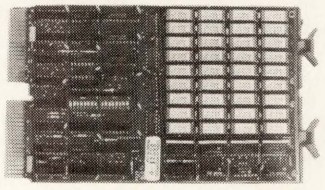


512KB SINGLE BOARD MULTIBUS® MEMORY
First to Offer 512KB on One Board

- Pin-to-pin MULTIBUS compatibility for both 8-bit and 16-bit systems.
- On-board parity with selectable interrupt on parity ERROR.
- Addressable as a contiguous block in 16K word increments up to 16 Mega Bytes.

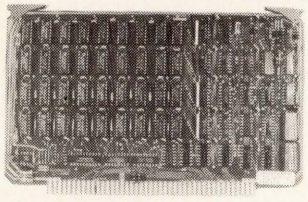
SINGLE QTY. PRICE: 128K x 9 $795. 512K x 9 $1,995.

256KB LSI 11/23® SINGLE DUAL WIDTH BOARD
First 256KB Memory on a Single Dual Board.



- Addressable as a contiguous block in 4K word increments through 4 Mega Bytes.
- On-board parity generator checker.
- Power requirements are +5V 1.2A.
- Battery back-up mode.

SINGLE QTY. PRICE: 128K x 18 $1,795.
SINGLE QTY. PRICE: 32K x 18 $575.



64KB EXORCISER I, II, and Rockwell System 65
Single Board Memory.

- Addressable as a contiguous block in 4K word increments with respect to VXA or VUA.
- Parity checker on board.
- Functions with on-board hidden refresh up to 1.5 meghz clock rates.
- Functions with cycle stealing refresh at 2 meghz clock rates.

SINGLE QTY. PRICE: 64K x 9 $575.

DON'T ASK WHY WE CHARGE SO LITTLE, ASK WHY THEY CHARGE SO MUCH.

Chrislin Industries, Inc.

31352 Via Colinas • Westlake Village, CA 91362 • 213-991-2254
TWX 910-494-1253 (CHRISLIN WKVG)

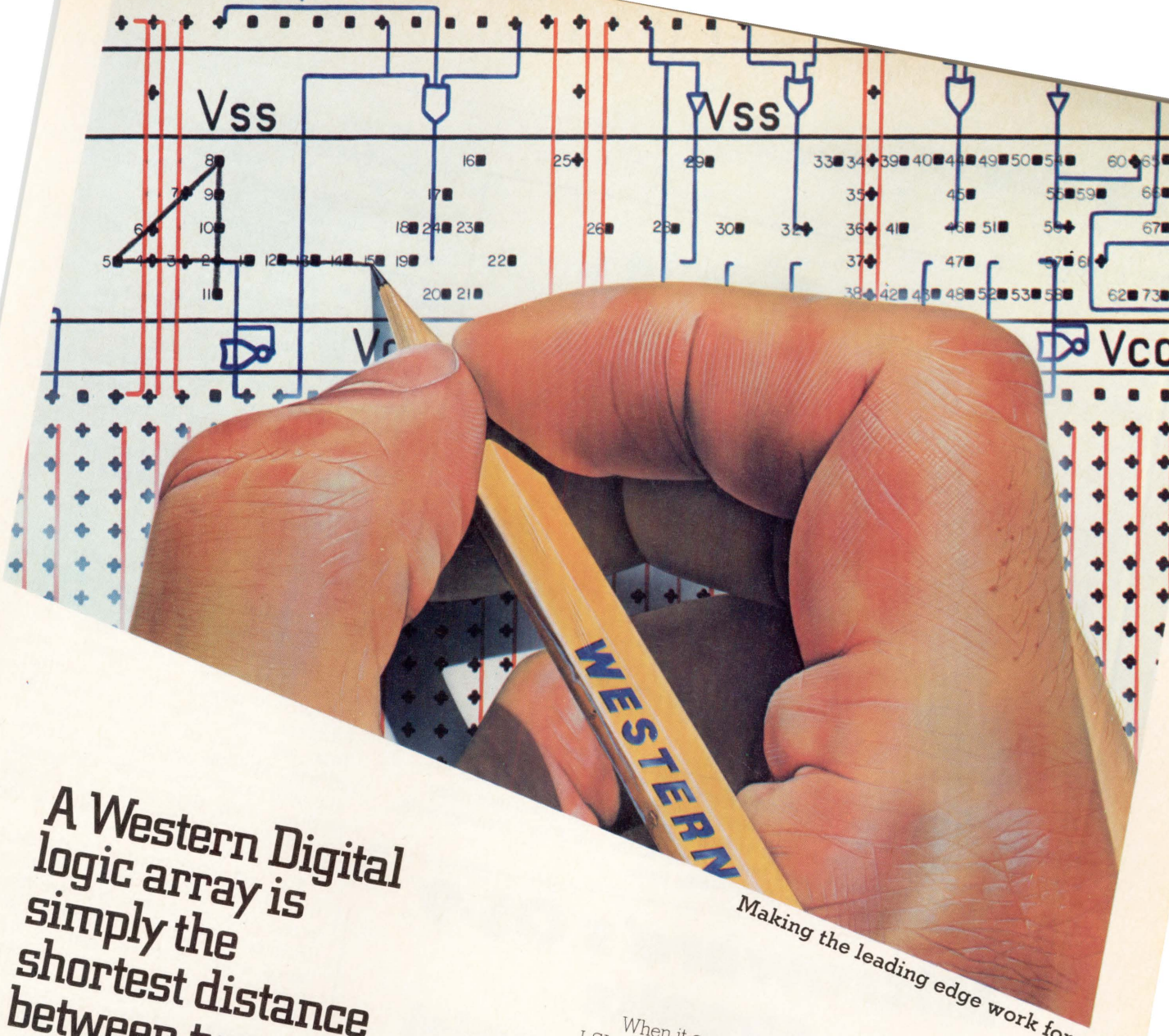
Multibus is a trademark of the Intel Corp. LSI 11 is a trademark of Digital Equipment Corp. EXORciser is a trademark of Motorola.

COMPUTERS

32-bit mini fits both technical/commercial areas

Small and cost-effective, the entry level model 3210 is appropriate for both technical and business computing. Capitalizing on its experience in 32-bit hardware and software, Perkin-Elmer Corp designed the unit to compete effectively with 16-bit systems from other manufacturers. The machine, while a low end system in the 3200 series, has more computing power than the largest 16-bit units, since 32-bit minicomputers can handle larger, more complex ap-

(continued on page 88)



A Western Digital logic array is simply the shortest distance between two points.



Making the leading edge work for you.

When it comes to integrating your digital design into LSI, there are basically two ways to go.

The Western Digital way. And, the long way.

Go with Western Digital and what you get is, in a word, simplicity.

For example, take our Logic Array Design Kit. It makes designing your own LSI circuits almost as easy as a connect-the-dots puzzle.

And as soon as you've finished your design, we digitize it, qualify it, test it and quickly transform it into a high-quality, semi-custom chip.

So, you get your prototypes in 4 to 6 weeks. Not months.

With Western Digital you also get a balanced complement of gates and flip-flops, greater reliability and a significant savings in board space. All for a price that makes good sense. Whether you need 1,000 or 10,000.

Western Digital eliminates plenty of headaches, too. Like plenty of complex transistor-level circuits, and costly computer-aided design. And plenty of waiting.

Like up to 6 months just for prototypes.

The choice is yours. But for the shortest, most practical route to market, contact the logic array experts at Western Digital.

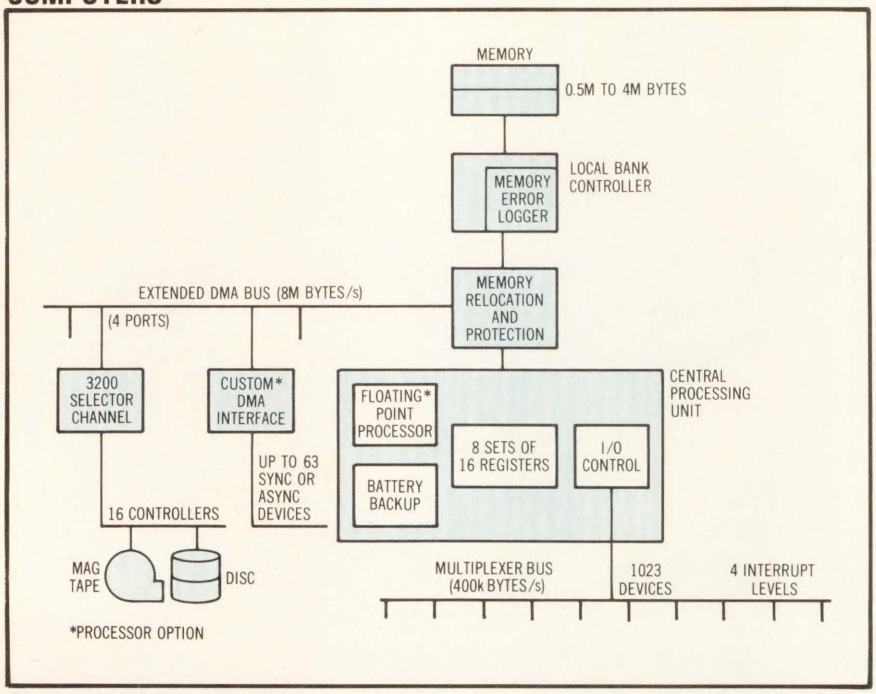
All you've got to lose is a long wait.

WESTERN DIGITAL
CORPORATION

Computer Products Division, 2445 McCabe Way, Irvine, CA 92714, (714) 557-3550.

CIRCLE 46 ON INQUIRY CARD

COMPUTERS



Entry level 32-bit minicomputer. Perkin-Elmer's new 3200 series machine serves both technical and commercial environments. Addressing up to 4M bytes of memory, it supplies the performance of larger, higher priced machines using 32-bit architecture with both 32-bit internal data paths and 32-bit memory paths, and both high and low speed communications paths

plications than their 16-bit counterparts.

Packaged in a 30″ (76-cm) cabinet, the system addresses up to 4M bytes of main memory and supports up to 32 users running various complex applications programs. It incorporates state of the art technologies in its memory and integrated cartridge disc drive systems. The basic configuration includes 512k bytes of MOS memory built using either 16k or 64k RAMs, system console, power supply with battery backup, 27M-byte cartridge disc drive, selector channel, and disc controller, and is priced at $49,900.

Central processor in the system provides 32-bit architecture including 32-bit internal data paths and 32-bit memory paths for high throughput. The 3210 incorporates eight sets of sixteen 32-bit general purpose registers. Register to register instructions permit operations between any of the 16 registers within a set, eliminating redundant loads and stores. Four sets of registers are dedicated to handling the four external interrupt levels. Three of the remaining four are allocated by the operating system. Multiple register sets alleviate the need to save and restore the general registers every time there is a context switch, thus significantly reducing the context switching times.

Two separate external communications buses are provided. The multiplexer (MUX) bus interfaces slower devices transferring data at 2M bytes/s; a high speed enhanced direct memory access (EDMA) bus interfaces secondary storage devices such as discs and tapes. This bus can handle transfers at 8M bytes/s in burst read mode, at 5.7M bytes/s in burst write.

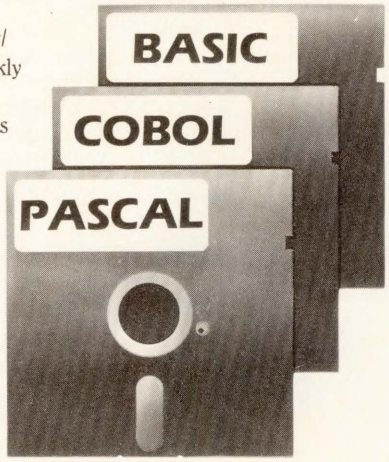
The processor supports up to 4M bytes of directly addressable main memory, using 64k-byte, 5-V RAM chips. Memory expansion is available in 512k-, 1M-, and 2M-byte modules, up to a maximum of 4M bytes in the single cabinet. Memory access time is 400 ns. Error correction is performed on a full 32-bit word using a 7-bit modified Hamming code. These seven additional bits on each word in memory perform error detection and correction on all single-bit errors. All double-bit errors are detected with some multiple-bit errors detected.

An integrated dual cartridge and fixed disc secondary storage system combines both performance and capacity of a Winchester technology fixed disc and convenience of removable media for software distribution, data transfers, and system backup. The dual-drive subsystem eliminates the need for magnetic

(continued on page 90)

Microware's OS-9™ speaks your language(s)

Microware's multilingual OS-9™ Multiuser/ Multitasking Operating System can be quickly installed on almost any 6809 microcomputer. This Unix*-like Operating System has become the industry standard due to its reliability, versatility, and supurb performance. And it is supported by the most-wanted languages: BASICØ9, COBOL, PASCAL; and software tools: Stylograph Word Processor, Macro Text Editor, Assembler, and more. Additional languages and applications programs are available for OS-9™ from many other software houses. For information on attractive OEM licensing plans, contact:



MICROWARE® 5835 Grand Ave., Des Moines, IA 50312
(515) 279-8844 • TWX 910-520-2535

International Representatives: Australia, Semcon Microcomputers, Ltd., Sydney, Tel. 02 848-0800. England, Dialogue Marketing, Ltd., Tel. (06285) 29222,Tlx. 848080 MICRO G. Germany, Prodata, Schriesheim, Tel. 0 62 21 / 86 04 26, Tlx. 465008 WEISS D. South Africa, Eagle Electric Co. (Pty) Ltd., Capetown, Tel. 45-1421, Tlx. 57-20713 SA. Switzerland, Digicomp AG, Zurich, Tel. 01 66 12 13, Tlx. 812035 DIGI CH.

*Unix is a trademark of Bell Telephone Laboratories. BASICØ9 is a trademark of Motorola, OS-9 is a trademark of Motorola and Microware.

CIRCLE 47 ON INQUIRY CARD

Making the leading edge work for you.

Look who's turning the disk controller market upside down.

It's no secret. Western Digital has been building a reputation for innovative disk controllers for years.

It started back in 1977 with the world's first LSI floppy disk controller. And now includes the first Winchester disk controller, too.

What's more, today, Western Digital's 7-member family of floppy disk controllers is *the* industry standard. Giving you nothing short of the broadest selection of controllers in the business.

And only Western Digital offers the vital support chips for both data separation and DMA control.

Of course, our pioneering Winchester controller effort is equally impressive. Either as a fully-assembled board or money-saving chip set. And our extensive on-line design support services are yet another plus.

Better still, more breakthroughs are on the way. So contact the only disk controller maker holding all the chips.

Western Digital.

We'll stand on our head to give you better solutions.

WESTERN DIGITAL
CORPORATION

Computer Products Division, 2445 McCabe Way, Irvine, CA 92714, (714) 557-3550.

CIRCLE 48 ON INQUIRY CARD

COMPUTERS

tape drive units for system backup, greatly reducing overall system cost. The system can be configured with 16M, 48M, or 80M bytes (unformatted) of Winchester fixed media storage, plus an additional standard 16M bytes of removable cartridge disc storage.

Both disc drive subsystems house their own independent servo, monitor, and control circuitry for reliability and system performance. The drives house two separate, independent head positioners which require no servo relock time and/or volume verify time when alternating between media. Both discs are referenced precisely to their own servo surface, eliminating any cylinder tracking discrepancies when changing volumes. Disc drive logic incorporates an internal microprocessor which replaces traditional disc drive electronic components. This microprocessor improves both reliability and maintainability, including diagnostic function capabilities.

When integrated with Reliance, the company's commercial software offering for transaction processing, the 3210 provides facilities for developing business applications programs. The 32-bit processing system is completely compatible with models 3220, 3230, and 3240. It uses the multitasking OS/32 operating system, and runs 32-bit languages that include the globally optimizing ANSI-77 FORTRAN VII, Pascal, ANSI standard COBOL, BASIC, CAL MACRO, RPG II, and CORAL 66. EDITION VII WORKBENCH, a standard version of the UNIX™ multiprogramming, timesharing operating system, is available on the unit and is fully supported by Perkin-Elmer as a standard product.

Price comparisons for 32-bit computers provided by Perkin-Elmer put the 3210 at $58,700, while a DEC VAX-750 sells for $89,900. A 16-bit Data General C350 with 512k-bytes memory and 20M-byte disc running RDOS sells for $79,000, while an equivalent configuration of the 3210 has a $56,000 tag. Base price of the system is $49,900; this includes 512k-byte memory, 16M-byte fixed disc, 16M-byte removable disc, console terminal, battery backup, memory error logger, loader, and clock. **Perkin-Elmer, Data Systems Group**, 2 Crescent Pl, Oceanport, NJ 07757.

Circle 257 on Inquiry Card

Extended instruction set in microcode extends processor performance

Initial tests performed on the Mark VIII indicate performance improvements as great as 100% over the earlier Mark V. According to Renny Bosch, vice president of new product research at Point 4 Data Corp, this results from a greatly extended instruction set implemented in microcode.

Like its predecessor, the computer provides a high speed central processor implemented with bit slice circuits, 128k bytes of main memory, and all options on a single printed circuit board. With its 7-slot chassis housing, it has ample additional room to accommodate various peripheral controllers. While supplying greatly increased throughput, the computer maintains software compatibility with both Mark III and V, making applications programs for those systems usable on the new CPU, and has a list price of only $10,700.

The computer can use the high speed interprocessor bus (HIP) to communicate with a second like computer at memory access speeds. Memory cycle time of 400 ns/word results in transfer rates of 5M

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COMPUTERS

bytes/s. To achieve these rates, the bus provides an additional high speed DMA port that connects to dual-ported memory in the second computer. The two computers can run simultaneously in parallel, transferring data as acquired or after processing.

A set of firmware instructions replaces a large number of functions that were previously implemented using subroutines or inline routines of several instructions within the IRIS operating system. The result is an increase in both processing speed and operating efficiency.

Implementing functions in firmware effectively reduces the time necessary to fetch an instruction from 400 to 100 ns. This, in conjunction with the pipelined CPU architecture, achieves an instruction rate of 7.5M instructions/s for routines executed directly in firmware. "In addition," according to Bosch, "each firmware instruction is 80-bits wide while a standard software instruction is 16-bits wide. Thus, more functions can be implemented in a single instruction set."

Among the 2000 macroinstructions developed for the CPU is a subset of 2-word instructions. These further improve efficiency by permitting the CPU to perform many functions as 32-bit instructions even though the address bus to memory is 16-bits wide. Significant among the firmware instructions are literal byte compare and literal byte access instructions. Hardware stack pointer and push and pop instructions supply a means of implementing stack oriented system software. Decimal add/subtract instructions offer a nibble shift ability that allows four bits of data to be left or right shifted at one time. An extended translation instruction allows a 1-byte parameter to be translated and vectored to a routine through a 256-word table. The extended instruction set was developed by the software group and then implemented by the hardware design staff; an approach that ensures the efficiency and relevancy of the instructions. **Point 4 Data Corp**, 2569 McCabe Way, Irvine, CA 92714.

Circle 258 on Inquiry Card

Engineering workstation integrates administrative and development tasks

Designed for hardware and software development, this computer based engineering workstation also performs administrative, documentation, and other tasks in a research and development environment. In developing the unit, by keeping space limitations and engineering functions in mind, Convergent Technologies has produced a compact design with a high degree of portability that integrates all engineering tasks.

The machine is a display-based computer designed around a 16-bit microprocessor. An optional 8087 arithmetic processor provides high speed computation. Each workstation consists of a lightweight desktop display and detachable keyboard. The 15″ (38-cm) display is organized as 34 lines of 80 or 132 characters and refreshes at 50 MHz. The screen is divisible into virtually unlimited windows down to the character level.

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Mass storage and electronics are housed in a floor-standing module. Storage devices range from a 1M-byte dual floppy to a 120M-byte Winchester subsystem. Up to 16 workstations can be combined in a distributed network. Individual workstations or clusters of workstations can communicate with a mainframe to up-load or down-load large scale programs or data bases.

For hardware development, the workstations offer five IEEE-796 standard Multibus® slots for linking and testing peripherals and instruments. These slots facilitate testing and debugging of multiperipheral system configurations, control loops, multiple sensors, and instruments for prototype development.

Processing power, large memory and mass storage capacity, plus full megabyte addressing capability, aid software development. The workstations offer five industry standard programming languages: ANSI 77 FORTRAN, ANSI 74 COBOL, Pascal, and BASIC, in addition to assembly language. A linker/librarian links object modules from the diverse languages, permitting applications to be written as a set of independently compiled modules in different languages with references to one another through cross-module calls.

For efficient software development, the text editor provides the capability to insert or delete single characters or groups of text, search for a string of characters, and move a block of text within a file or to/from another. The debugger provides facilities necessary to debug realtime applications on the system. It supplies breakpoint capability, single-step execution, initiation of execution, memory and register examination and modification, process and exchange status display, and trace of procedure nesting on the stack.

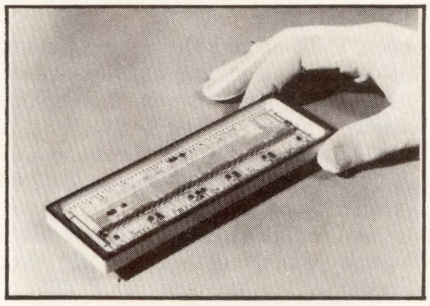
For technical manual preparation, a text processing package allows simultaneous display of up to eight separate documents. Configurable pages, layouts, and automatic recovery of operator keystrokes after power failure are standard features.

List price for the workstation with 128k bytes of RAM, 10M bytes of Winchester, and 0.5M bytes of floppy disc storage is $22,500. Volume discounts are available. **Convergent Technologies**, 2500 Augustine Dr, Santa Clara, CA 95051.

Circle 259 on Inquiry Card

SYSTEM ELEMENTS

Charge-coupled device chips form high resolution image array assemblies



Buttable CCD chip array. Hybrid electro-optical sensors using buttable CCDs form continuous arrays that may be mounted for superior image quality, rapid data readout, and sensitivity up to 100 times better than that of conventional single-line arrays. Sensors (pictured), a 45-chip array, have a resolution power of more than 10,000 picture elements with gap of only two pixels between each chip and data gathering capability of 200M pixels/s

Mechanically buttable CCDs that mount in arrays of arbitrary length with minimal loss in image quality are the result of five years research by Itek Corp and Bell Northern Research. The electro-optic sensor technology offers the potential for high image resolution and sensitivity in military, medical, and industrial applications.

The electro-optic sensor uses CCD chips that are mechanically buttable—capable of being mounted side by side with all connections made through the sides of the chips. Chips joined in such a way can be assembled to form rugged CCD sensors of arbitrary length, eliminating the complex mirrors and beam splitters necessary in previous imaging array assemblies.

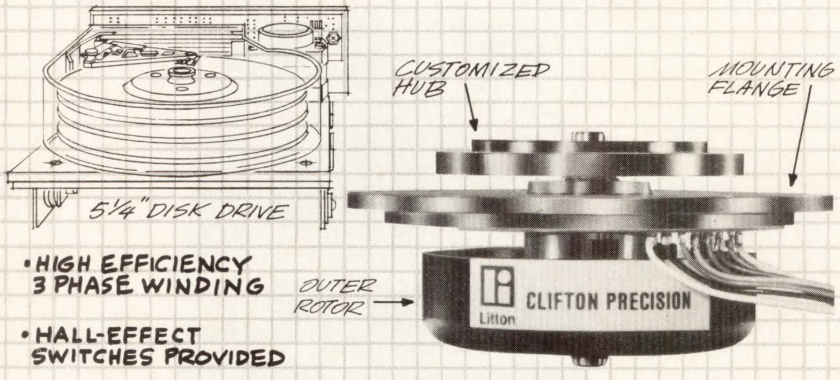
A 5-chip hybrid formed has resolution in excess of 10,000 picture elements, and a gap of only 2 pixels between each pair of chips. The chips used contain 2048 x 96 sensing elements each, spaced at 13-μm intervals. Spectral sensitivity ranges from 0.4 to 0.1 μm, and line rate is 20,000 lines/s. Time delay and integrate (TDI) operation can be used for an effective sensitivity improvement of as much as 100 over that possible with a conventional single-line array.

The sensor obtains the ability to define some 10,000 shades of gray through a computerized dynamic scaling

(continued on page 94)

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SYSTEM ELEMENTS

process. Very high readout speeds are attained through multiple signal taps at 256-element intervals. Information can be read from each tap at a rate of 5M pixels/s. With 8 taps/chip, the 5-chip sensor has a data gathering capacity of 200M pixels/s.

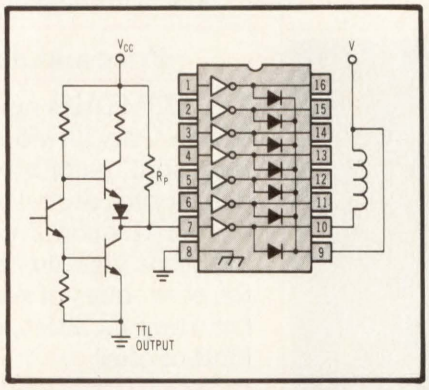
Producing excellent images even when optical contrast is very low, the sensors are suitable for use in military surveillance/reconnaissance of large land areas. In industry, potential applications include inspection of complex electrical components, and use within automatic assembly equipment that requires sensors with very high spatial resolution. They could also serve as the eyes for industrial robots programmed to detect the size, shape, and position of various components in an assembly process.

The CCD hybrid's sensitivity to x-rays opens a range of diagnostic procedures in internal medicine. The sensors can enhance x-rays in real time in conjunction with an intensifying phosphor screen.

Itek is currently performing development work on use of the sensors in quality control. It is also exploring the feasibility of incorporating them into x-ray equipment to provide higher quality realtime images for fluoroscopic and radiographic procedures. **Itek Corp**, 10 Maguire Rd, Lexington, MA 02173; and **Bell Northern Research**, Ottawa, Ontario, Canada.

Circle 260 on Inquiry Card

High voltage, high current Darlington transistor arrays second sourced



Pullup resistors. Exar uses resistors with XR-2003 Darlington transistor array to increase drive current

Two families of high voltage, high current Darlington transistor arrays are now second sourced by Exar Integrated Systems, Inc. Originally introduced by Sprague Electric Co in plastic packages, the newly available XR-2001/2002/2003/2004 group is implemented in 16-pin ceramic packages. The XR-2011/2012/2013/2014 family is now available in plastic and ceramic.

Both families consist of seven silicon NPN Darlington pairs on a common monolithic substrate. The outputs for both groups are open collector and may be wired together. Internal output diodes allow the driving of inductive loads without need for external diodes.

The XR-2001/2004 products operate with peak inrush currents of up to 600 mA. The 2011/2014 family operates with peak inrush currents of up to 750 mA. The outputs may be paralleled to achieve higher load current capability, although each driver in the 2001/2004 group has a maximum continuous collector current rating of 500 mA; the 2011/2014 group has a rating of 600 mA. The drive current can be increased by using pullup resistors as shown in the Figure. **Exar Integrated Systems, Inc**, 750 Palomar Ave, Sunnyvale, CA 94088.

Circle 261 on Inquiry Card

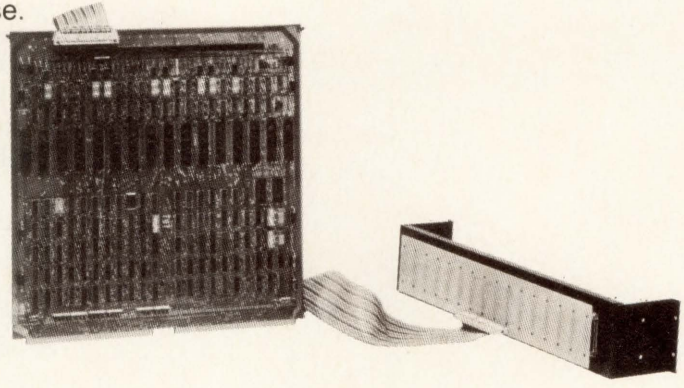
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CIRCLE 53 ON INQUIRY CARD

SYSTEM ELEMENTS

Large, flat panel display implemented in gas electron phosphor technology

A prototype gas-electron-phosphor (GEP) display panel, developed by Lucitron Inc, the 34.4″ (87.4-cm) diagonal, 3″ (8-cm) deep, FLATSCREEN™ panel offers 12.5 elements/in (4.9/cm) vertically and 18.5 elements/in (7.3)cm) horizontally, or 131,072 dots with 128 levels of gray. Using 0.56″ (1.42-cm) high, 5 x 7 dot matrix characters, this resolution will yield 25 rows of 85 characters/row. Luminance is more than 50 ft-L (171 cd/m²) in white and higher in green, to allow viewing in a brightly lit room. Viewing angle is restricted only by the distortion of an off center line of sight. Edges and corners are in the same focus as the screen center. An RS-170 interface is standard. The entire screen is accessible; information can be scrolled and rotated.

The new GEP technology uses a gas discharge for scanning and selection. In the process, electrons are extracted from the gas discharge and accelerated to produce light from conventional CRT phosphors. Because of the panel's internal multiplexing, a full resolution display requires only 96 drivers. Such a display on an ac plasma panel, on the other hand, uses 1024 drive circuits; 16 for horizontal scan, 10 for vertical scan, 32 video drivers, 32 cathode leads, and 4 others including high voltage.

The company sees applications for the panel in military command and control, CAD/CAM, stock brokerages and exchanges, MIS, teleconferencing, training, process control, airport and hotels, and conference product displays. The panel weighs about 40 lbs (18 kg). Power consumption is less than 1000 W for a fully illuminated display. The first product is slated for shipment in the first quarter of 1982. **Lucitron Inc**, 1918 Raymond Dr, Northbrook, IL 60062.

Circle 262 on Inquiry Card

PERIPHERALS

Graphics and imaging system presents true 3-D display

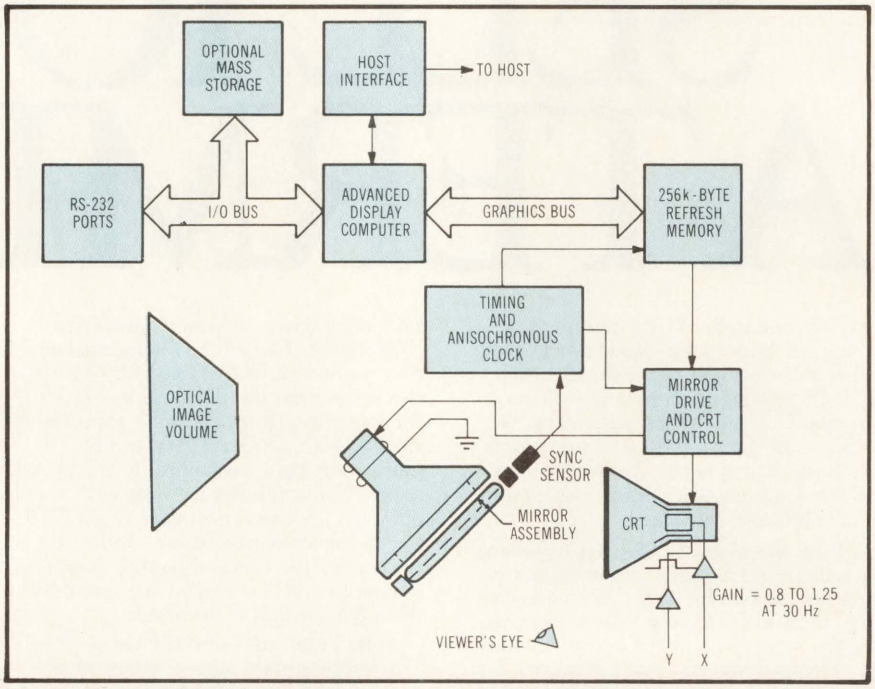


Fig 1 Genisco SpaceGraph synch sensor. Located at mirror rim, sync sensor modifies divisor of anisochronous clock to create equal divisions of physical travel for vibrating mirror

A 3-dimensional display system with extensive standalone features presents graphics and imaging data in a space-filling optical volume, allowing the operator to see different perspectives by moving his head in relation to the image. The SpaceGraph terminal, by Genisco Computers Corp, projects images from an electrostatic vector CRT located above the operator's head onto a flexible, variable focal length mirror. Optical depth axis is created by slight changes in the curvature of the mirror, resulting in relatively large changes in its focal length and image area depth viewed by the user. A mirror motion of 0.38 cm yields viewed Z axis of about 30 cm.

The flexible mirror, vibrating at 30 Hz, is mounted on a hi-fi woofer. The terminal's timing logic divides that motion into 32,768 separate image planes—16,384 each for the forward and rearward phase of its travel. In graphics mode, the CRT writes one dot for each image plane, to a random point on its 4096 x 4096 screen in 500 to 600 ns. It therefore can easily keep up with the motion of the mirror and build an image of up to 32,768 separate planes from the roughly 0.5 x 10^{12} voxel positions available in the image volume.

In order to achieve an image the operator could treat as truly 3-D, two sources of distortion had to be overcome. One, the anomalous perspective caused by writing to different mirror points, had caused lines intended to

(continued on page 98)

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CIRCLE 55 ON INQUIRY CARD

PERIPHERALS

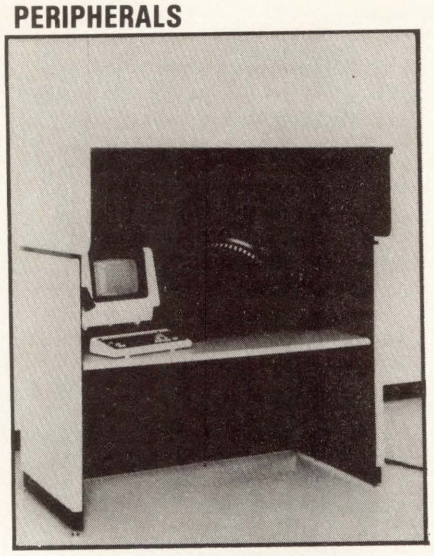


Fig 2 Electrostatic deflection CRT. SpaceGraph unit writes to points on its screen which are then reflected at optical image volume in vibrating mirror, where the 3-D image appears. Alphanumeric terminal at operator's left is used to control display system

recede in Z-space as parallels (and thus appear to converge) to in fact diverge because of the mirror's curvature. The second distortion resulted from the sinusoidal rather than constant motion of the mirror with respect to time. To obtain equal increments of mirror motion, different increments of time were assigned to each image plane.

Both problems are solved in hardware. The anomolous perspective is corrected by attaching variable gain amplifiers to the X and Y deflection plates of the CRT. Amplifier gain is controlled by a sensor on the mirror rim, and varies from 0.8 to 1.25 of nominal in step with the 30-Hz period of the mirror. A given dot is therefore moved a proportional amount nearer or farther from the center of the CRT to compensate for the divergence in optical volume caused by the curved mirror surface.

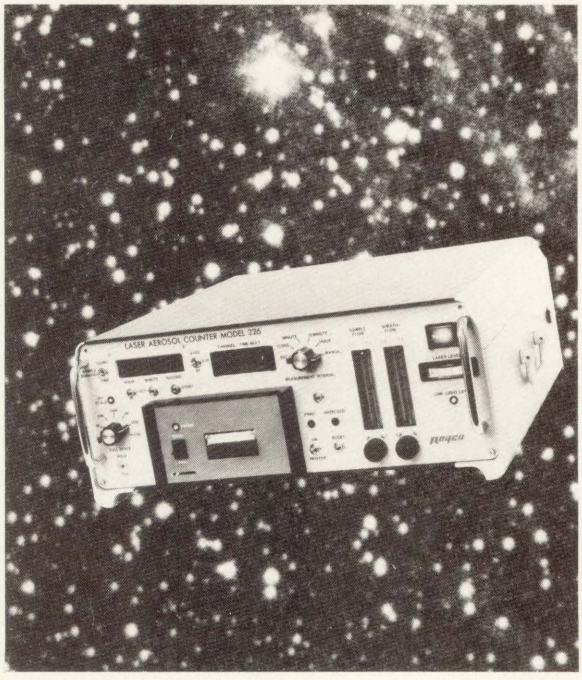
The synch sensor on the mirror rim is also used to control timing and correct for the continuously changing rate of mirror motion. Since the mirror slows and even stops for an instant at each end of its travel, 20% of the forward and rearward motion is not used for display. The synch sensor relays rate of motion information to the anisochronous clock. The sensor information is used to calculate an ever changing divisor for clock pulses; a shorter time slice is assigned to rapid travel and a longer slice to slower travel. Mirror motion is broken into equal slices of physical distance. (See Figs 1 and 2.)

In addition to the graphics mode, in which the terminal's advanced display computer generates vectors from host data to create wireframe figures, the SpaceGraph also supports an imaging mode. Display data in imaging mode are transferred directly from the host computer to the display's refresh memory via a DMA channel. In imaging mode, a total 262,144 voxels can be displayed as data planes stacked one behind the other. The user can select the number of planes, the display resolution, and also remove planes in front to view data on the inside of the image. Display volume configuration can vary from 64 planes with a resolution of 64 x 64, to 4 planes of 256 x 224 voxels each.

In both graphics and imaging modes, each voxel has an 8-bit intensity value

(continued on page 100)

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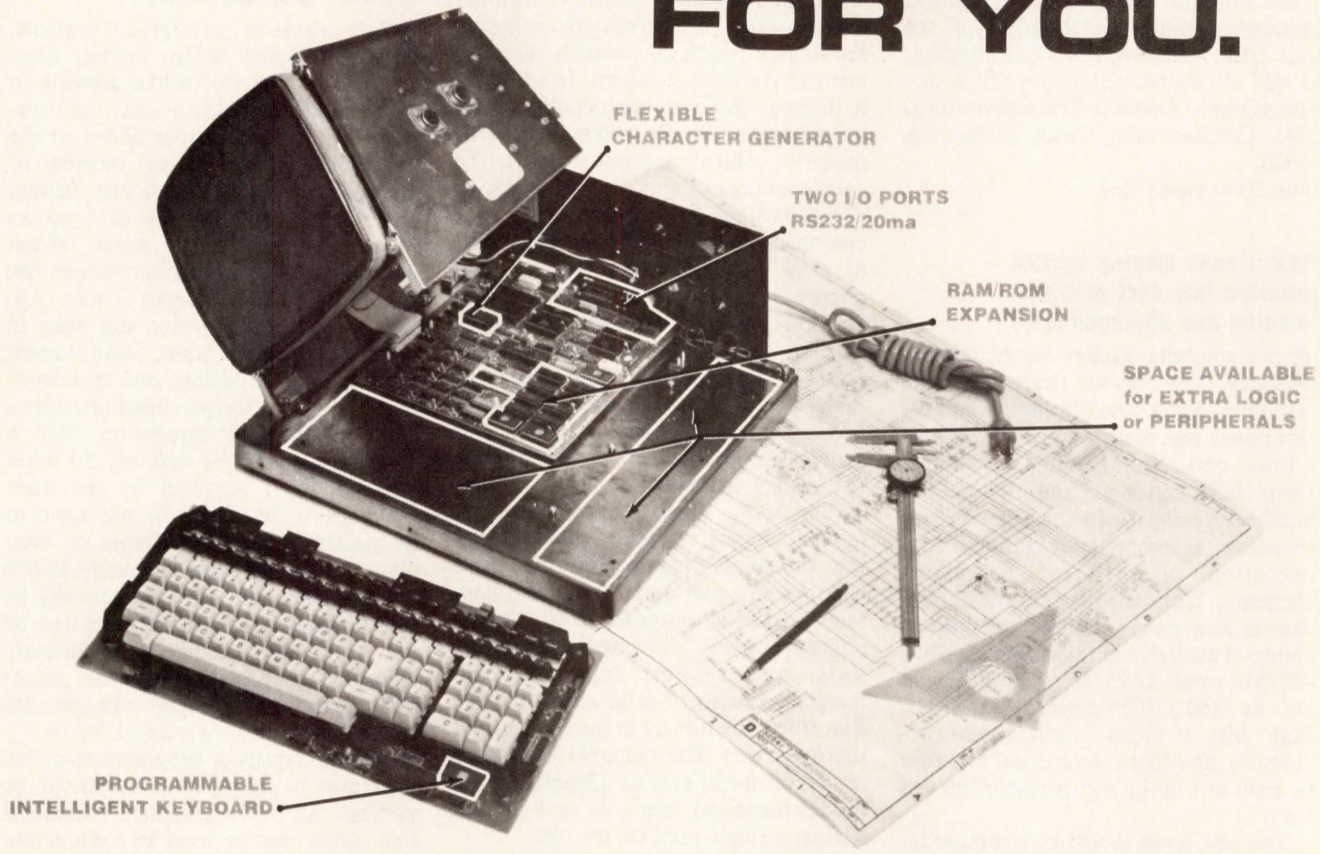
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CIRCLE 57 ON INQUIRY CARD

PERIPHERALS

with seven bits determining gray scale (128 values) and one bit allowing the voxel to be blinked or blanked. By choosing to write only graphics during the forestroke of the mirror, and an image during the backstroke, the user can combine the two display modes. Software subroutines conforming to the Siggraph graphics CORE standard perform processing and transformation of the data base, view selection, and clipping, as well as other functions specific to the SpaceGraph. **Genisco Computers Corp**, 3545 Cadillac Ave, Costa Mesa, CA 92626.

Circle 263 on Inquiry Card

Raster scan display system provides low cost graphics imaging and alphanumerics

Architecturally similar to the RM-9000 series, the RM-9450 series of high resolution raster scan display systems offers power and features of the RM-9000 at a lower cost. Manufactured by Ramtek Corp, both series use the multiple-bus architecture shown in the Figure. This structure accommodates simultaneous operation of different processing elements. Consisting of a rackmount chassis and power supply, the RM-9450 system is available in resolutions of 640 x 480/512 pixels at 25/30 or 50/60 Hz, as well as 1280 x 1024 pixels at 25/30 Hz. Eight bits of refresh memory are provided in the 640 x 512 versions, and four or eight bits in the higher resolution version.

The new series is software compatible with the RM-9000. Software features include context switching, display list processing, high resolution fonts, clipping, textured lines, filled polygons, pan and zoom, high speed erase, and local functions. A subset of the RM-9400, the RM-9450 firmware decodes and processes a high level binary formatted instruction set, which is RM-9000 compatible, over a high speed 16-bit parallel interface. The instructions are immediately executed or stored as subpictures in a 12k-byte user RAM space for deferred execution.

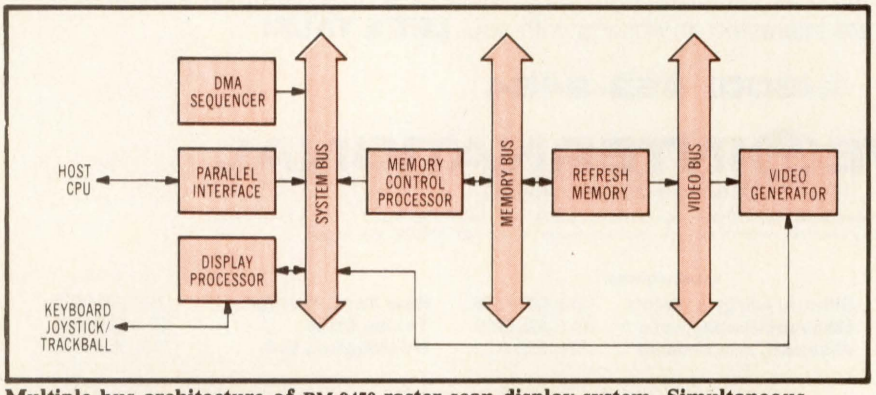
TTL DMA Sequencer performs high speed, nonprocessor transfers involving multiple devices on the system bus, as, for example, between the computer interface and display processor or memory control processor. Directly or indirectly the display processor controls each element of the display system. In addition, it decodes received instructions, stores subpictures and fonts, and may drive the memory control processor (MCP). To enable storage of subpictures, fonts, or downloading Z80 object code for customer-specific requirements, the display processor contains a Z80 microprocessor with 32k bytes of EPROM and RAM, a timer, memory map, cycle-stealing DMA, interrupt control logic, and 12k bytes of additional user RAM. Serial ports are provided for interfacing a keyboard and joystick/trackball. A general purpose interface is provided on the display processor.

The MCP, which draws primitives (alphanumerics, graphics, images, etc) into the refresh memory and performs clipping and pan and zoom, also contains a special purpose 16-bit bipolar microprocessor with dedicated ROM, RAM, and support logic. Refresh memory consists of solid state MOS RAM that stores the picture in raster scan, dot matrix format. The memory is organized in 4- or 8-bit groups (depending on model numbers). Each 4- or 8-bit cell defines a single pixel on the CRT.

The video generator transforms the stored picture into industry compatible video signals. All outputs utilize, as a guide, EIA standards RS-170 or RS-343-A specifications for composite video.

Cursor and overlay mixing is performed either in a lookup table or through P/ROM. Three off the shelf video generators satisfy most applications. **Ramtek Corp**, 2211 Lawson Ln, Santa Clara, CA 95050.

Circle 264 on Inquiry Card



Multiple-bus architecture of RM-9450 raster scan display system. Simultaneous operation of different processing elements allows high throughput

3-D surface processor upgrades graphics family

A 3-D surface processor option, from Megatek Corp, permits users to fill in any part of a line drawing to create solid, textured, or patterned surfaces. The option can be added to the Graphics Engine™ of any member of the company's WHIZZARD 7200 family. The family includes the 7210 stroke refresh system, the 7250 raster refresh system, and the recently announced 7290 dual-output stroke/refresh system. Applications for the option are seen in seismic data presentation, finite element or solid object modeling, and LSI layout.

Functionally, the processor provides a true polygon fill capability; only a polygon needs to be defined; no other information is supplied by the user. Polygons to be filled do not have to be standard sizes and shapes or even planar. They may have as many as 670 defined sides and will automatically be filled with surface vectors generated by the processor. Using a proprietary algorithm and pipelining, with vector calculation, the processor can generate fill vectors in less than 2.5 μs/vector.

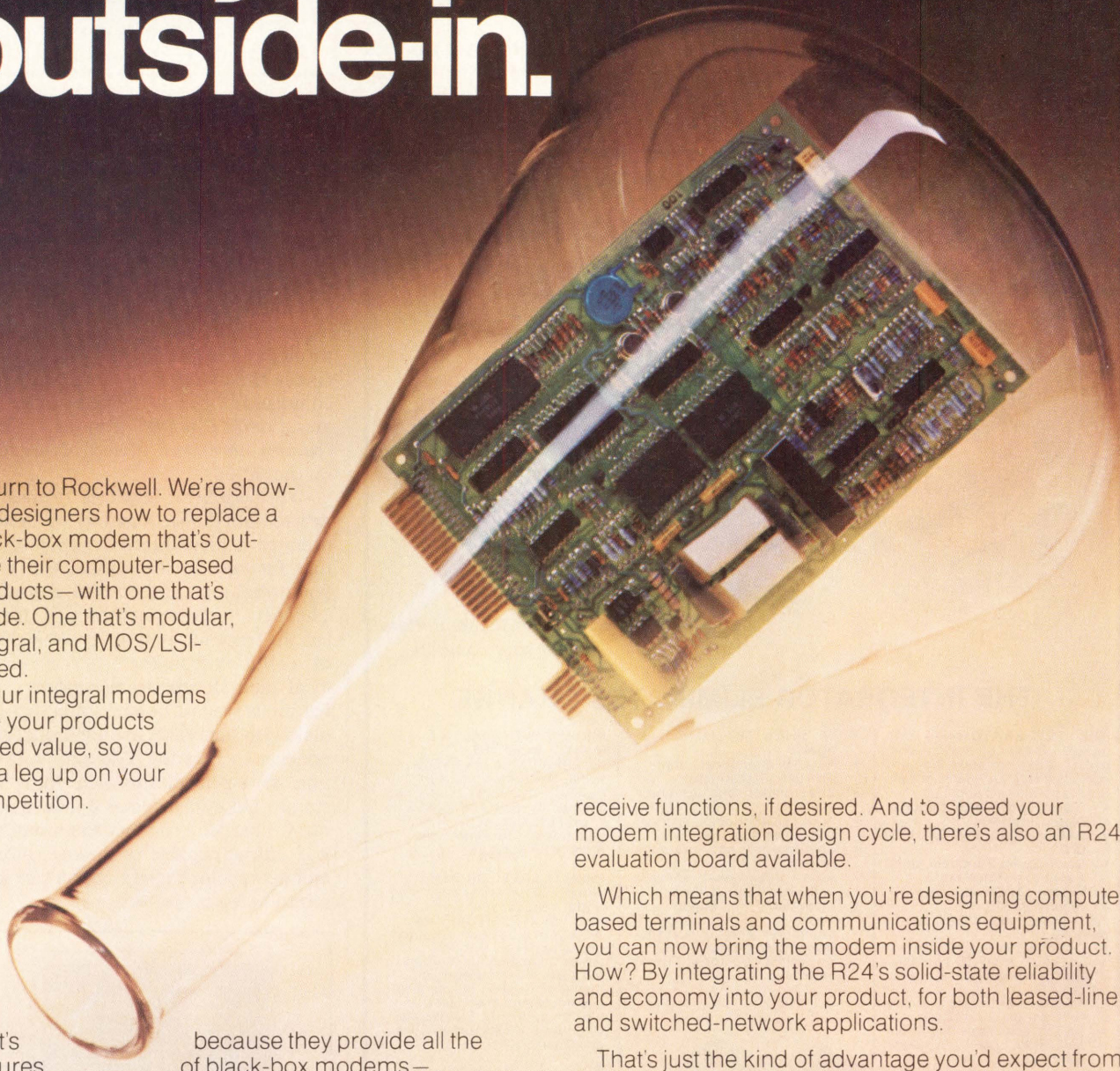
The fill density is programmable. Fill lines may be specified as horizontal or vertical. All of the company's standard line styles may be used in conjunction with the fill lines to create pattern or textured fills. Once an object is filled with a color, the outline of its shape may be drawn in another color, for emphasis.

A unique feature of the 3-D surface processor is that it allows for true holes in objects. The holes, in this system, are left unpainted within the filled object; thus graphic data that would normally be seen through the hole are seen.

The surface processor may be used with or without the optional WHIZZARD hardware module for clip, rotate, scale, and translate (HCRST) functions. When combined with the HCRST module, the surface processor's fill function occurs after a rotate, scale, or translate function, but before the clip function. The filled object thus may be rotated, scaled, or translated dynamically. **Megatek Corp**, 3931 Sorrento Valley Blvd, San Diego, CA 92121.

Circle 265 on Inquiry Card

How to turn your modem outside-in.



Turn to Rockwell. We're showing designers how to replace a black-box modem that's outside their computer-based products—with one that's inside. One that's modular, integral, and MOS/LSI-based.

Our integral modems give your products added value, so you get a leg up on your competition.

That's because they provide all the features of black-box modems—but at a fraction of their cost. Plus their compactness gives you new physical design freedom.

And Rockwell modems are available at a level of integration that meets your requirements. Take our R24, for example. A 2400-bps synchronous modem, it comes in three configurations—all exceptionally compact, and compatible with Bell 201 B/C and CCITT V.26 A/B standards.

First there's our fully assembled and tested single-board modem, ready to plug into your system—like the one shown above. Then there's our set of three discrete modules, ready to be designed into your own modem. They allow you to separate transmit and receive functions, if desired. And to speed your modem integration design cycle, there's also an R24 evaluation board available.

Which means that when you're designing computer-based terminals and communications equipment, you can now bring the modem inside your product. How? By integrating the R24's solid-state reliability and economy into your product, for both leased-line and switched-network applications.

That's just the kind of advantage you'd expect from Rockwell, the company that's delivered more integral LSI 4800/9600-bps modems than anyone else in the world. That's right—*anyone*. And Rockwell modems are in stock now—fully assembled, on production or evaluation boards, or as discrete modules.

So don't leave your modems on the outside looking in. For information or applications help, call toll free: (800) 854-8099; in California, (800) 422-4230. Or write: Rockwell International, Electronic Devices Division, RC55, P.O. Box 3669, Anaheim, CA 92803.

Rockwell International

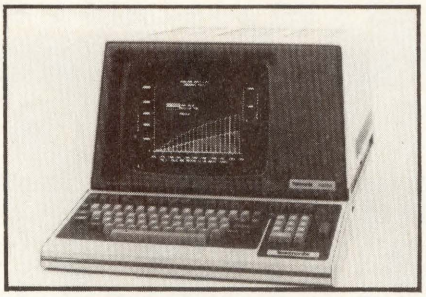
...where science gets down to business

CIRCLE 58 ON INQUIRY CARD

PERIPHERALS
Monochrome and color display terminals upgraded

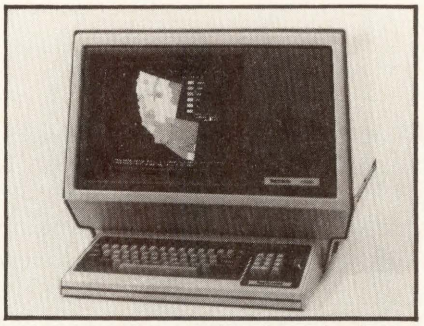
Faster data communications and enhanced capability are offered in an upgraded version of Tektronix's 4020 series. The fully compatible 4020A series from Tektronix Inc includes the 4025A, a raster scan terminal with text handling and graphics capabilities, and the 4027A color terminal. Statistical analysis, computer aided presentations, technical programming, laboratory analysis, and project management are seen as applications for the terminals' alphanumeric and graphics capabilities. Existing 4020 series terminals can be upgraded via field installed circuit boards.

The series' internal processor has been upgraded from the 8080 to the 8085 and



more local processing speed provided through E-ROM based firmware. Both the 4025A and 4027A will handle data communications throughput, with flagging, at speeds of up to 9600 baud. In some cases, users will find that flagging is not necessary to achieving maximum throughput. Both terminals now include a 16k display memory base. The 4027A maintains a 48k base of graphics memory. Increased local graphics throughput capability in the 4025A includes the addition of up to 16 macro commands, locally defined circles and arcs, and clipping firmware. These features have been offered as standard on the 4027.

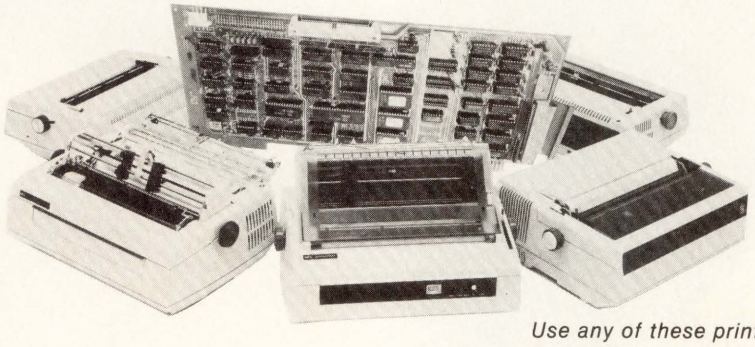
GPIB peripheral interface firmware is new to both the 4025A and 4027A, allowing users to achieve plotter output resolution far beyond the normal 640 x 480 point resolution of the terminal displays. The new plotter pass-through feature lets the terminals pass 4096 x 4096 points of resolution from the host computer or local tape storage to the plotter. This feature is seen to be well suited for slide making systems that use additional components such as the Tektronix 4662 Option 31 8-pen plotter and local tape storage. Also included as standard in the 4027A is hardcopy and video output, plus RGB output capable of driving color TV monitors, color camera systems, or large screen video projectors.



A new 4025A option is a keyboard graphic input (GIN) feature which allows the user to pick X-Y coordinates from the terminal display using a full-screen crosshair cursor, and automatically transmit those coordinates back to the host. GIN capabilities are standard on the 4027A. **Tektronix Inc**, PO Box 500, Beaverton, OR 97077.

Circle 266 on Inquiry Card

Intelligent Solution MAKES Dumb Printers *SMART.*



Use any of these printers with your computer.

THE INTEGRATOR ELIMINATES CHANGE.

THE INTEGRATOR—A Z80-based interface board—connects these printers to any computer with an RS-232 or Centronics parallel I/O port.

- **Diablo M-630 with Qume or Diablo interface.**
- **NEC 3500 Q/D, 5500 Q/D, 7700 Q/D.**
- **Qume Sprint 3 & Qume Sprint 7 with 13-bit interface.**
- **Fujitsu SP830. HyType II.**
- **Ricoh RP 1600.**

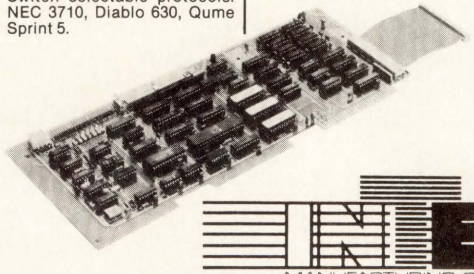
And gives you these bonus features:

- Optional 16K or 48K RAM.
- 16 baud from 50-19, 200—hardware/software selectable.
- RS-232, Centronics Parallel, IEEE ports, Current Loop.
- Switch selectable protocols: NEC 3710, Diablo 630, Qume Sprint 5.
- 24 switch selectable functions.
- Auto bi-directional printing with optimized thruput.
- Sheetfeeder and graphics modes.
- Auto proportional spacing and tab setting.
- Sheetfeeder and graphics modes.
- Auto proportional spacing and tab setting.
- Upgradable to latest software.
- Complete word processing features, standard.
- Supports optional front panel.

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Intersell added THE INTEGRATOR to the NEC Spinwriter. Since then, this successful, value-added printer has enabled the sale of the SELLUM I "with satisfaction guaranteed", to dealers and systems integrators.

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The INTEGRATOR is answering a vital need for you. Find out how THE INTEGRATOR will solve your programmable interfacing problems with this intelligent solution. Intek offers the service and support you require to develop private labeling, licensing agreements, and custom protocols. Call Garrick C. Colwell, VP Marketing, today at (408) 946-9041.

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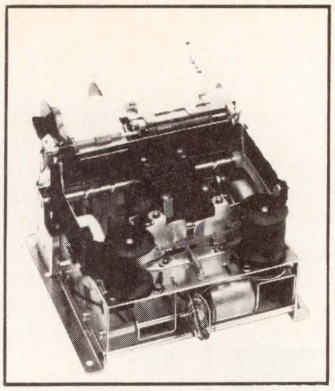
CIRCLE 59 ON INQUIRY CARD

WESTREX

DOT MATRIX PRINTERS

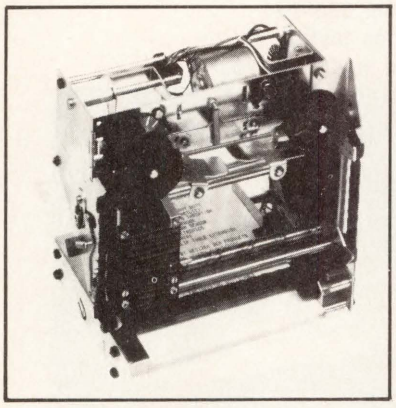
800 SERIES

INTRODUCING OUR NEW FAMILY OF COMPACTS



MODEL 820
SPLIT PLATEN PRINTER

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- Five Line Validation
- Paper-Supply and Take Up
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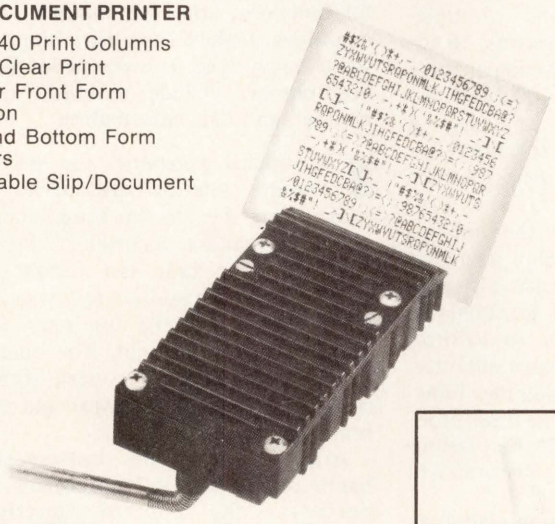


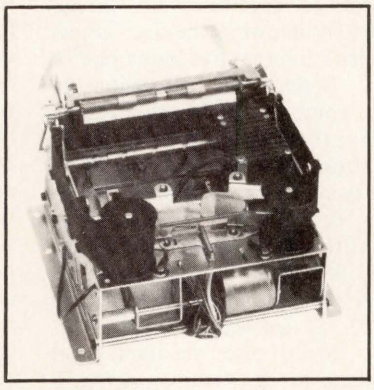
WESTREX 800 Series of alphanumeric bi-directional printers include split platen printers, flat bed slip/document printers and 51 to 96 column journal printers in a variety of standard models to suit a wide spectrum of OEM applications. All WESTREX 800 Series printers utilize the same simple, reliable drive system, head position sensors, ribbon transport mechanism and other quality tested components for maximum cost effectiveness.

Basic models illustrated on this page are obtainable with various options to suit your application needs. Data sheets with technical specifications for each of these products are available upon request.

MODEL 840
SLIP/DOCUMENT PRINTER

- Up to 40 Print Columns
- Large Clear Print
- Side or Front Form Insertion
- Top and Bottom Form Sensors
- Adjustable Slip/Document Stop





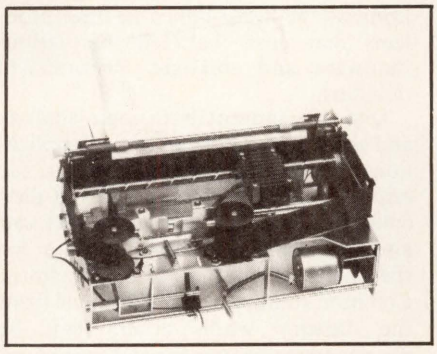
MODEL 850
JOURNAL PRINTER

- 51 Print Columns
- Integral Paper Supply Holder
- Easy Top Paper Insertion
- Document Validation Capability

AT THE HEAD, THEY'RE CLASS!

MODEL 801
LOW PROFILE, LOW WEIGHT, PRINT HEAD

- 7 Needle Vertical Array
- Low Power Consumption
- 100% Duty Cycle
- 100 Million Character Life



MODEL 880
JOURNAL PRINTER

- Up to 96 Characters Per Line @ 12 CPI
- Bi-Directional Printing
- Standard & Graphic Feed
- 576 Print Dots Per Line

For full details, write or call us

Litton **WESTREX OEM PRODUCTS**

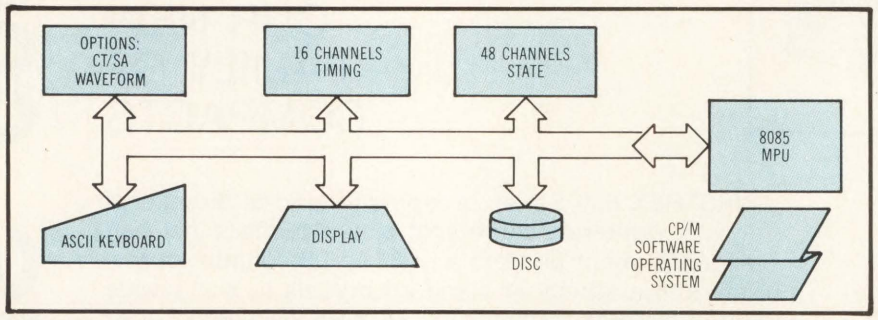
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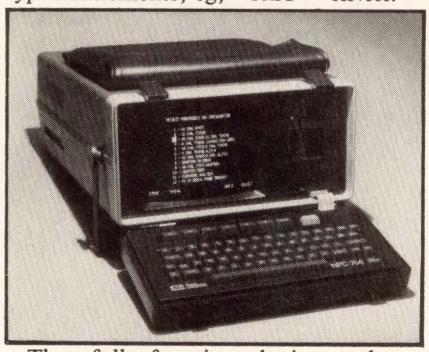
TEST & MEASUREMENT

Access to internal computer expands versatility of 64-channel logic analyzer



Features of NPC-764 Logic Analyzer. Twelve operating modes are available. User has access to device CPU

Offering more utility than typical logic analyzers, the 64-channel NPC-764, from Nicolet Paratronics Corp, can be used as a basic development system, automated data acquisition system, IEEE 488 controller, and personal computer in digital product design, simulation, development, production, and field service. Such versatility was accomplished by allowing the user access to the device's internal 8085 based microcomputer. Besides an expansion in capability, computer access also results in a machine that is familiar to engineers with a strong software rather than hardware background. Engineers with a software orientation should feel comfortable with the full ASCII keyboard, 9″ (23-cm) CRT, 80-char x 25-line display and CP/MOS. Menu driven with six software directed softkeys, the device also accommodates typed statements, eg, "TRIG = H375H."



The full function logic analyzer system consists of two independent logic analyzers tied together with a user accessible CP/M compatible software operating system. 300k of storage on an internal 5.25″ (13.34-cm) floppy are available for programs or analyzer setups and collected data. The analyzer is also compatible with the company's present options and accessories such as an analog waveform analyzer, counter-timer/signature analyzer, and dedicated probes for the analysis of microprocessors and serial data channels. The unit also provides both IEEE 488 and RS-232 peripheral interfaces. Device components are shown in the diagram.

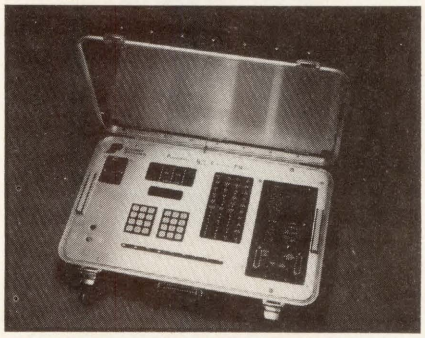
Logic analysis functions are ROM based. These menu directed functions include 48 channels of logic state analysis with 16 levels of triggering, auto restart for branch analysis, and multiple-clocking for multiplexed systems; 16 additional channels of logic timing analysis with sample rates up to 100 MHz for high speed hardware analysis; a 100-MHz counter-timer/signature analyzer for systems performance monitoring; and RS-232 RECEIVE/TRANSMIT capability for the analysis of serial data. Logic analysis capabilities include 12 basic measurement functions of which 7 are standard. The remaining functions (waveform, counter, timer, and signature analyzer) are offered as optional plug-ins. Functions can be menu-linked to trace problems that cross between the various hardware and software measurement domains.

Disc can support both logic analysis and general purpose computing applications. When used with the analyzer, for example, up to 64 test setups and data collections can be stored. The user can also execute disc-resident routines for special processing and display functions. Common routines will be available from the factory while others can be developed by the user for customized applications. When used as a personal computer, the device can execute CP/M compatible software including BASIC, FORTRAN, Pascal, 8085 Assembler, and Text Editor.

Through the product's IEEE 488 interface, the device can also operate as a full-fledged bus controller. Using standard IEEE 488 commands, the NPC-764 can control external test and measurement functions whether or not the 12 internal analysis functions are part of the automated test setup. The device can be expanded to include another disc for a total storage of 1M byte, an RS-232 compatible P/ROM programmer, an RS-232 compatible emulator, and an assembler/compiler. **Nicolet Paratronics Corp,** 2140 Bering Dr, San Jose, CA 95131.

Circle 267 on Inquiry Card

Universal qualifier simplifies testing of storage module drives



Disc drive qualifier. Two keypads, one for functions, other for numeric quantities, replace customary binary switch array used to code entries for head number, cylinder number, address, and data information

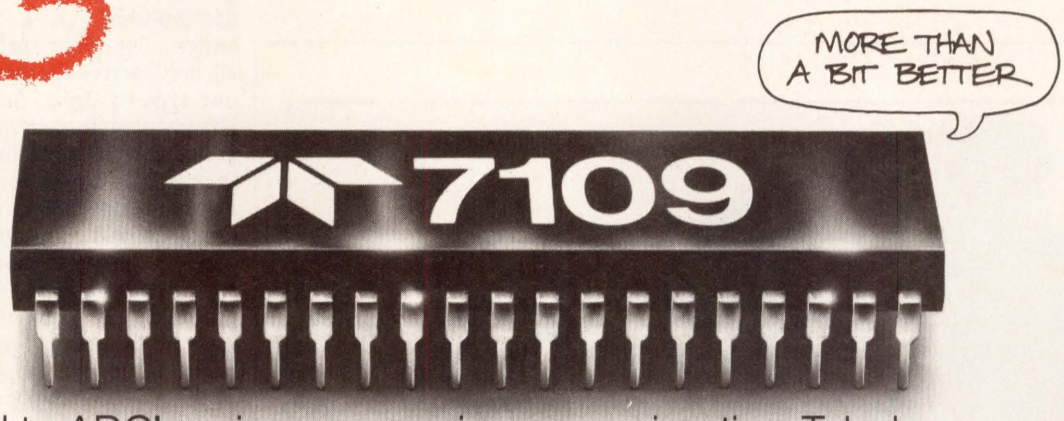
Nontechnical personnel can perform complex tests on disc drives and packs using the PM 4000 programmable disc drive qualifier, according to Pioneer Research. The unit can format disc packs, flag and readdress faulty sectors, and greatly reduce the time required to perform head alignment. The qualifier can be programmed to work with all storage module drive (SMD) and most non-SMD formats.

Architecture of the instrument is based on an 8085 microprocessor that performs the control functions. Operating programs, format instructions, and preprogrammed diagnostic routines are resident in 8k of P/ROM (expandable to 24k). Storage for keyboard entered programs and the error count and pass count registers is handled by 2k RAM. A second area of RAM, normally 1k but expandable to 2k, called the DMA RAM, is provided, since the 8085 cannot operate in real time at normal disc data rates. During normal write to disc operations the microprocessor loads a sector of data into the DMA RAM; this is then transferred to the disc in real time.

When a disc pack is being formatted, the DMA RAM data remain fixed except for incrementing the address for each sector; no time is lost between sectors.

(continued on page 106)

The Amazing ~~12~~ 13-Bit ADC



Compared to ADC's using successive approximation, Teledyne Semiconductor's integrating 7109 is truly amazing. Our 12-bit binary ADC not only interfaces directly with your microprocessor or data acquisition system but gives you a 13th sign bit free. So you'll get a lot better resolution when converting bipolar inputs.

Speaking of inputs, the 7109 features high impedance with low leakage current of 1 pA and high sensitivity of 100 μV/LSB. As a result, there's no problem of overloading by your source.

What's more, the 7109 has an auto-zero system that eliminates zero offset adjustments and compensates automatically for drift caused by external components. Also this dual-integrating ADC does away with sample-and-hold amplifiers, along with their inherent inaccuracies.

There's more to relish from the single-chip CMOS 7109. Like internal reference, no missing codes, excellent differential non-linearity, and lower power requirements – only 20 mW.

On the output side, the 7109 provides byte organized 3-state outputs for direct connection to an 8- or 16-bit bus. For simple serial data transmission, a handshake mode allows direct connection to industry-standard UART's.

For more amazing information about the 7109 or our other data conversion products, contact us today. You'll be amazed.

Teledyne Semiconductor, Dept. B4, 1300 Terra Bella Avenue, Mountain View, CA 94043; phone (415) 968-9241, ext. 241. Dept. B6,

TELEDYNE SEMICONDUCTOR

The Data Conversion Specialist

CIRCLE 61 ON INQUIRY CARD

TEST & MEASUREMENT

To reload this redundant data, the microprocessor can access a portion of the DMA RAM while a write is in progress. This allows the address to be incremented while the disc is being written with the data field. A complete track can be formatted for each revolution of the disc.

Another RAM, called the Format RAM, is the same length as the DMA RAM but is 4 rather than 8 bits wide, and is clocked in parallel with the DMA RAM. It can store up to 16 formats and is uploaded from a format table. The Format RAM identifies, byte by byte, the type of data, such as preamble, label, data, gap, or error correcting code, in the DMA RAM. Its output is also used to enable the write amplifier at the appropriate time.

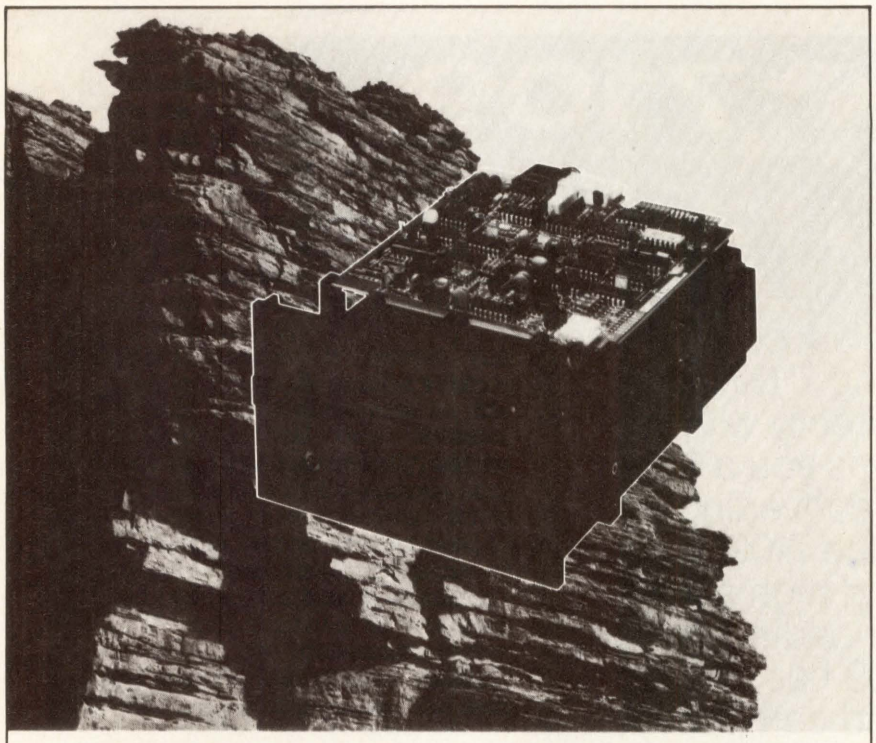
The instant selection of any preprogrammed format parameters in P/ROM is accomplished via a hex thumbwheel switch. The same qualifier can exercise all units where the user has more than one type of drive. Sector formats not already contained in P/ROM can be programmed by setting the unit's Drive ID thumbwheel switch to zero. This action keys the instrument to accept instructions that will complete the desired format. The alphanumeric display indicates requests for data, which are keyed in via the keypad. The qualifier is ready to format the disc pack when the keying sequence is completed. An 80M-byte disc pack can be completely formatted in 70 s, approximately.

Head alignment is speeded and simplified because the qualifier's microprocessor does all calculations for this procedure in real time. Reversal switching is done automatically, and the null signal is read by a 4-quadrant ADC. The converter, through software, drives the read data LEDs on the front panel to give a nonlinear analog indication of head position. The head is adjusted so that a minimum number of LEDs is on and centered. The alphanumeric display then indicates total effective misalignment directly in microinches. The need for calculations and judgment of magnitude equalities is eliminated.

The qualifier has a 9600-baud RS-232-C interface for connection to a printer or CRT terminal. LED indicators provide status signals from the drive, including unit select/ready, seek end, on cylinder, seek error, heads loaded, write protect, drive fault, and high temp. Thirty test points are also available. A and B cable connectors for flat or round cables, and universal head alignment cable connectors are provided.

Housed in an attache style carrying case, the qualifier measures 14 x 21.5 x 6″ (36 x 54.6 x 15 cm) and weighs 25 lb (11 kg). Power requirement is 100 W at 100-115/230-240 Vac, 50-60 Hz. Single quantity price is $5950. **Pioneer Research,** 1745 Berkeley St, Santa Monica, CA 90404.

Circle 268 on Inquiry Card



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Unique DC Spindle Drives feature our continuously-running brushless DC motor whose typical life expectancy is over 10,000 hours. Rock-stable, no electrical noise will interfere with the integrity of your data.

Superior Chassis features fiberglass reinforced polyester (FRP) which, unlike aluminum, won't stretch with heat. Extra-rugged and precision molded, the unit also has a shield to insulate the head from outside interference.

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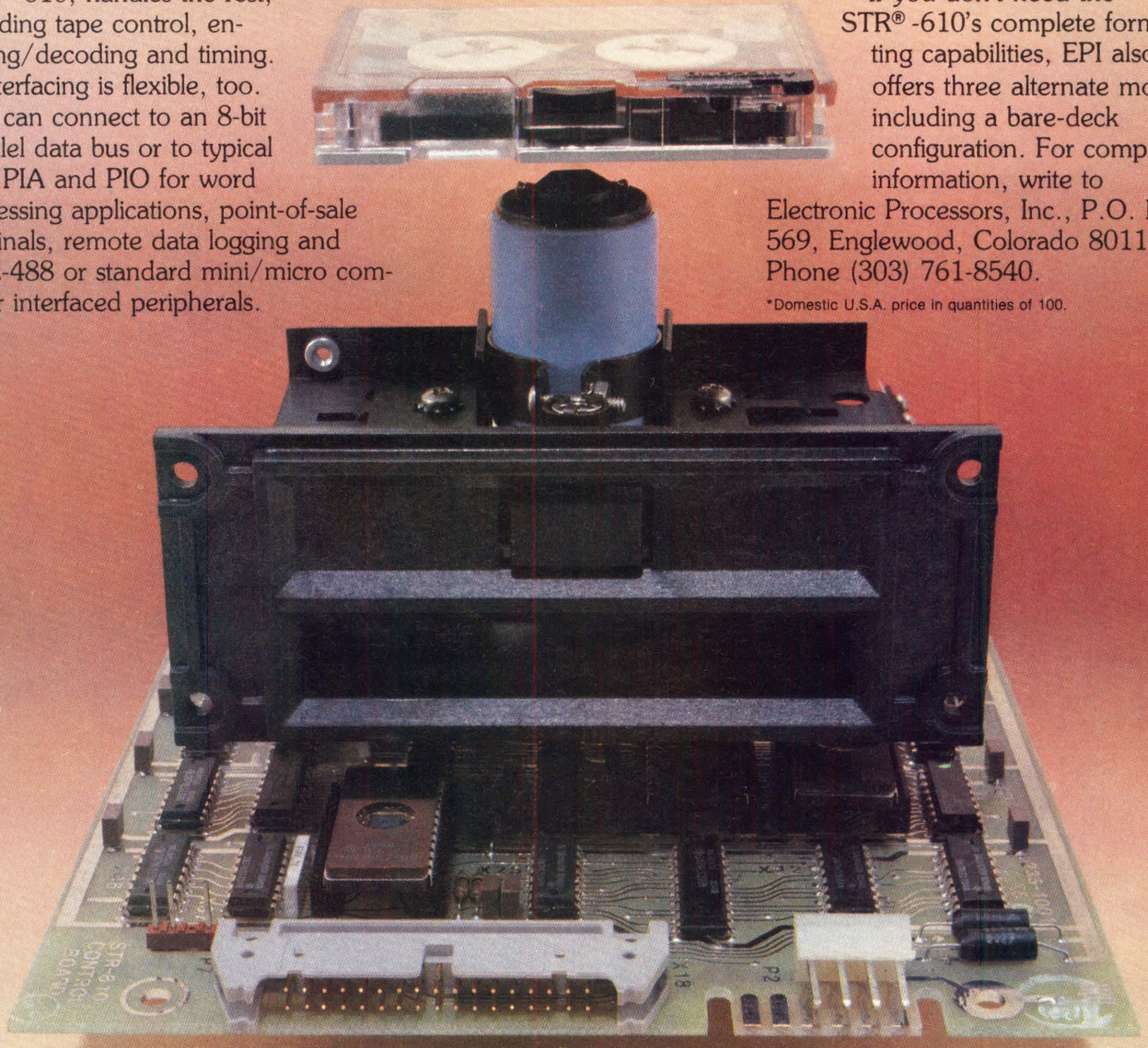
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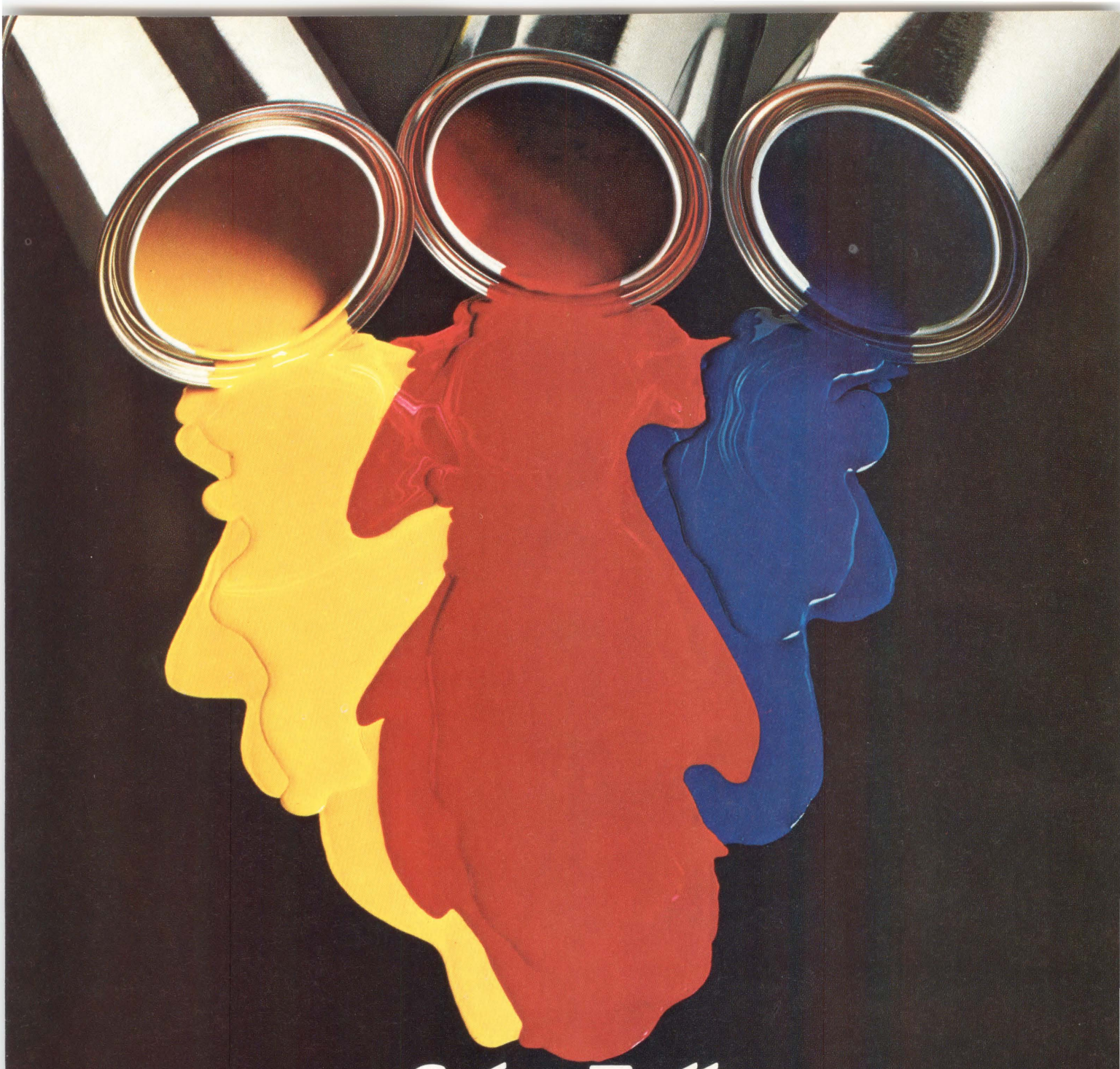


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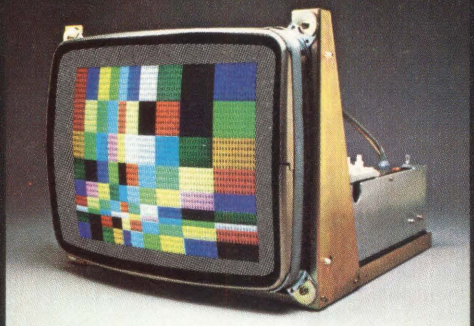


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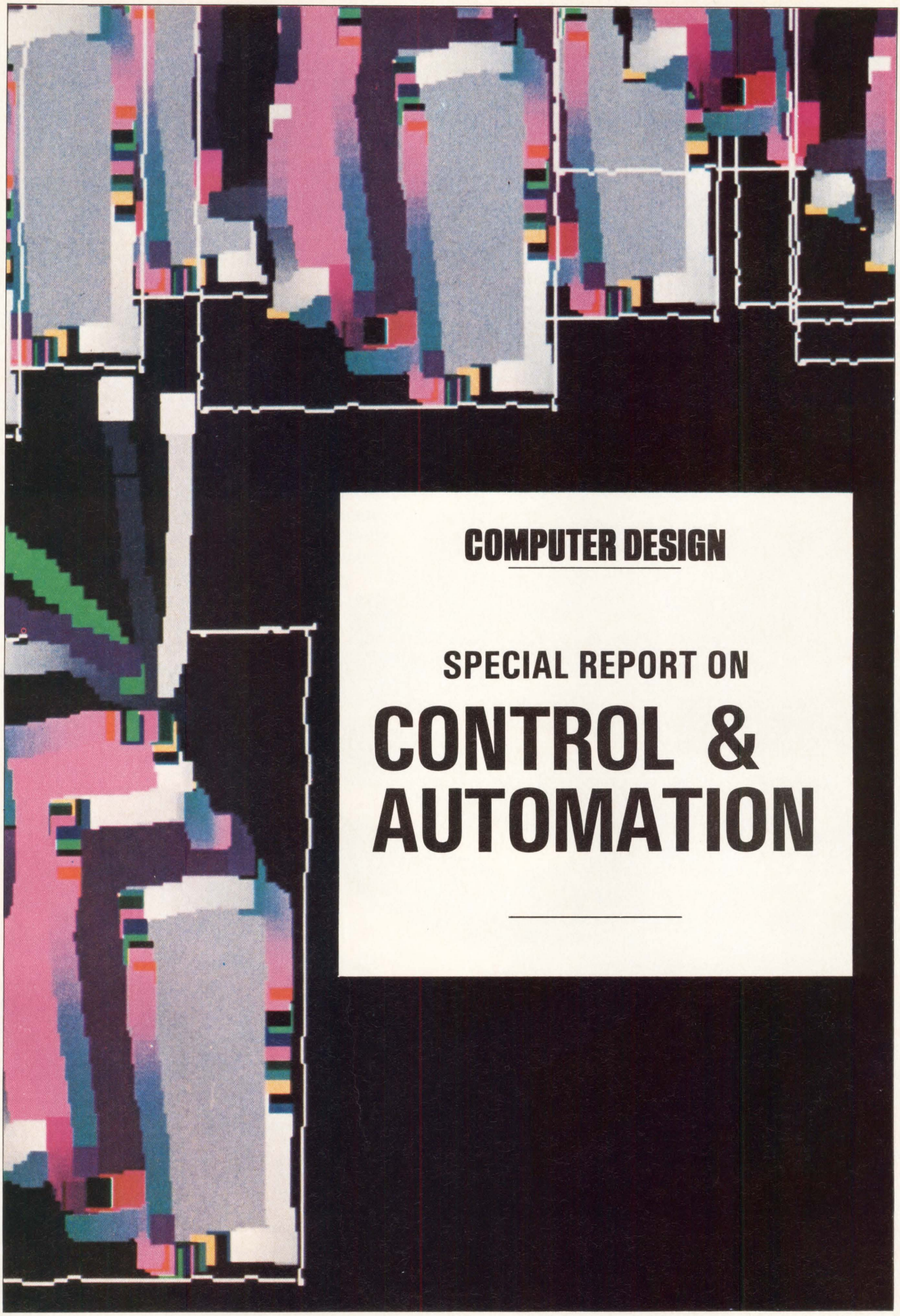
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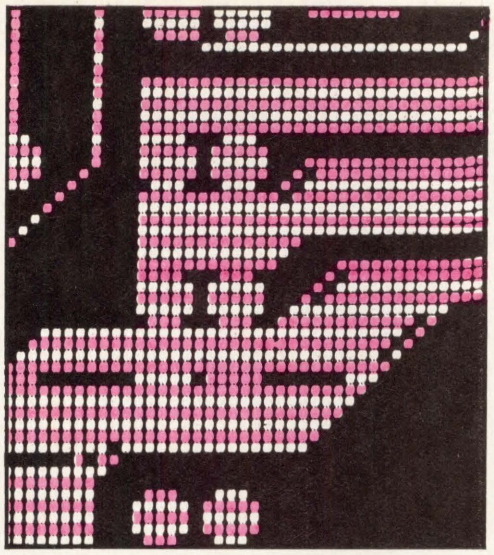
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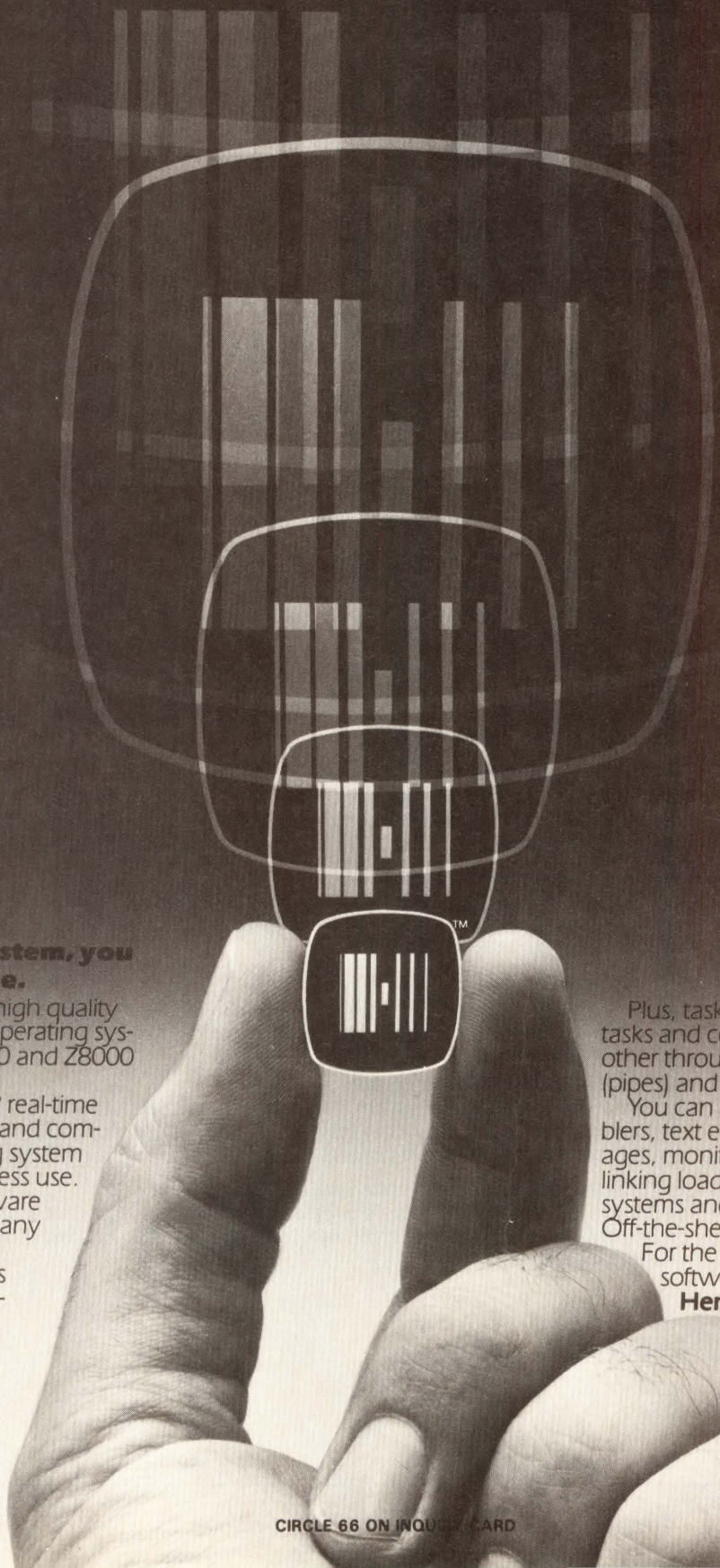
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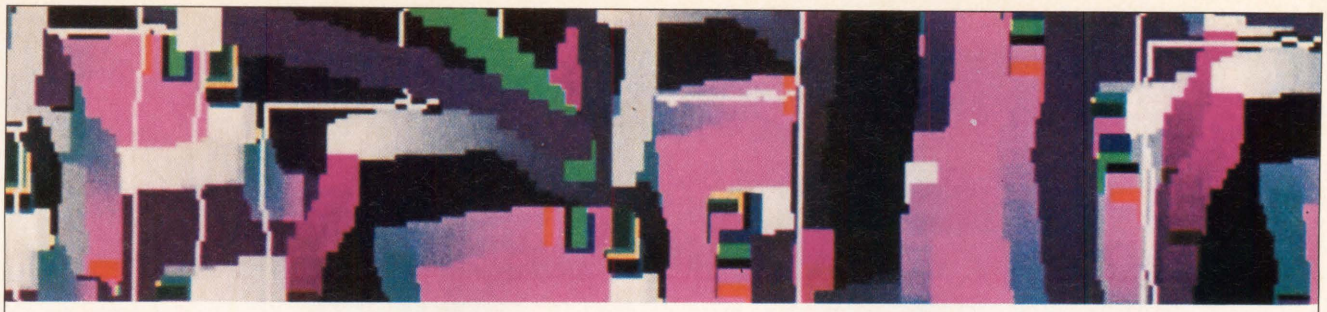
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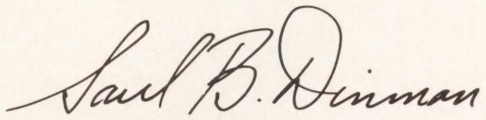
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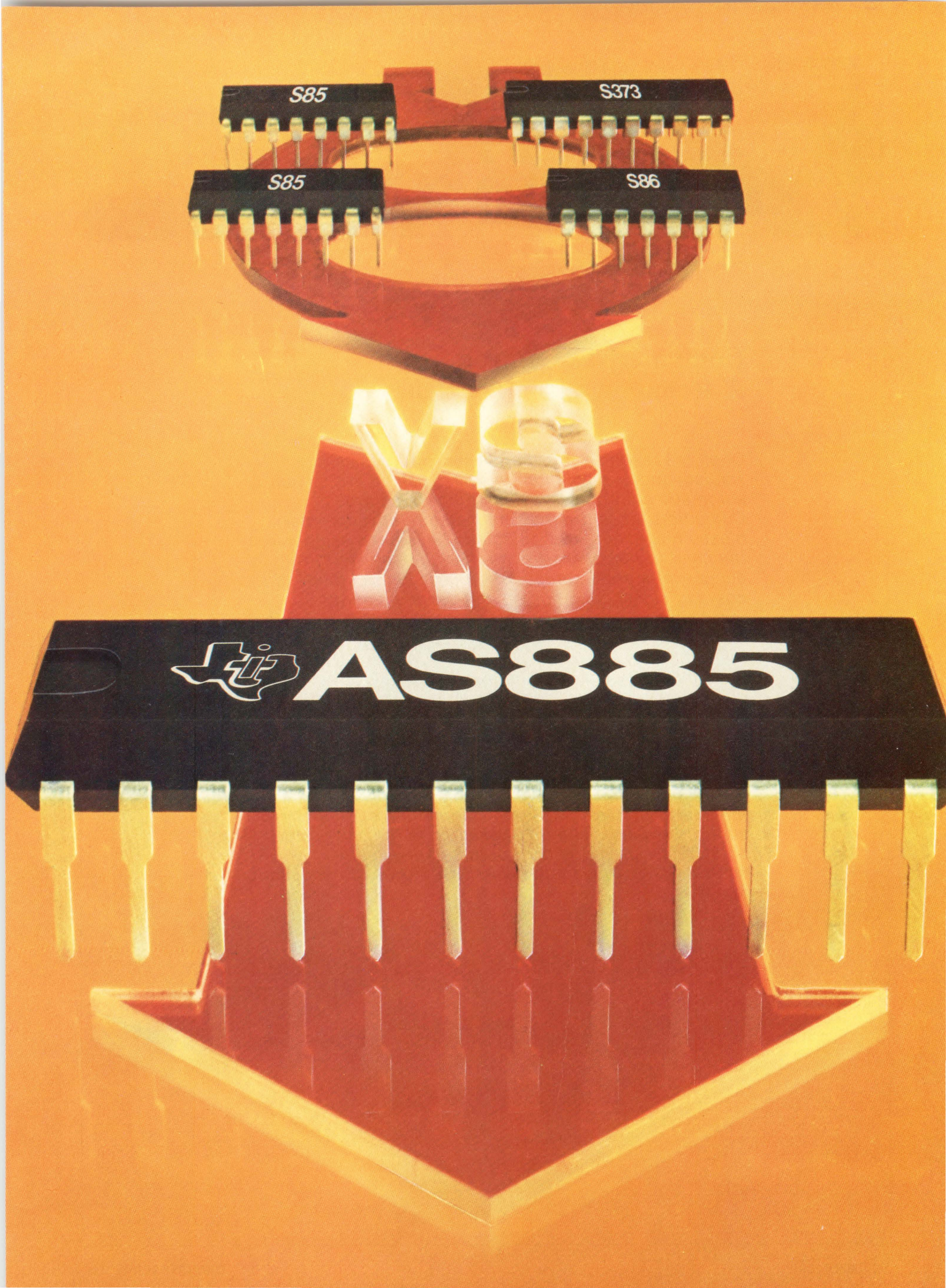
Computerized control: A technology finally catches up

Of all the technologies that have benefited from the semiconductor revolution, few have gained more than automatic control, particularly process control. Computerized control has stagnated relative to other blossoming digital technologies. It has been hampered by the need to timeshare a controller, thereby amortizing its costs over a great number of process control loops; the costs of signal conditioning and cabling; and the requirements for manual backup systems that had to be completely redundant controllers because of the nature of the timeshared beast.

At last, it appears that hardware technology has put computerized control back in step with its sister technologies. The greatest impact in control technology is probably going to come from low cost distributed intelligence. Intelligent transducers, intelligent conversion devices, intelligent controllers, and local area network technology are now providing economical solutions to all of the nasty problems that have plagued the computerized control industry since its awakening in the early sixties. The ultimate dream of the control theorist—adaptive control—also appears to be well on the way to economic reality.



Saul B. Dinman
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S85
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AS885

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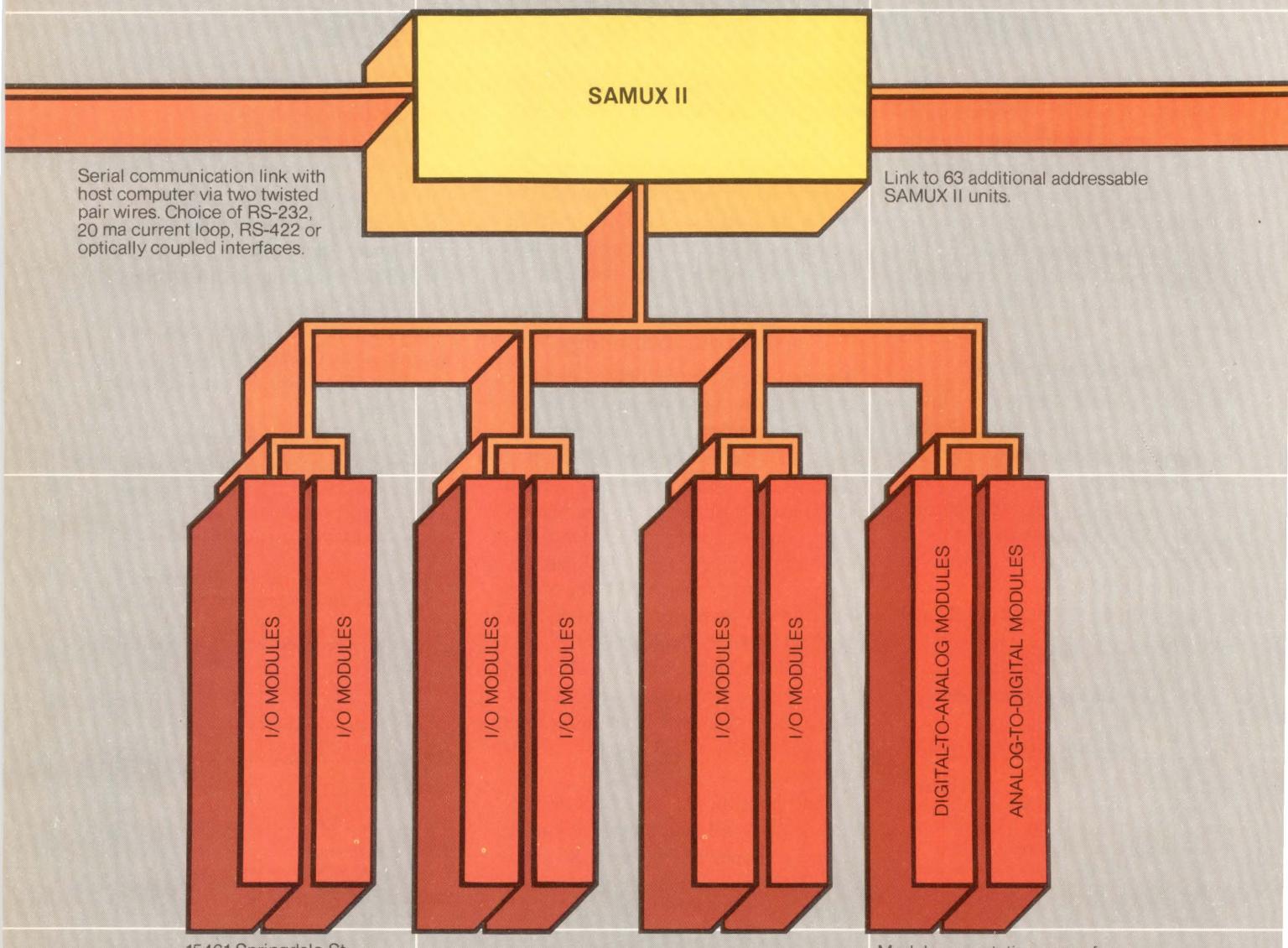
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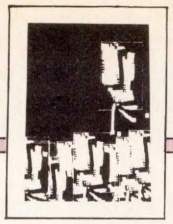
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DIGITAL TECHNOLOGY IN PROCESS CONTROL

The 20-year evolution of digital technology in process control has culminated in a combination of today's distributed control philosophy with yesterday's shared function approach

by Thomas J. Myron, Jr

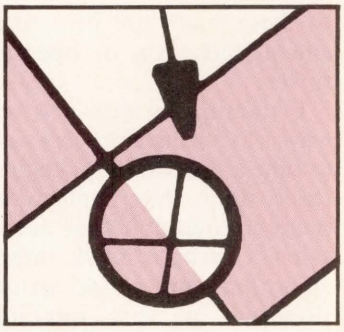
When digital computer technology was first applied to industrial process control in the early 1960s, the goal was to bring as many functional loops under direct digital control as possible. Essentially, this meant bringing a measurement—be it rate of flow, temperature, pressure, or chemical composition—into a computer from a field location. The computer then performed a standard mathematical operation on the difference between the measured value and a desired value, or set point. Computer output operated a device, such as a valve or speed control, to reduce the deviation between measured and set point values. In this role, the computer became a direct replacement for the traditional analog feedback controller.

Over a span of more than three decades, conventional analog controllers developed many features that made them easier to use, while industries accumulated considerable experience in tuning and applying these controllers. Digital computers supplied the newest technology and a virtually unlimited calculating capability, but this breakthrough exacted a price. At the regulatory level, process engineers and operators were losing the flexibility and familiarity that they had acquired over many years of analog control.

Since most digital computers and computer specialists in those early years came from an electronic data processing environment, data processing and industrial process control were united in a shotgun marriage.

Thomas J. Myron, Jr, is manager of process management and control design at The Foxboro Company, 38 Neponset Ave, Foxboro, MA 02035, where he is responsible for the design and start-up of advanced control systems. Mr Myron holds a BS in chemical engineering from Rensselaer Polytechnic Institute, attended St John's University Law School, and undertook graduate studies in engineering management at Northeastern University.

Today, for the most part, process control engineers and operating engineers have reclaimed their dominance by establishing the directions that suppliers must follow, both in developing control equipment and in designing its operator interface.



Security and familiarity are major concerns

At the regulatory control level, an overriding concern for operational reliability called for a variety of backup mechanisms between the computer and the process (Fig 1). General levels of operator intervention, in the event of computer failure, were auto/manual takeover, set point tracking, and supervisory control. Auto/manual takeover allowed the operator to manipulate the process directly in the manual mode, while in the automatic mode a signal from the computer passed through the station to the process.

With set point tracking devices, the set point tracked the process measurement whenever the computer was running. In the event of a computer failure, the backup device would take control at the last set point and measurement values. An auto/manual function was also available, thereby allowing three levels of process control: direct digital control, local control, and manual intervention. With supervisory control, in contrast, the computer provided a set point only to the hardware controller, which was responsible for all control functions.

Regardless of backup mode, new problems arose. Backup reduced the advantage of direct digital control over conventional hardware. Cabling was also a difficulty: For each computer and backup device to have all the information required, a substantial amount of hardwiring was needed between devices. Furthermore, when the operator had two different interfaces and one

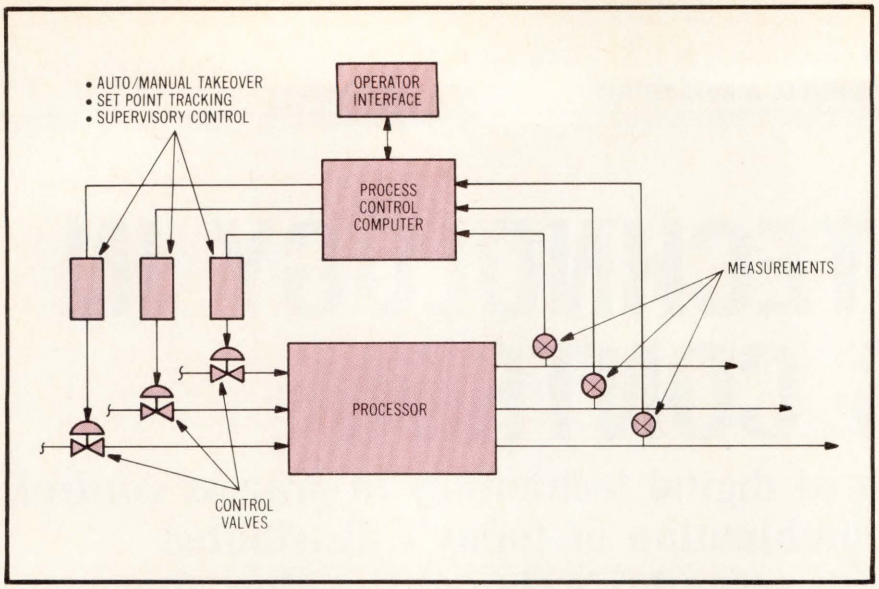


Fig 1 Direct digital control with hardware backup. Three types of backup mechanisms protect against computer failure: auto/manual takeover, set point tracking, and supervisory control

of these might not be used for months at a time, ease and effectiveness of operator control were bound to suffer.

Unfamiliarity with new control devices and the new ways of viewing a process were also a problem. In trying to tune a process loop, engineers were often totally confused when they applied familiar tuning rules. They spent considerable time unraveling ground rules for the velocity proportional integral and derivative (PID) algorithm, and raised serious questions about inconsistencies in what was intended as a "standard" method. Ideally, implementation of a standard algorithm should not depend on the device or technology used. In particular, it should not be necessary to consult one control specialist for digital algorithms and another for algorithms in dedicated hardware. A fundamental decision (at least with respect to The Foxboro Company) was made at this point: Implementation of algorithms at the regulatory level should be as consistent as possible, regardless of the device or method used.

The value of the noninteracting PID algorithm also came under attack from the standpoint of real world process characteristics and user application needs. Noninteracting PID can achieve twice the performance of interacting PID; however, most industrial processes are nonlinear over normal operating ranges and may require external feedback to prevent saturation or windup. Where external feedback is used in a noninteracting controller, the effective gain is

$$K_c = \frac{100}{P}\,\frac{1 + (D/I)}{1 - (D/I)}$$

This means that when D equals I, the effective gain increases without limit and, when D exceeds I, the effective gain is negative, reversing the action of the controller. Neither condition is desirable. The objective, instead, is a controller for which D can never equal or exceed I. The interacting controller defined by Eq (2) of the Panel, "Conventional feedback control algorithm," achieves that goal, increasing control loop stability at the expense of optimal response to process perturbations. Since nonlinearity of the process prevents optimal tuning over normal load variations, opting for loop stability appears to be the best choice.

Distributed control systems extend familiar methods

Transfer of information between the control computer and the backup device was cumbersome, at first; depending upon the number of control loops that the computer was scanning and the rate at which it scanned each loop, information transfer could slow response time considerably. The economic incentive to implement higher levels of control and the need for fast data transfer motivated the design of systems that implemented more recognizable process control combined with fast, secure process communication.

A distributed control system is a collection of devices for process control, operator interfacing, and process input/output that connect by means of a communication link. Fig 2 shows a typical distributed control system in which each device cluster is usually dedicated to a particular operating region of the plant or mill. The number and type of devices in each cluster depend on the application and the end user's operational needs. In this example, clusters B and C have operator workstations, but clusters A and D do not. Because they have communications capability, however, A and D can be located at substantial distances from the operator interface. Terminating field wiring locally (eg, at D) and establishing a communications link with the operator lowers costs.

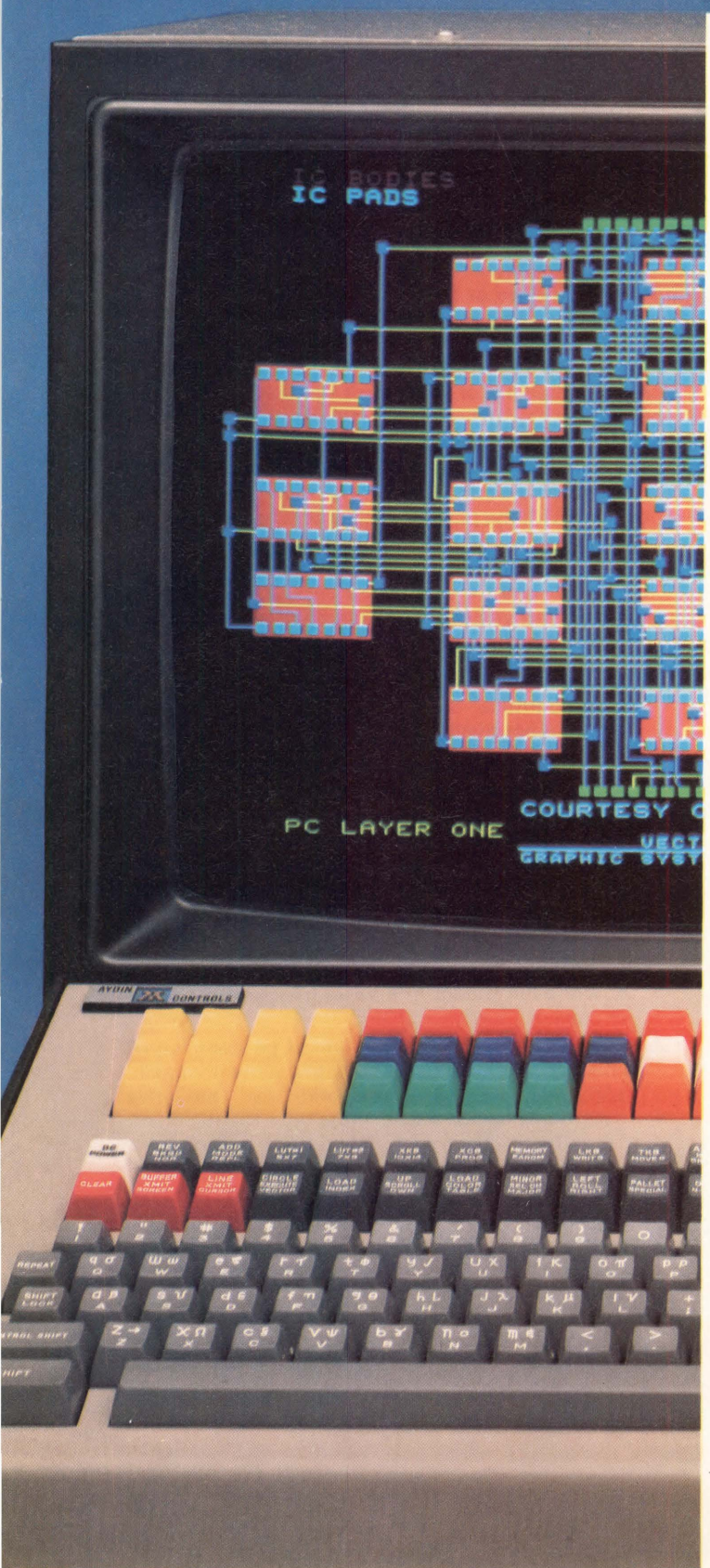
Some users are concerned with communication redundancy. Most redundant systems offer many choices, ranging from a single communication link [eg, Fig 2, 1(a) only], through backup of this link [1(b)], to redundant communication paths [2(a), 2(b), and 3(b)]. Again, the level of communication security and redundancy depends on the application. Today more than twenty manufacturers supply distributed control systems.

Shared devices reflect a significant change

Perhaps the most significant changes at the regulatory control level involve use of *shared display* and *shared control* devices. Shared displays are microprocessor based devices that contain many display templates in software. Templates can be selected, configured, and arranged on a video screen to meet the control and operational objectives of a plant or mill. Historically, plant operators interacted with discrete instruments, switches, and alarms located on so-called panel boards. In a large plant, the panel board could measure 100′ (30 m) or longer. The plant operator could perform certain tasks by manipulating knobs and switches on the instruments, and also observe the behavior of individual loops. Operators could transfer control between automatic and manual modes, change set points, vary

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Conventional feedback control algorithm

A version of the ideal proportional integral and derivative (PID) algorithm can complement regulatory control in a digital computer.

$$m = \frac{100}{P}\left(e + \frac{1}{I}\int e\,dt - D\frac{dc}{dt}\right) \qquad (1)$$

where

- m = controller output (a positional value from 0% to 100%)
- $\frac{100}{P}$ = controller gain
- I = integral time (minutes)
- D = derivative time (minutes)
- e = error (actual measurement vs desired measurement)
- c = actual measurement

Sometimes the $-D\frac{dc}{dt}$ term of Eq (1) is written

$$+D\frac{de}{dt}$$

The derivative component responds to changes in set point as well as to changes in measurement. In most modern controllers, the derivative component is limited to the rate of change in measurement only, as shown in Eq (1).

The first PID analog controllers for the process industries were pneumatic. With them, the ideal algorithm described by Eq (1) was just that: an ideal. Although the I and D settings in Eq (1) were independently adjustable, mechanical difficulties precluded manufacturing a device that could implement the ideal equation. The working PID equation that takes into account the interaction of all the control modes, proportional (P), integral (I), and derivative (D), is

$$m = \frac{100}{P}\left(1 + \frac{D}{I}\right)\left[e + \frac{1}{I + D}\int e\,dt - \frac{I}{(1/I) + (1/D)}\frac{dc}{dt}\right] \qquad (2)$$

where all terms are previously defined. The PID algorithm described by Eq (2) is termed "interacting," whereas the Eq (1) algorithm is "noninteracting."

Not until the electronic era could Eq (1) be implemented in standard hardware; now virtually all electronic controllers can implement the noninteracting equation. Using the performance (described by Shinskey) of integrated measurement error per unit process load change, it can be shown that the "ideal" Eq (1) algorithm can provide twice the performance of the interacting algorithm described by Eq (2).

With the ideal algorithm as a base, the digital computer equivalent was developed by differentiating Eq (1) with respect to time, and converting the resulting equation to a difference (Δ) equivalent

$$\Delta m = \frac{100}{P}\left[\Delta e + \frac{\Delta t}{I}e_n - \frac{D}{\Delta t}\Delta(\Delta c)\right] \qquad (3)$$

where

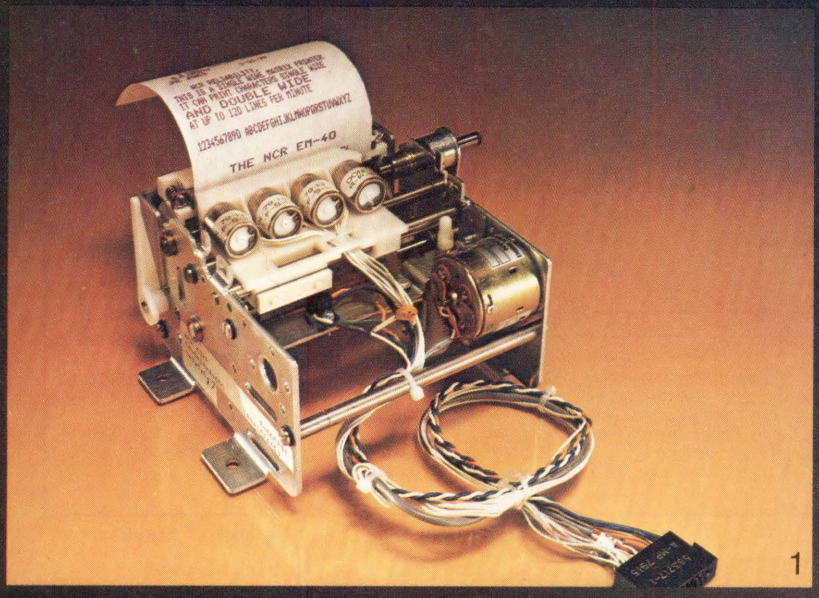
- Δm = change in controller output
- Δt = sampling or scan rate
- Δe = change in error since the last scan, $e_n - e_{n-1}$

The algorithm described by Eq (3) is sometimes referred to as the "velocity" algorithm, while that described by Eq (1) and Eq (2) is the "positional." Here velocity and positional advocates divide sharply.

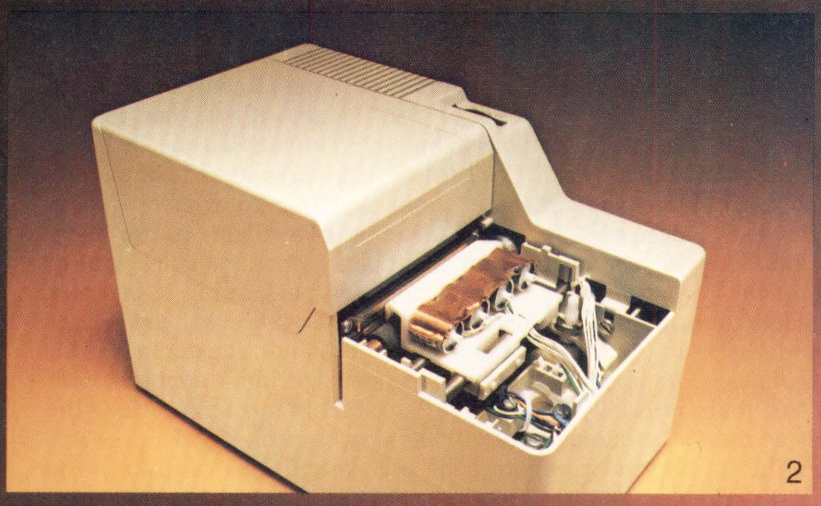
Initially, nearly all digital computer control devices intended for use at the regulatory level could implement the Eq (3) algorithm. The velocity, or incremental nature, of this algorithm made actual control takeover very secure, since the algorithm output had only to increment or decrement from where the final operator was at that point. Another feature of the velocity algorithm was its relative insensitivity to computer failure. On a loss of pulse output, for instance, the valve or final operator maintained its last position. With the positional algorithm, a balancing or initialization to where the final operator was at the time of failure is essential if the process is not to be "bumped," and the final operator position changed. However, the velocity or incremental algorithm has some drawbacks.

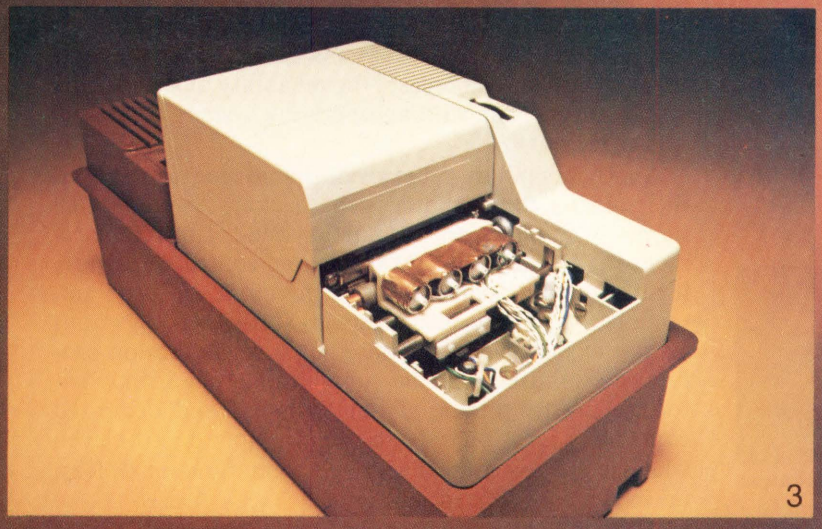
- Various combinations of the PID algorithm, such as proportional only or proportional plus derivative, are not available.
- Limits cannot be placed on the final operator position, except mechanically at the device itself.
- "Auctioneering" between controllers, where a single final operator is available to many controllers, one at a time (sometimes called auto select), is not available.
- Integral saturation (or windup) is not intrinsically available, since the input of the algorithm is a string of pulses telling the valve to move up or down, even though the valve may be fully open or closed.
- Loop tuning procedures have to be completely changed. For example, the actual derivative gain according to Eq (3) is the ratio $D/\Delta t$. Derivative gain of analog controllers must be in the region of 10 to be effective and stable. For the derivative gain of a typical direct digital control loop using the velocity algorithm to be 10 would have to be either coincidence or the careful selection of Δt as an adjustable parameter. Consequently, derivative action is rarely effective with velocity PID algorithms implemented for direct digital control and almost never used.

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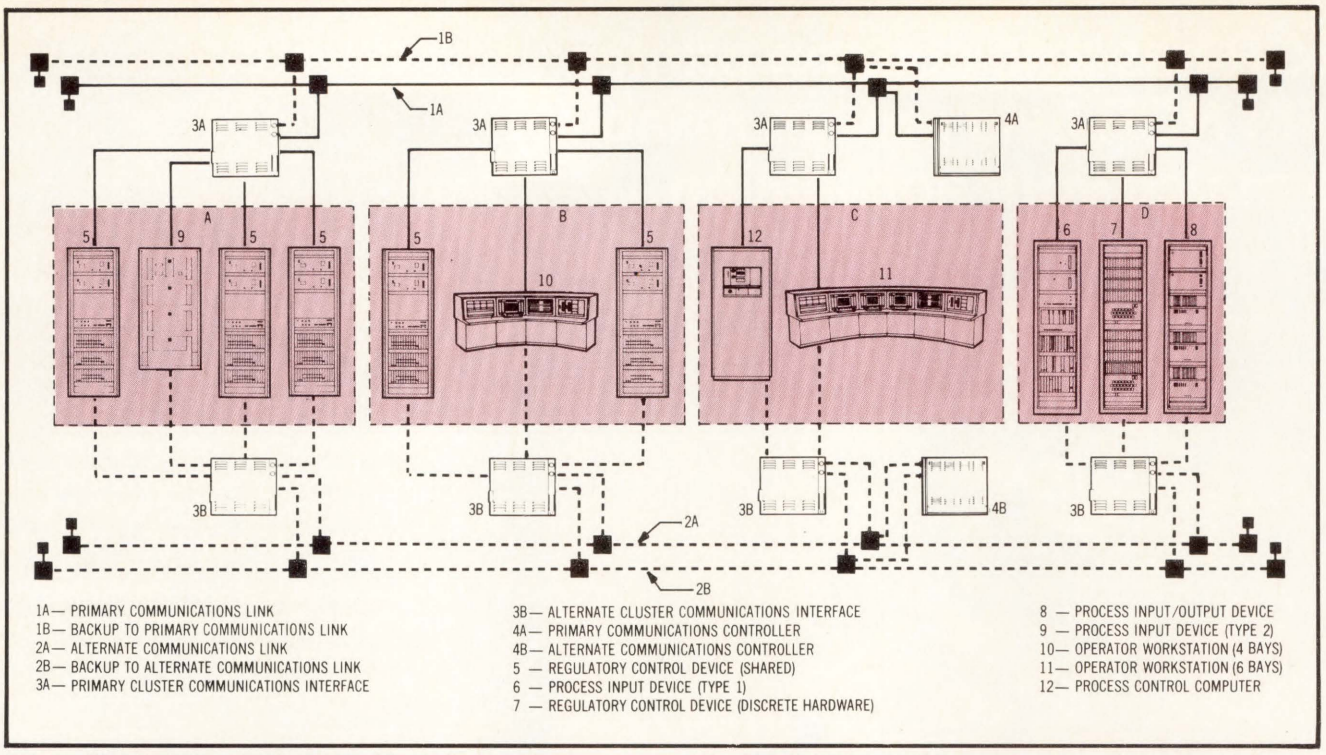


Fig 2 Distributed control system. Each cluster of equipment can control one region of plant or mill. Number and type of devices in cluster depend on cluster function

output limits and alarm points, and observe deviations between a measurement and its set point.

By stepping back from the panel, an operator could observe interaction among different loops. Moving back still further, he could observe the operation of an entire plant section. However, at large panel boards, it was difficult to see the status of the entire plant. Once the operator moved away from the panel, no control action could be taken; only observation was possible.

Fig 3 shows a section of a typical panel board. In contrast, Fig 4 shows the various display levels available to an operator in a shared display device. At the highest level, each of eight groups can have up to 64 faceplates, for a total capacity of up to 512 displays. As the operator pages down through the display levels at the keyboard, more and more detail becomes visible. This is analogous to stepping closer and closer to a panel board and narrowing one's field of vision. Eventually, the operator arrives at the loop access level. Discrete control tasks can be performed here, and the same observations can be made as with the analog instrumentation in Fig 3. Although the shared and discrete displays of Figs 3 and 4 are not identical, there is a similarity between them that supports the trend toward familiar ways of observing a process.

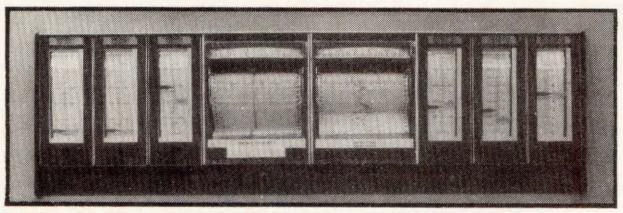


Fig 3 Analog control panel segment. Instruments monitor behavior of individual loops. Operator can observe entire plant section by stepping back from panel, but direct action is then impossible

Shared controller blends analog and digital techniques

From a process control viewpoint, one of the most exciting devices available is the shared controller, which contains a group of control algorithms that can be selected, configured, and interconnected as needed. It is sometimes difficult to see just where shared control fits into the range of tools available to control system designers. In fact, if the range of available control techniques varies from a simple, manual, analog control station to a digital computer performing a complex optimization algorithm, the shared controller is closer to the dedicated analog world than to the digital world. Its scan rate, the rate at which algorithms are processed, is usually fixed at 2 to 3 cycles/s, a rate approaching the continuous nature of analog control. (With a process control computer, the user specifies a scan rate.) The operating system resides in read only memory; parameters of a given algorithm can be changed, but its fundamental operation remains intact. This arrangement significantly increases the reliability of shared controllers over those with an operating system in random access memory.

Another similarity between shared controllers and their analog counterparts is the backup system, which normally involves an automatic, one-for-one replacement for at least a part of the shared control hardware, if not the entire controller. Furthermore, no programming language is needed. Instead, software connections similar to hardwiring are based on a configuration procedure established by the supplier. The algorithm set, too, is mostly analog. Finally, shared and dedicated controllers function only at the regulatory control level, whereas process control computers can function at least up to the coordinated unit level.

Although shared control has many characteristics of analog control, it has some important differences. For

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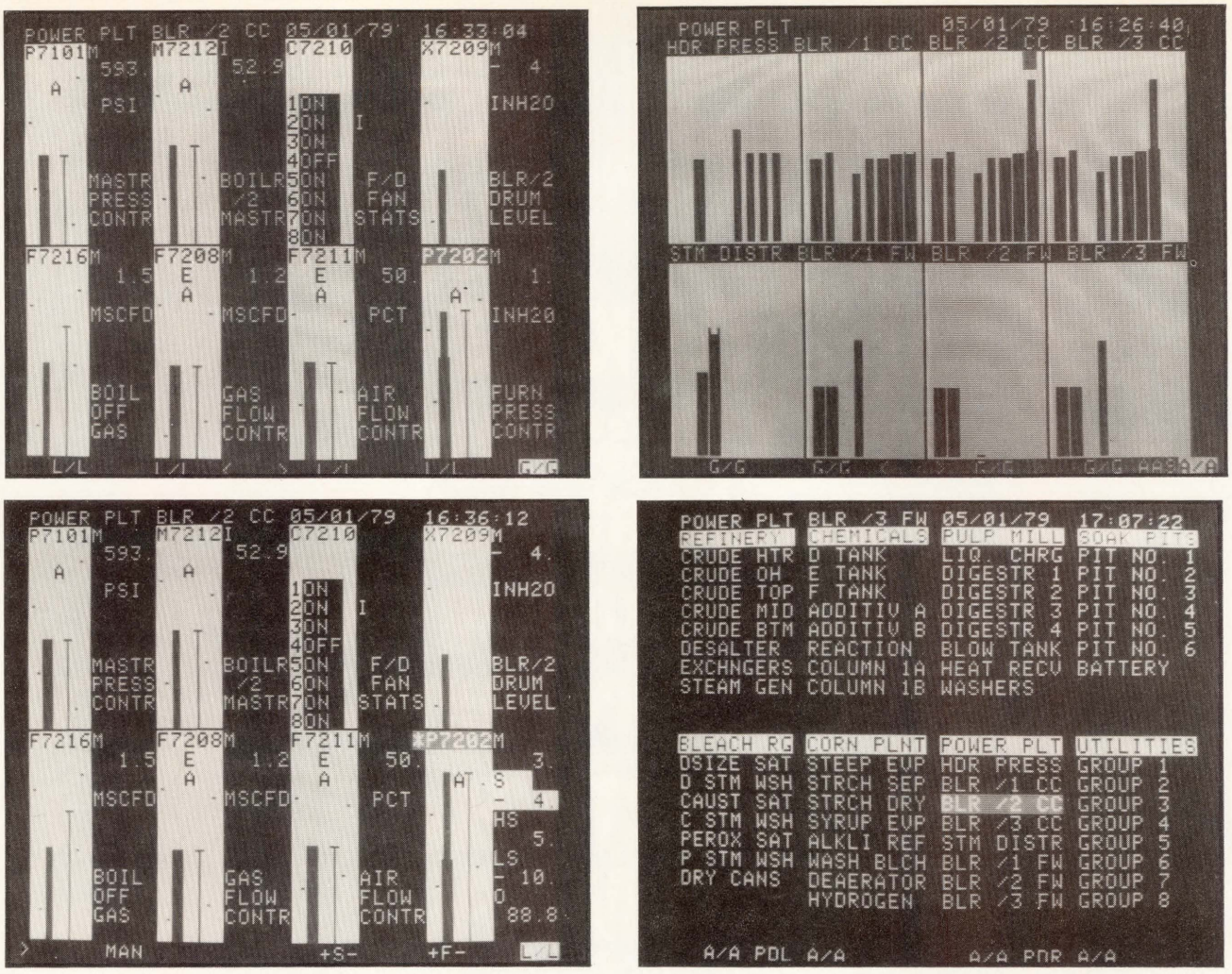


Fig 4 Shared display. Four typical levels of plant display (clockwise from top left) are plant view, area view, group view, and loop access view. Switching among levels is like stepping closer to a control panel.

distributed control systems, shared control allows much greater distance between the control location and the remote operator interface, and its use of digital technology minimizes communication problems. A video interface is easy to incorporate, and algorithms for control system design can be connected through a keyboard. Control system design is also much more flexible with shared controllers. Algorithms can be added, modified, or deleted at will to comply with control system design changes or plant expansion.

Shared control makes it easy to consider advanced control strategies without paying a penalty for omitting some function. It allows operator training by means of a simulation capability. Individual algorithms can be combined to produce algorithms that previously required process control computers. Finally, the inherent digital technology of shared control devices can incorporate digital algorithms into analog algorithms without the need for external wiring.

In a typical shared display and shared control arrangement, analog or digital field signals are brought to the shared controller (Fig 5), and the analog or digital outputs are sent from the controller to the field. The controller section has 60 software blocks that can be configured to assume any algorithm from an extensive menu. Algorithms are configured from the display at the operator workstation, by means of a removable, general purpose keyboard.

Fig 6 diagrams the PID controller algorithm. All elements in this diagram, except for the nonlinear extender element, represent individual software blocks that are supplied in the shared controller of Fig 5. Virtually all of these are also available with dedicated analog control; however, it may take separate hardware

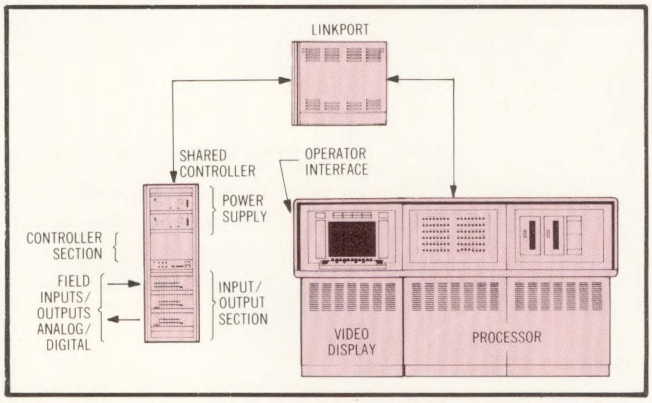
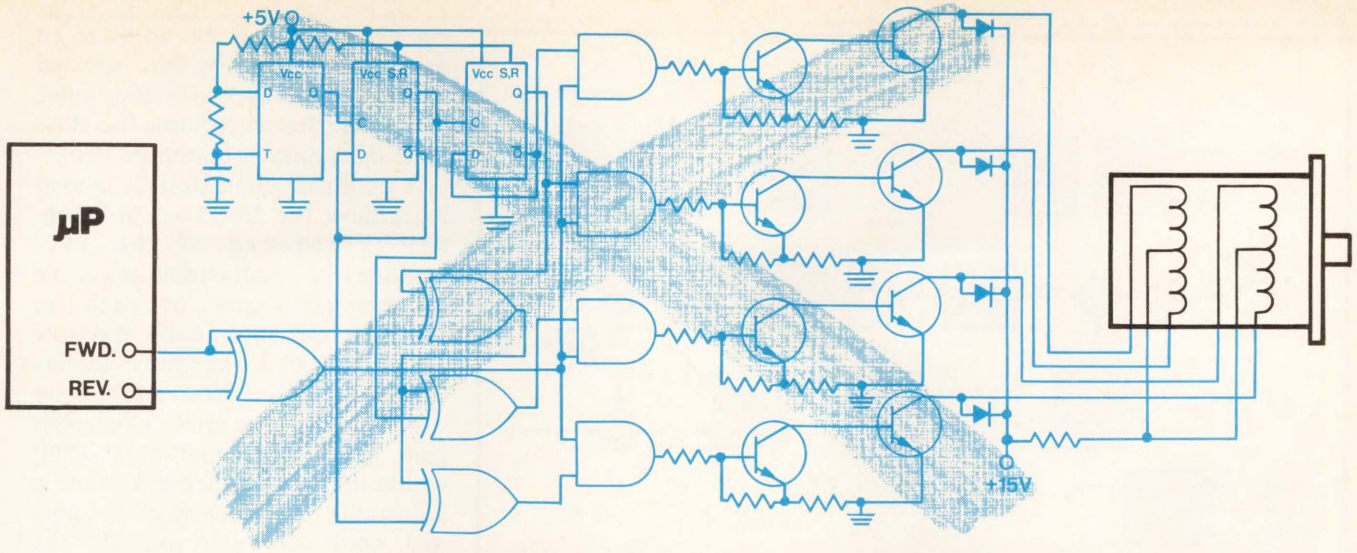
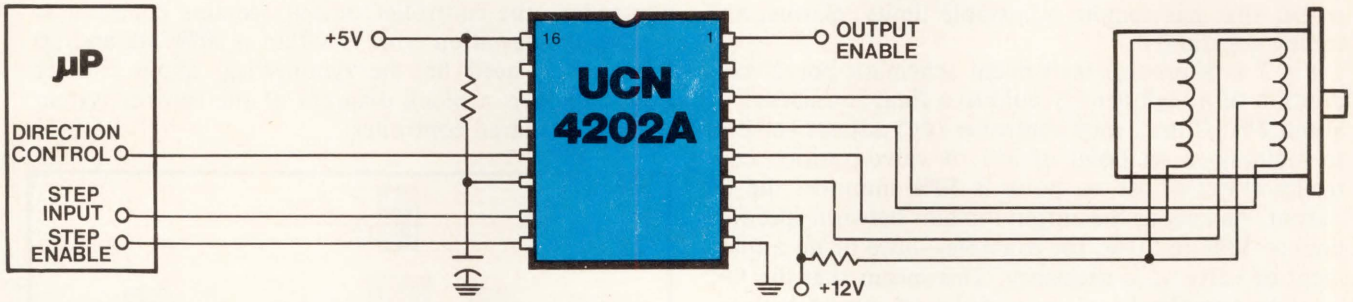


Fig 5 Shared display and control system. Input/output section at left routes signals to and from field. Controller section houses microprocessor. Workstation has general purpose keyboard and shared display



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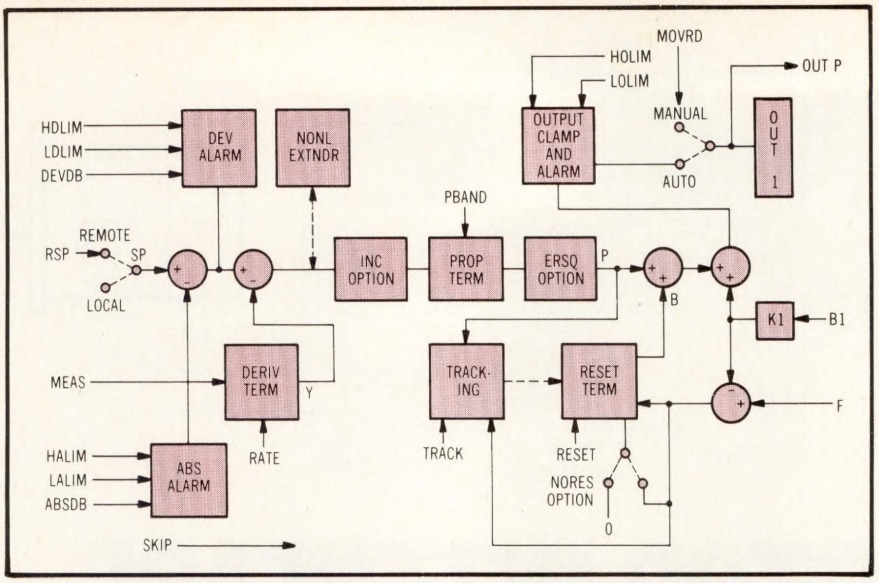


Fig 6 PID controller block diagram. Except for nonlinear extender labeled NONL EXTNDR (at top), shared controller supplies a software module for each block

units or combinations of hardware to achieve the result of one software algorithm. With shared control implementation, the algorithm can be as simple as a strictly proportional controller or as complicated as a PID controller that has remote adjustable limits, alarms, and tuning constants.

Fig 7 is a process instrument schematic for 2-stage dilution of a high density pulp to a final consistency of about 3%. Consistency controller (CC) adjusts valve V1 to maintain a set point of 3%. A valve position controller (VPC) whose set point is 50% monitors the CC output. As long as the output remains between specified limits—30% to 70%, for example—little or no adjustment of valve V2 is necessary. This means that the VPC must be completely tolerant of the CC output between 30% and 70%. If, however, V1 goes below 30% or above 70%, the amount of water added to the process via valve V2 must be adjusted to bring the output within selected limits. In this way, the CC loop valve (V1) is kept from operating too close to its maximum or minimum stroke.

A nonlinear characteristic is used to achieve the tolerance or insensitivity required of the VPC. Nonlinearity is adjustable about the set point (zero error) by specifying the high deviation (HD) and low deviation (LD) breakpoints. In this example, HD = 20% and LD = −20% about zero error. Controller gain [ie, proportional band (PB)] within the HD and LD breakpoints is adjustable as a fraction of the normal controller gain outside the breakpoints. Thus, if the normal controller gain is set at 0.5 (PB = 200%) and the gain fraction within HD and LD is set at 0.05, then the operating gain within the HD and LD breakpoints is 0.5 x 0.05 = 0.025, or a proportional band of 4000%. If the gain function is set to zero, the controller gain within the HD and LD breakpoints is zero (PB = infinity); and the controller behaves like a "gap" controller—the controller output remains constant as long as the deviation error is within ±20%. HD and LD breakpoints need not be symmetrical about the set point. Fig 8 is a block diagram of the control system within the shared controller.

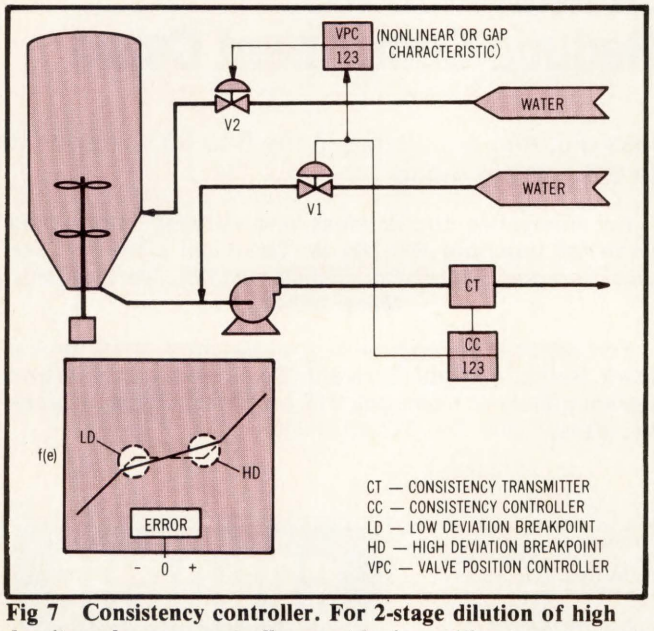


Fig 7 Consistency controller. For 2-stage dilution of high density pulp, VPC controller must be insensitive to CC output over wide range. Nonlinear characteristic (insert) achieves this and can be adjusted about set point by specifying high and low deviation

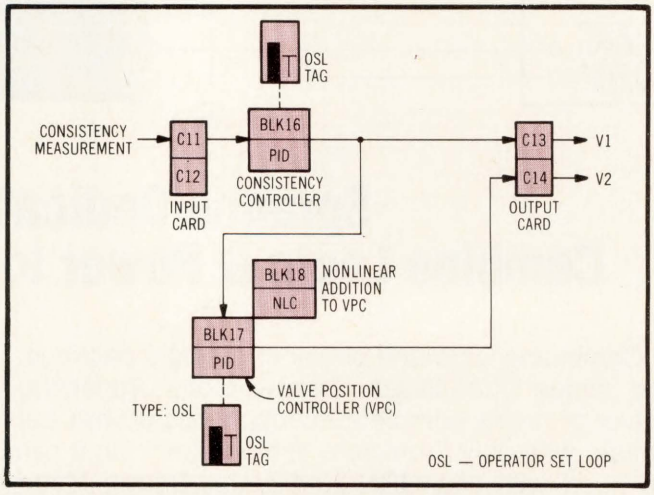
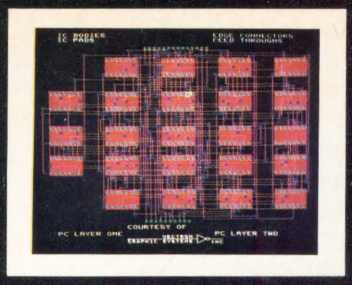
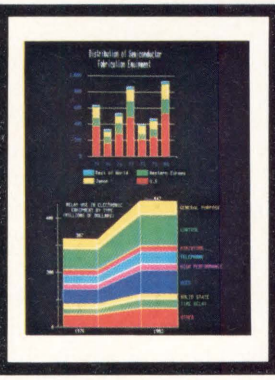


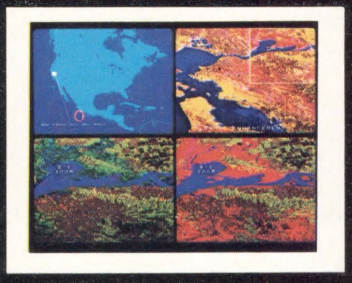
Fig 8 System block diagram. Blocks that operator must access connect to faceplate displays via broken lines; such shared display drawings are not within shared controller but are in shared display system

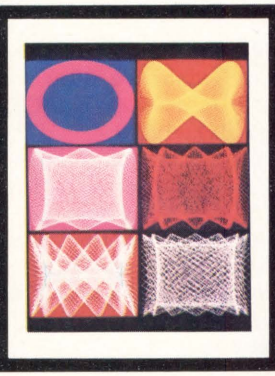
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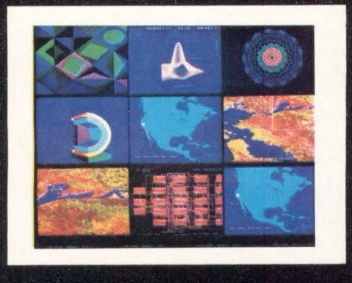
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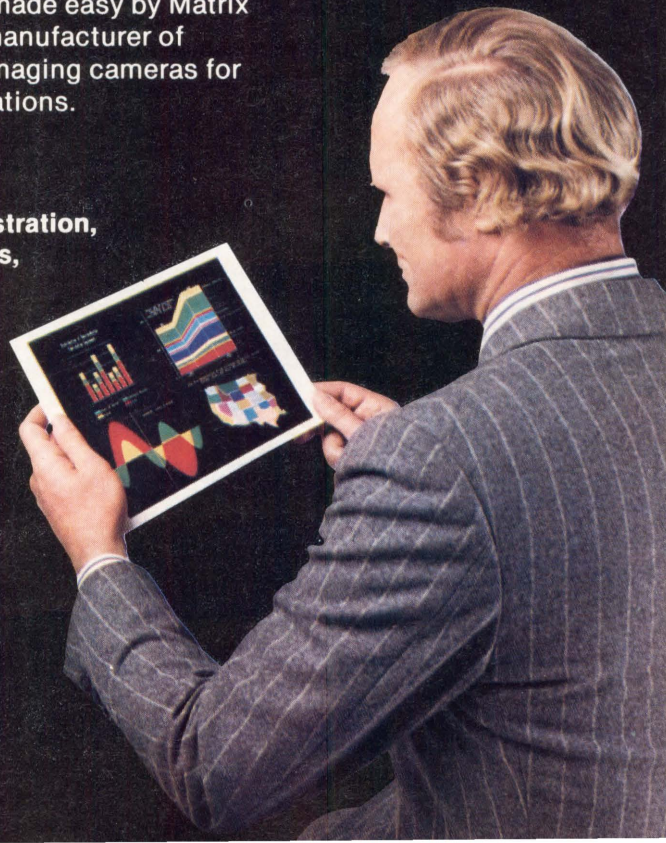
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Classes of industrial process control

Regulator control—directly controls one or two process parameters such as rate of flow, temperature, or chemical composition. Plant operators usually interact with a process at this level. Operators must accept regulatory control to keep automatic control fully automatic.

Unit control—regulates the performance, operation, and optimization of a particular operational unit, such as a distillation tower or a chemical reactor.

Coordinated unit control—manages the performance, operation, and optimization of several related or connected operational units.

Plant control—encompasses the performance and optimization of an entire industrial facility.

Multiple-plant control—coordinates all phases of corporate production activity. At this level, the major perturbations are economic in nature. Multiple-plant control usually involves large computer systems, not the sensor based, realtime systems that characterize the other four levels of process control.

The five classes of industrial process control form a hierarchy of levels that must be implemented in sequence. For example, coordinated unit control cannot be achieved without first providing successful unit control. At the lowest level, regulatory control and its associated process measurements form a critical element. If regulatory control is not implemented correctly and accepted by operations personnel, all other levels of control are essentially blocked from application.

display formats were partially reestablished. Digital control products became more "block" oriented and easier to configure, and the need to heavily staff computer experts was eliminated.

Shared display/control systems now operate easily at least to the unit level and possibly to the coordinated unit level of control. (See "Classes of industrial process control.") Analog control devices have always performed at least second-level control, such as feedforward, but advanced control enjoyed only limited application. With dedicated (discrete) analog products, upgrades to sophisticated control strategies invariably called for a long period of modification and adjustment. In contrast, modifying, adding to, and testing a shared control system can be accomplished within minutes. Process computer flexibility, combined with analog hardware, has significantly improved process operations capability. Now that flexible analog hardware is readily available, shared control will be limited only by the user's imagination.

Acknowledgments

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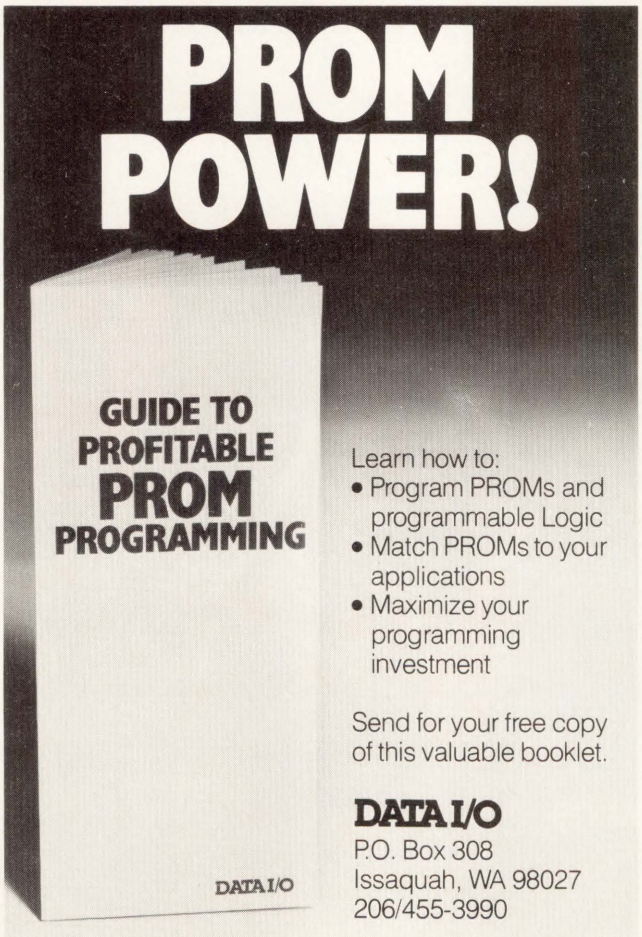
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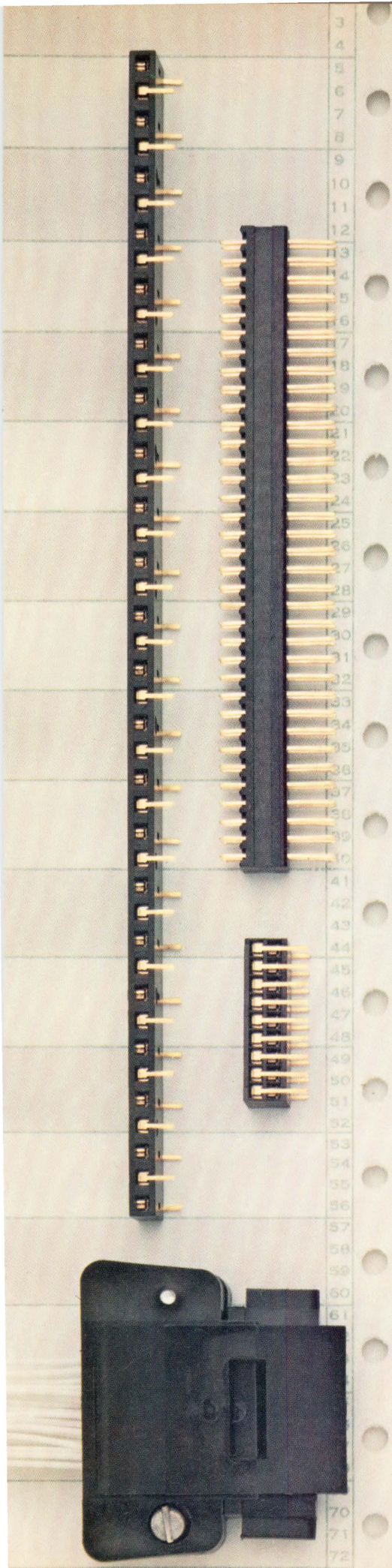
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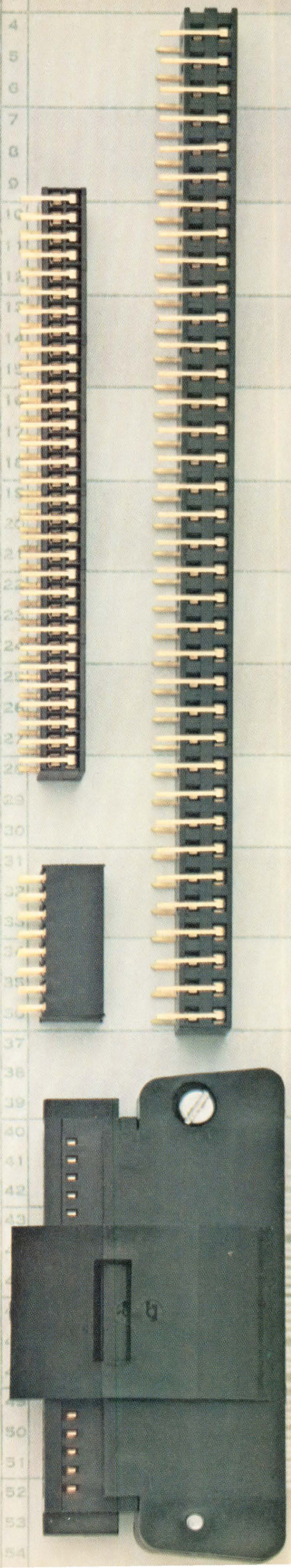


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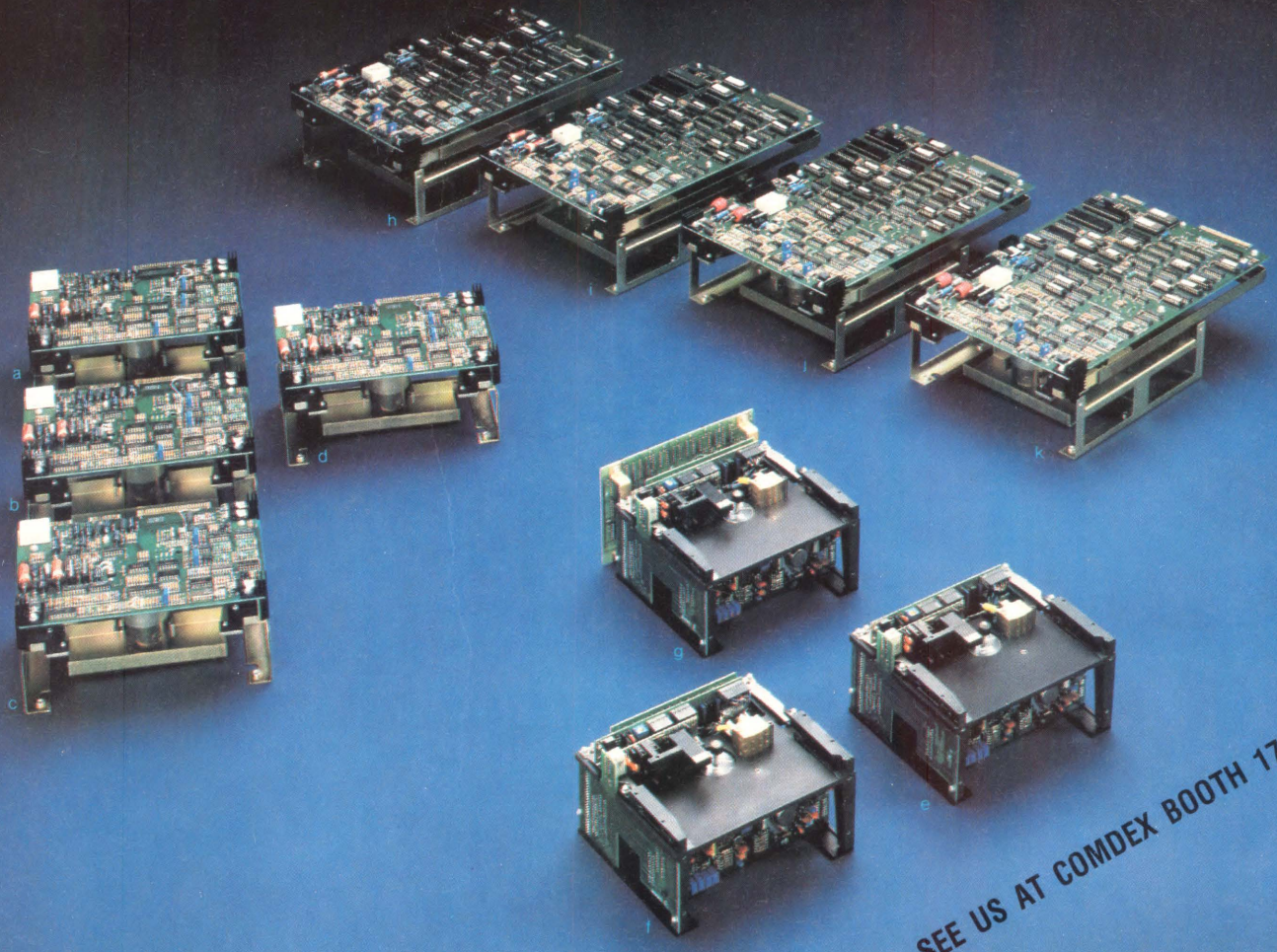
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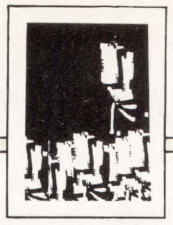
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CIRCLE 76 ON INQUIRY CARD



CAD COMBINES ANALOG AND DIGITAL LAYOUT ON SWITCHER PCB

Combining digital with analog PCB layout techniques results in a CAD strategy that provides efficient layouts for switching power supply boards

by William Adams

A trend away from linear power supply technology and toward use of switching power supplies has led to a reevaluation of printed circuit board design techniques. Manual procedures that were acceptable in linear power supply designs have proved inadequate for designing switchers in which the printed circuit board is essentially the entire structure. A turnkey system has been adapted to automate the printed circuit board design process with significant gains in engineering efficiency, standardization, ease of manufacture and, most critical, prototype cycle time.

A major portion of the market for power conversion equipment is devoted to power supplies used in data processing and communications systems. Traditionally, these systems had linear power supplies containing large magnetics (eg, chokes, transformers, stabilizers), dissipative devices (transistors mounted on heat sinks), and printed circuit boards (PCBs) with relatively few components. However, during the past few years, there have been significant increases in system capability and decreases in physical size. A desktop or minicomputer system currently can provide the same capability that previously required a room sized system. The switching power supply can fulfill the requirements of these recent developments, being more efficient and smaller than an equivalent linear unit.

Power demands of systems manufacturers also require a significant commitment to switching power supply design and manufacture. In making this commitment, product orientation changes from a package of large magnetics, dissipative devices, and relatively low density PCBs, to a package in which small magnetics—as well as a majority of other components—are mounted on a complex PCB (Fig 1). Switcher design dictates strict component placement and routing constraints, which further increase design complexity. Computer aided design (CAD) systems, widely used in the electronics industry, have attributes consistent with the needs of power supply manufacturers and technological changes in power supply products. Improvements in engineering efficiency, standardization, manufacturability, and prototype cycle time all are realized.

William Adams is manager of computer aided design engineering at Acme Electric Corp, Water Street, Cuba, NY 14727, and is currently implementing design retrieval systems. Prior to this, he designed power semiconductor products and process parameter control systems for General Electric Company. Mr Adams holds a BS degree from the State University of New York at Oswego and is pursuing an MBA degree at Syracuse University. He is a member of the IEEE Computer Society.

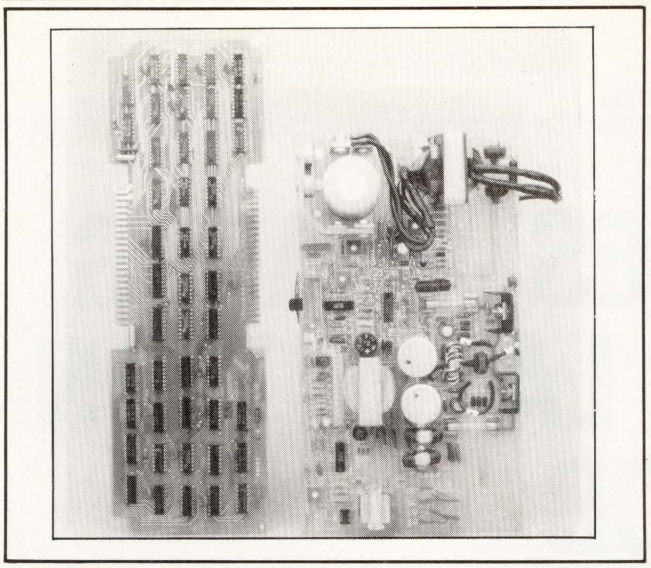


Fig 1 Digital vs analog PCB. Fundamental differences in component mix, layout, and power requirements enforce different design strategies

Manual methods

Most custom power supply manufacturers follow typical manual method procedures before installing a CAD system that include these steps:

- Produce a preliminary electrical design to meet customer specifications; provide a schematic diagram with a parts list supporting that design.
- Where necessary, breadboard the preliminary design.
- After review of the preliminary design and breadboard, begin the mechanical layout. Determine preliminary PCB size.
- Packaging engineer provides layout of PCB.
- Determine hole sizes and connection pads from tabulated lists.
- Produce the PCB layout at two times full scale; hand-tape layout in preparation for photography.
- Electrical and packaging engineers review artwork produced by the preceding process; modifications are incorporated as needed.
- Approve artwork; order the required number of cards.
- Produce PCB prototypes using the released artwork.
- Evaluate design; changes or modifications are again incorporated as needed.

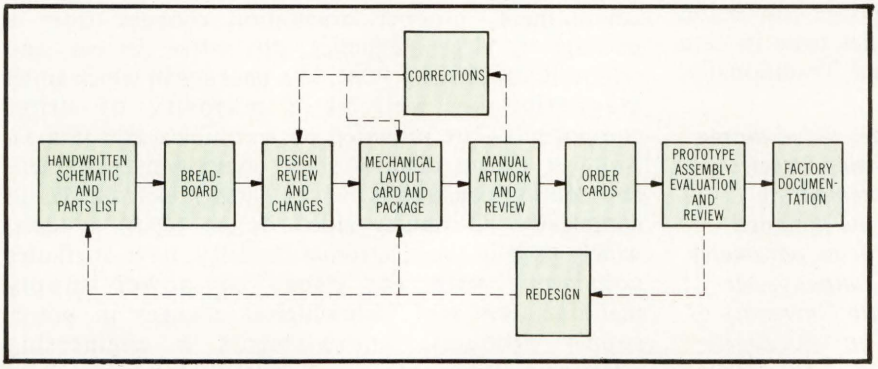


Fig 2 Manual design method. Prototype design cycle spans 12 to 20 weeks. Although fairly efficient for simple, low density, linear power supplies, it is not effective for complex switchers

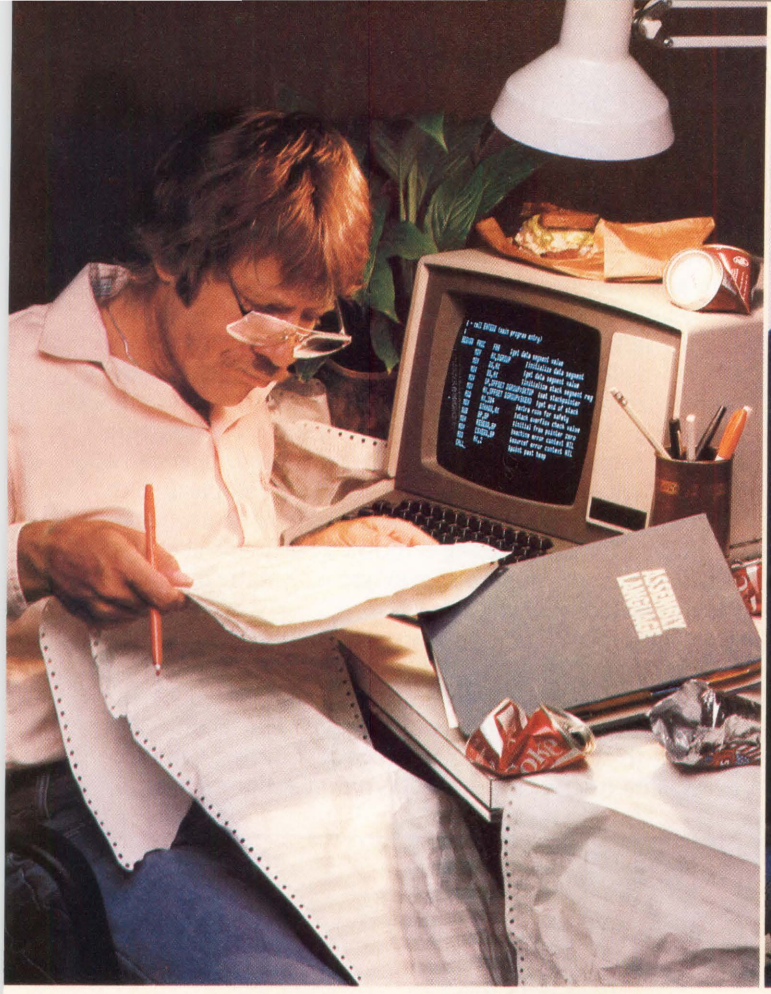
While reasonably effective when applying simple, low density techniques, manual design methods are totally ineffective for complex switcher PCBs (Fig 2). Misalignment and incorrect selection of hole positions and pad sizes on double-sided boards, and routing errors are some major difficulties encountered. In addition, a large portion of the power supply business is custom based; the ability to make changes quickly and accurately is fundamental to business success. Many times, minor changes dictate an entirely new board layout. In linear power supply designs, standardization has built up over the years. However, switching power supply technology continues to change rapidly. New components and circuit techniques accentuate the need for a more flexible design process.

Hybrid analog/digital product presents unique challenge

One manufacturer began surveying computer aided design systems in 1978. The survey showed most of the turnkey systems were designed for digital PCB layouts rather than the hybrid analog and digital layout commonly found in a power supply. For the survey, a digital PCB was defined as a board composed of integrated circuits operating at low power levels. In switching power supplies, large amounts of power are routed among discrete components, such as diodes, capacitors, and resistors. The power supply also contains some digital circuitry for control purposes.

The marriage of analog and digital circuitry on the same PCB presented a challenge which was not met by former CAD offerings. In fact, many concepts supported by CAD vendors are counter-productive when applied to power supply PCB layout. Specifically, automatic component placement becomes unworkable when a board contains 80% discrete components of approximately 30 different shapes and sizes. In addition, automatic routing and placement using connection length as the major criterion is not desirable in a power supply. Limited system algorithms do not always permit designers to select spacings that meet standards set by regulatory groups. Furthermore, previously used circuit blocks cannot be called forth easily for use in a new PCB design. Although the drawbacks appeared quite severe, the potential for CAD did exist. One formal program was launched in 1980 which led to the acquisition of a turnkey CAD system.

The systems reviewed received a preliminary check. If a system appeared to meet requirements, a sample "benchmark" switcher was used to evaluate it. The major factors that determined selection of this CAD designed PCB were the system's ability to handle 100 designs per year, and capability to be operated by a user unfamiliar with computer programming. Other selection factors included the system's integration of post-processing for artwork production, automatic test, and automatic component insertion sequences; comments from present users on service, software support and training; and online error checking capability.





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Interim method implements a service bureau approach

Implementing the CAD design concept involved restructuring the engineering design team. Previously an electrical and packaging engineer did the complete design, now a CAD engineer and technician were added. In seeking to maximize utilization of the CAD hardware, a service bureau was established. Electrical and packaging engineers provided information to the data preparation technician and CAD engineer, who then provided card layouts.

Several problems developed in this approach. Initially, insufficient time was devoted to establishing a design library, and data preparation time was consistently underestimated. The service bureau environment, successful in digital designs, fails to serve the need for electrical and packaging engineer interaction, as is required in analog designs. Consequently, design responsibilities could not be clearly defined, and strategic objectives for PCB changes and prototype lead times could not be met.

This early experience with CAD exposed underlying problems. The CAD system was being used as a drafting tool, and not as a design tool; therefore, the CAD engineer was being used as an operator, not as an expert. The system also precluded effective interaction between the packaging engineer and CAD engineer. Errors occurred in basic data entry that were directly related to undefined responsibility and authority. Basic change techniques were not adequately delineated, and delays were caused by use of an outside source for photo plotting.

Ultimate method integrates two design strategies

A new approach was developed, interrelating two strategies which later proved quite successful. Development of procedures and computer programs were advanced to enhance analog component placement and routing capabilities. Then, project management techniques needed to reorient the work and data flow were developed, thus providing a cost-effective balance between automated and manual design engineering.

The implementation of these strategies required a three-stage approach. Stage I involved reorganizing the basic project team to consist of an electrical engineer and a packaging designer, with the CAD engineer and technician as support. The packaging designer was trained to operate the design console. During stage II a new reentrant router, which would allow an analog design strategy, was evaluated, and the generation of in-house artwork was explored. Stage III, yet to be implemented, involves restructuring the electrical packaging interface and generating a formalized prototype schematic system that uses standardized blocks and part lists integrated with the material requirements program and vendor control systems. This system is based upon a design retrieval data base and graphic interaction.

During the first implementation stage, four mechanical designers were trained as CAD system operators. Data preparation was handled on a routine basis under the supervision of the CAD engineer. This realignment of responsibility proved effective in avoiding system problems which involved data preparation and post-processing. The number of design errors caused by a lack of experience with a switching power supply design were reduced, and a more effective team effort was fostered. Data preparation capability was extended from the input of basic PCB data to include information for generating the schematic's components and its connections on and off the board. Hence, a "back" schematic technique developed, comparable to back annotation, which generates a schematic useful for further design change. Fig 3 shows a basic self-checking feature used to compare the revised schematic output to the interactive PCB changes.

In the second stage, a reentrant router replaced the manual, computer assisted approach. With this new router, analog design schemes can be tailored to the needs of a particular power supply. The engineer is allowed to select areas of the board, groups of connections, side of the board, and a minimization of vias, as

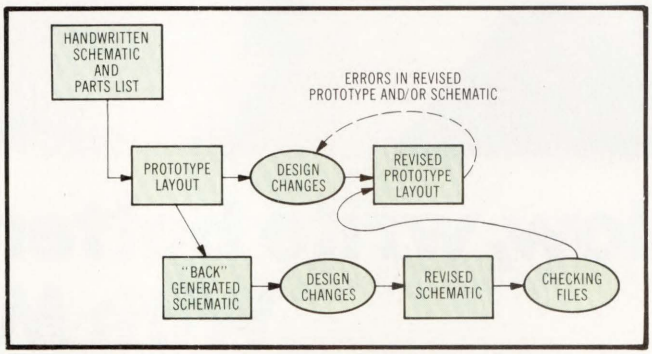


Fig 3 Basic self-checking feature. So called "back" schematic can be used for further design refinements. Then, revised schematic output is checked against interactive PCB changes

well as angle and segment criteria, to determine the extent of routing during each pass. The router also helps designers lay out a multilayer board using design automation techniques giving a four to one increase in productivity while routing noncritical runs.

Generating artwork is usually time consuming because final design checking must be delayed until the photo plot is back from the service bureau. In stage II, inhouse artwork is generated using the basic quick plot capabilities of the design system, modified to allow generation of true track widths and true pad diameters. Initially, the artwork will be used for inspection of electrical and packaging requirements. Stage II will extend the artwork scheme to generate master artwork for prototype production.

Stage III is expected to provide the most significant overall benefit to the design process by supplying the electrical engineer with standard building blocks of schematics for basic structures or design functions. These functions include input and output sections, regulation, control, pulse width modulation, bulk transformers, and so forth. The basic concept calls for the electrical engineer to review customer requirements and determine if standards previously used are

appropriate. If so, these tested schematic blocks may be incorporated into the design. These blocks not only aid the electrical engineer in generating a schematic for the first pass on the CAD system, but also will aid in standardizing parts. With further extensions to data files, individual blocks will contain various layout schemes that were tested in a pseudo-breadboard fashion on a sample PCB.

This concept will also help the packaging engineer by providing extensive input lists, and standardized schematic formats and parts among many board designs. Later in stage III, actual routes in the individual blocks will be passed along to the packaging engineer, providing the majority of routes available for critical areas on the board, or various configuration options for each individualized block. This will enable the packaging engineer to check preconfigured routes, determine which previously tested layout scheme will be used, and ascertain the best layout scheme for interrelating blocks and the associated critical runs. The remaining routes, normally noncritical, will be handled by the reentrant, multilayer router implemented in stage II.

Before completion of stage III, a universal parts list capability will be initiated. This will permit automatic searching of the data base for information, such as part numbers; various design items, prices, and symbols; and libraries which are needed to enhance the mechanical and electrical design. It will also eliminate manual input of descriptive information for each card and reduce the overall data input for individual designs to a part number.

Summary

A major commitment to a fast changing, competitive technology led to an examination of existing design procedures. The shortfalls this examination uncovered have been successfully bridged through the introduction of a turnkey CAD system, and a series of major changes in project management and work flow procedures. Significant improvements already are realized in design efficiency, standardization and prototype cycle time. While this success was not easily won, it increased confidence that a computer aided design system can significantly improve design effectiveness, and ultimately, customer service. CAD system enhancements are systematically being added through an ongoing program. The gains to date are expected to be overshadowed by those yet to come. The future of system design is definitely linked to an ever increasing use of CAD.

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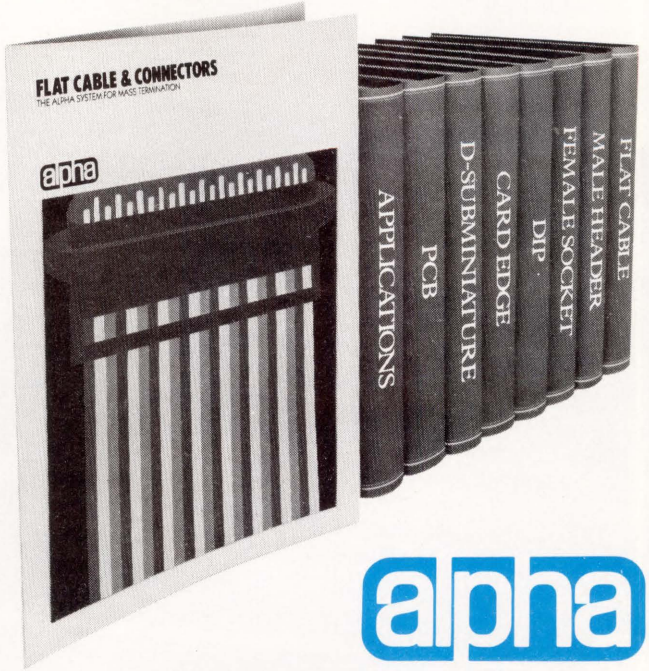
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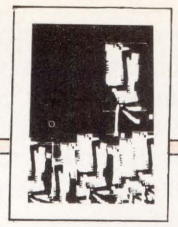
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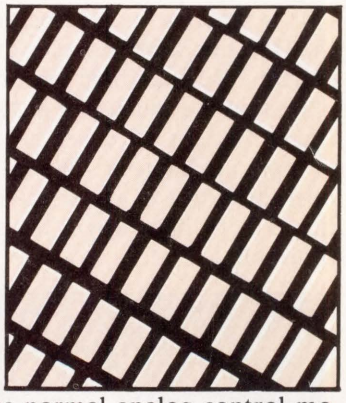
TOUCH PAD CONTROL FOR THE HARSH ENVIRONMENT

Micro-proximity sensing devices furnish totally sealed, solid state replacements for electromechanical controls that require elaborate protection to cope with industrial environments

by Robert A. Abler

Electromechanical controls cannot withstand hostile or unfriendly environments without special design considerations. Moving parts, contacts, connections, mountings and fragile elements cause premature malfunction and permanent failure if not protected from harsh environments, external disturbances and rough handling. In addition, it is always expensive—and sometimes impractical or impossible—to fully protect control devices. Protection schemes often impede proper operation; the action of most electromechanical controls, and the basic design of others, introduces undesirable effects such as contact bounce, electromagnetic interference (emi), and time delay into control systems. The need to suppress or eliminate these effects creates additional design and product expense.

Different manufacturers usually design varying types of electromechanical control components, so there is little compatibility or operating similarity among them. The devices are designed to serve the application, not the user. As instrument and equipment designs become totally digital, it is increasingly difficult to design digital control systems that accommodate normal analog control motions of the human operator.



Current electromechanical devices cannot access the total capabilities of sophisticated electronic systems, since the basic technology of electromechanical control devices is 50 to 100 years outdated. This technological retreat has not kept pace with the semiconductor technology of microprocessors, ICs, LSIs, and so forth. The resulting effect is that few, if any, alternatives are available to instrument or equipment designers, who have been forced to select slightly different sets of do it yourself control components or to build their own custom control systems, with colors, sizes and shapes used to discriminate components.

The problem of a harsh environment has been countered through use of protective coverings, elaborate gasketing and the reduction of control elements. These attempted solutions all increase operator inconvenience and/or reduce the operator's ability to access

Robert Abler, vice president, operations, for TASA, Inc, 2346 Walsh Ave, Santa Clara, CA 95051, has also authored papers in the fields of magnetics, biomagnetics, nonimpact printing, and spectroscopy. He received a BS degree in engineering from San Jose State University, and holds several engineering patents.

the total capabilities of the instrument or equipment being controlled.

Solid state touch controls

A new technology, called micro-proximity sensing, responds to the need for human controlled action (except voice) and can replace every type of control device with a solid state equivalent, operated by touch and finger motion. This totally electronic approach not only eliminates all mechanical movement and its accompanying problems, but also provides a new, integrated control system capability which will have far reaching impacts on the design of future electronic instrumentation.

Discrete controls

Micro-proximity sensing technology is a method of control that combines the analog world of the human body with the digital world of solid state electronic design, without the need for mechanical intervention. Though highly sophisticated, the technology is deceptively simple in its mechanical design. The touch pads are located on a substrate, such as a PCB. In the case of coded output panels, the sensors are placed in the desired locations where switches would have been placed. (See Fig 1.)

When a touch pad is activated, a distinctive change of electrical voltage levels occurs. This is immediately reflected in a parallel coded output on the output lines. Approximately 1 μs after the data signal is valid and latched, a continuous, latched strobe appears on the remaining output line. All signals are open collector, single load transistor-transistor logic (TTL) outputs.

It is inherent in the operating principle of the panel that the operator becomes an active component in the system. The electronic sensors recognize the bare finger placed on the touch pad as valid entry instruction if the finger flattens to cover an area approximately 0.20″ (5 mm) in diameter. When this occurs, the electrical operating state of the selected sensor changes from low (logic 0) to high (logic 1), passing through the preset threshold.

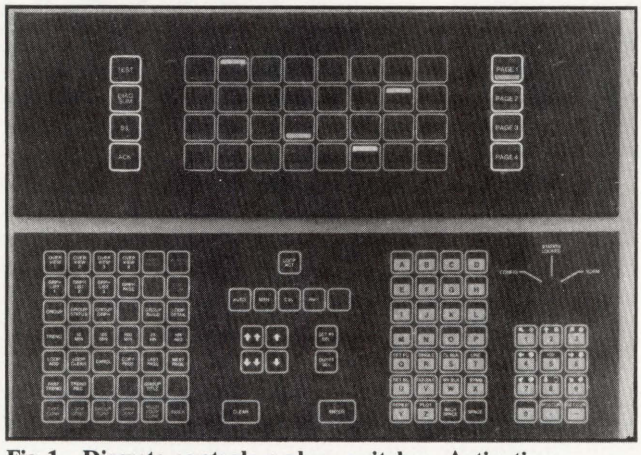


Fig 1 Discrete controls replace switches. Activating touch sensitive pad causes distinctive change of voltage on output lines

The sensing is accomplished in the LSI circuit, which also performs the coding function. This provides a fully coded, bounce free parallel output and strobe for each activation. All control panels have two key lockout capability for all binary encoded sensors; however, internal functions can provide two key operations if required.

Continuous controls

The Ferenstat™ is essentially a solid state potentiometer, with sensors that respond not only to the presence of a finger, but also to its motion and direction. In addition to eliminating an analog to digital converter (ADC) in many control applications, the Ferenstat eliminates mechanical wear caused by moving parts. Its sealed construction also makes it highly resistant to harsh environments and operator inflicted damage.

The construction of the Ferenstat and its two-dimensional counterpart, the TouchGraphic X-Y positioner (see Fig 2) are somewhat different from that of a switch panel, however they are technologically the same and can be integrated into a single control system. The development of the Ferenstat involved a high degree of "human engineering." The heart of the design lies in its proprietary array of high speed capacitive sensors, arranged in clusters. They are able to function in close proximity without interfering with one another.

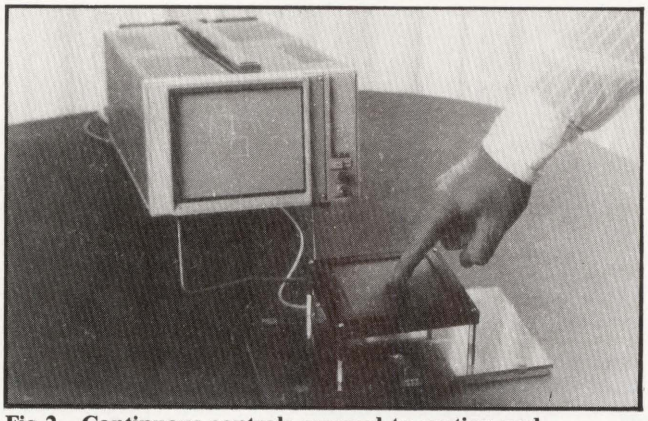


Fig 2 Continuous controls respond to motion and direction. Solid state detector registers presence of finger on sealed and insulated surface

These detectors register the presence of a finger on the sealed, insulated surface. The total group of sensors is sampled in parallel at a rate fast enough to detect the most rapid possible finger motion (Fig 3). Each sample clock loads the output of all sensors into a parallel register. This so called "present" register is then compared with the "previous" sensor sample to detect the direction and extent of motion.

The logic which accomplishes this compares the contents of each bit in the present register to adjacent bit positions of the previous sample. In so doing, it is possible to detect the new sensors activated, indicating that motion occurred and in which direction.

The results of this count are then applied simultaneously onto the digital output terminals, which can drive a display and interface directly with the equipment being controlled. The Ferenstat generates positive up/down pulses without regard to where the operator places a finger on the surface, since the output is relative, not absolute position oriented. Because of this,



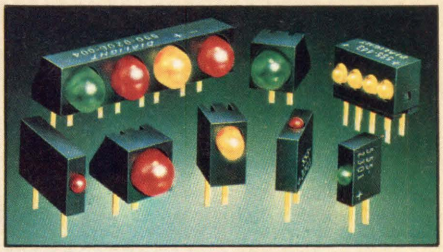
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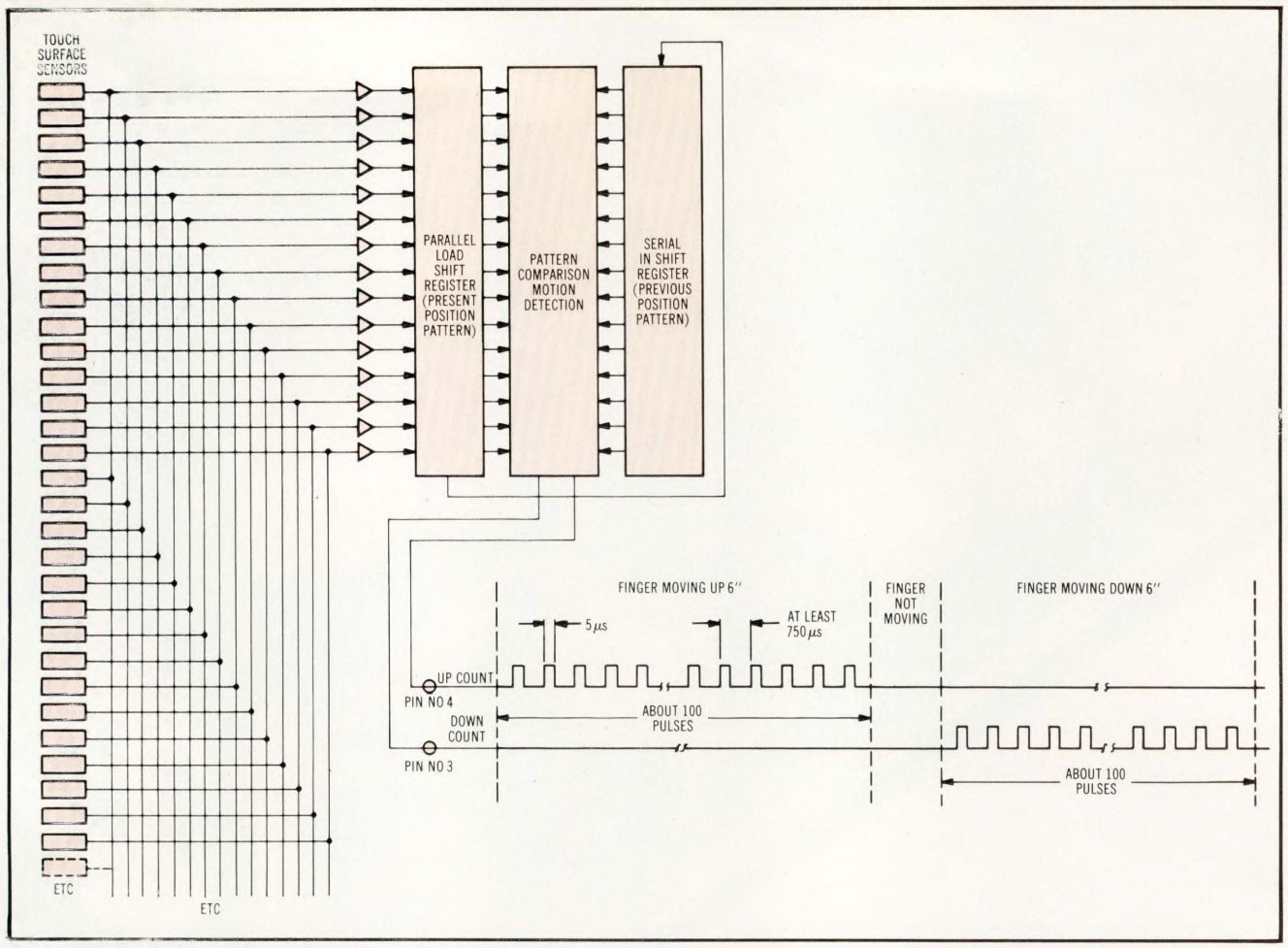


Fig 3 Touch sensitive circuitry. Block diagram at left shows two registers that hold present and previous positions. In timing diagram at right, clock pulses gate input samples to detect finger motion and determine its direction

the device is not limited in resolution by its length, but only by the manner in which the design engineer chooses to use the pulse train. Furthermore, with a simple software algorithm, the Ferenstat can be given a finger velocity sensing capability enabling its resolution to become completely controllable by the operator, in real time, by manipulating finger speed.

Limitations

The few limitations or disadvantages of the new microproximity control technology are highly specialized and limited in application. When first presented with the solid state control technology, many engineers may feel a major disadvantage is the lack of tactile feedback. However, only in a few specific applications, where other forms of audiovisual operator feedback cannot be incorporated, is tactile motion an operator specified requirement. Several human factor studies support this contention, showing that there is little correlation between switch movement and the performance level of the operator.

A few unique application requirements may make it difficult or even impossible to achieve satisfactory performance from the new control technology, for example, underwater operation, metal bezel which covers most of the control panel face, or operation through heavy gloves. Successful operation through a medium or light glove has, however, been achieved.

Conclusion

With the advent of solid state control technology, design engineers now have a solution to the problem of designing control systems that resist hostile environments. The new technology can cost effectively replace any assembly of electromechanical control components, providing such additional benefits as higher reliability, realtime control, and more features for design freedom. The system also reduces overall system costs, including unit cost, engineering time and expense, service and repair, purchasing, receiving, inventory and overhead. With its unprecedented benefits, microproximity sensing has tremendous potential for existing applications and the future—the number of new development possibilities are almost unlimited.

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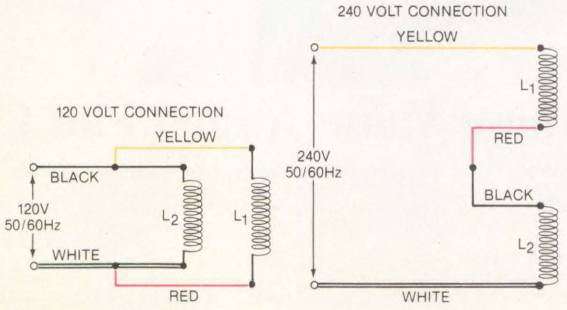


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SMART A-D DOUBLES THROUGHPUT

A microcomputer dedicated to the analog front end furnishes a high degree of local intelligence, boosting throughput by unburdening its LSI-11 host

by Andrew W. Davis

Multiplexers increase the efficiency of analog to digital conversion systems by permitting a costly system element, the analog to digital converter, to be shared across multiple channels of analog input. A typical block diagram of a high performance, direct memory access, microcomputer analog to digital system is shown in Fig 1. Although this configuration is the most widespread, it is also possible to configure the multiplexer after the sample and hold amplifier, or even after the analog to digital converter. These approaches are more expensive since fewer resources are shared, but generally they lead to higher system throughput. While much of the technical literature deals with the cost, speed, timing and accuracy tradeoffs inherent in alternative system designs, little attention has been paid to the flexibility constraints imposed by the multiplexer design implementation.

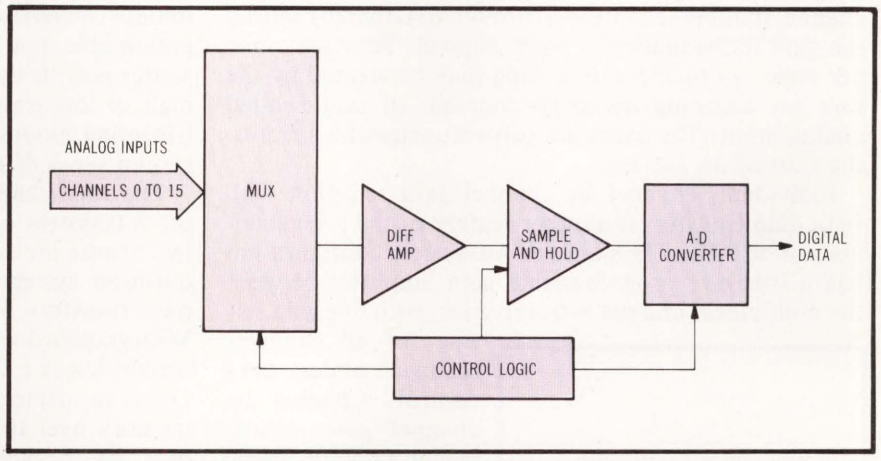


Fig 1 Multiplexed data acquisition. MUX handles 16 channels of analog input in this customary architecture. Placing MUX inboard of sample and hold or A-D converter would reduce efficiency

Analog to digital (A-D) conversion systems generally allow for data transfer via either programmed input/output (PIO) or direct memory access (DMA). It is possible under PIO to control a multiplexer for each individual data conversion, and in this way to scan any number of channels in any sequence; however, the PIO approach involves high software overhead and can lead to throughput rates from 50 to 90% lower than those available via DMA.

DMA data conversion systems offer the highest system throughput rates, but generally limit the programmer to scanning one channel continuously or to scanning all channels in numerical sequence. Some recent DMA devices allow the programmer to scan any contiguous subset of channels, for example channels 5, 6, 7, 5, 6, 7, etc, until a given number of conversions have been placed into the memory buffer.

The combination of PIO total user scanning flexibility and the fast A-D data transfer rates possible under DMA are used in the design of the Data Translation DT3362. Within this A-D system the multiplexer contains a user programmable random access memory (RAM) channel gain list file that allows any channel sequence from 1 to 256 entries long to be scanned by the ADC. Although the RAM list is loaded under PIO, the actual 12-bit A-D conversions and data transfers are done under DMA control at throughput rates up to 250 kHz.

An architecture compatible A-D system for the DEC LSI-11/2 and 11/23 microcomputer, the DT 3362 provides for up to 64 single ended (32 differential ended) analog input channels on a standard quad-sized board. In addition to the RAM channel gain list file multiplexer, the board features multiple A-D triggering schemes, up to 250 kHz throughput to memory, and an external data

Andrew Davis is marketing director with Data Translation, Inc, 100 Locke Drive, Marlboro, MA 01752, and is responsible for all marketing functions of the company. Prior to joining Data Translation, he served as a product manager with Data General Corp. Mr Davis holds an MS degree from Cornell University and an MBA degree from Harvard University.

port, used with a companion dual ported memory board, for data transfers that do not require system bus resources.

The A-D system implements an onboard RAM channel list file for versatile multiplexing. An LSI-11 processor on the Q-bus has read/write access to the onboard RAM enabling it to store and read the channel numbers under software control. The RAM is 1024 bytes organized as four totally independent pages of 256 bytes. (See Fig 2.) The start address pointers and final address pointers are also programmable for each of the four pages. When the A-D conversion process is started, whether by program control or an external trigger, an incremental pointer in the A-D hardware will begin at the start pointer and increment through the RAM list to the final pointer, at which time the hardware will automatically reset the incremental pointer back to the start pointer location. Because the pointers are user defined, any subportion of the 256 byte list can be utilized.

Each byte in each page can be loaded with 2 bits for programmable gain (1, 2, 4, or 8) and 6 bits for the channel number (channels 0 through 63), thereby setting the gain individually for each channel. Four lists, one per page, up to 256 entries long may be created by the user for scanning up to 64 channels of single-ended analog input. The pages are software selectable prior to the start of an A-D scan.

Individual, channel by channel gain selection with DMA data transfers is another feature of the RAM channel gain list file. The standard A-D system configuration has a software programmable gain amplifier between the multiplexer and the A-D converter, with one gain setting for all channels scanned under DMA control. Channel by channel gain adjustments may be made only with an increase in software overhead and a resultant decrease in system throughput with a PIO-driven data collection program. For example, if bytes 0 to 2 contain 6, 9, and 4, with 0 as the starting address and 2 as the final address, the ADC will multiplex channels 6, 9, and 4 and then start over. No time will be lost scanning through all 16 channels nor will extra memory be required to hold values for absent channels. Note that the three channels multiplexed could be any three channels in any order. Moreover, the final address pointer and the start address pointer could be loaded with the same value. When this is done, the incremental pointer will always stay at the same RAM list location so that only one channel will be sampled by the A-D.

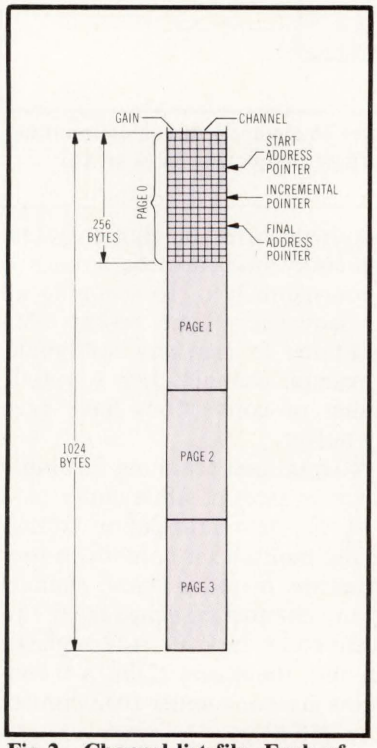


Fig 2 Channel list file. Each of 1k bytes can designate channel number and gain. Software selects page before start of scan

If successive bytes of page 0 contain 0, 1, 0, 2, 0, 3, etc, the A-D system will again multiplex through the list from start address pointer to final address pointer. If the ADC is triggered at 200 kHz, channel 0 will be scanned at 100 kHz, but channels 1 through 5 will be sampled at only 20,000 samples/s. To scan a selected subset of channels, different instruments or experiments are connected to the ADC; only one will be scanned at any particular time, depending on which page of the RAM channel list file is selected by the software. This function is useful, for instance, in some medical applications where several patients may be monitored by one computer system.

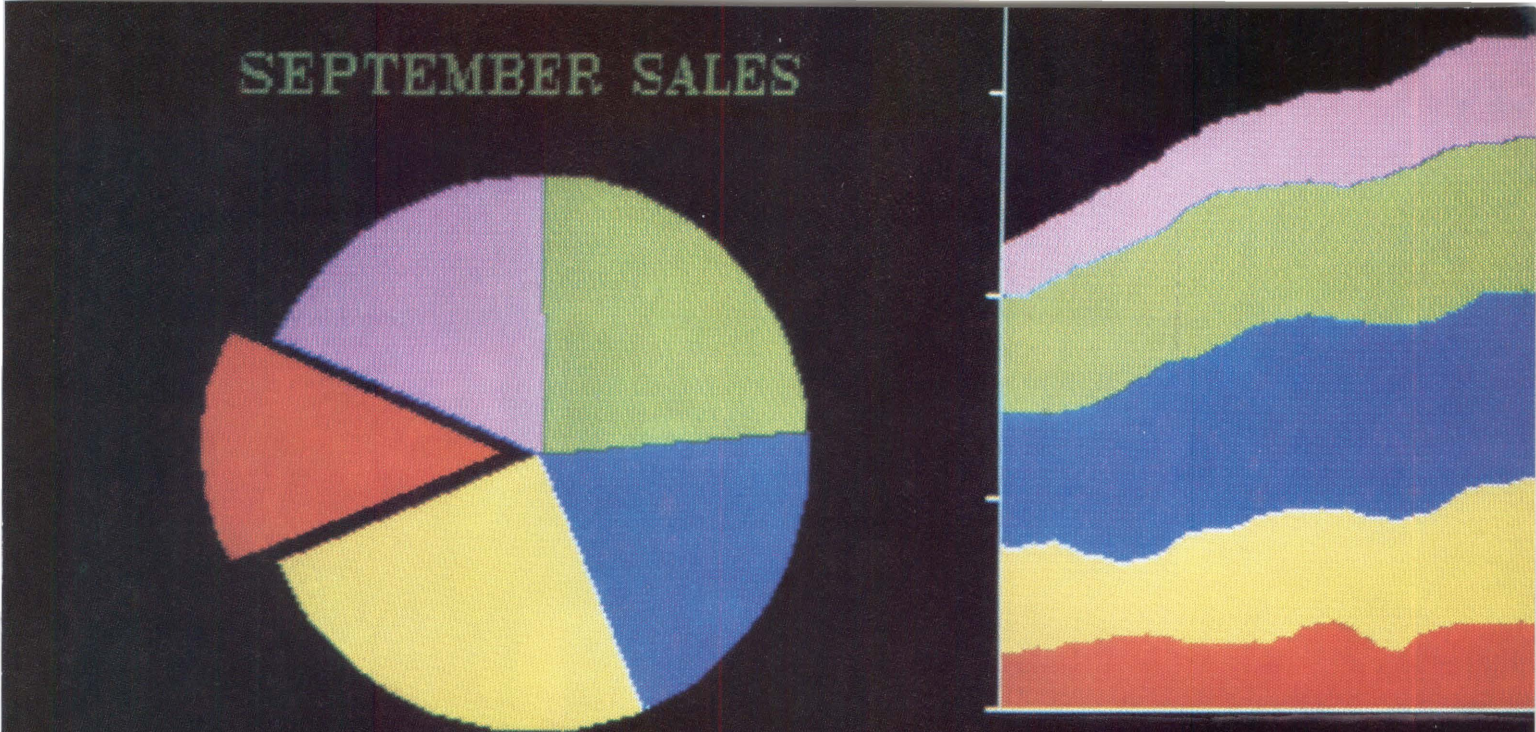
A conversion can be initiated by the A-D system by either issuing a software command or by software enabling of an external trigger source input. Once enabled, any transistor transistor logic (TTL) compatible signal can be connected to the external trigger input to initiate conversions. This is usually done by using a programmable realtime clock, but any external trigger source may be used. Conversions will be initiated on the high to low transition of the input signal. These two triggering modes allow the user to trigger the A-D subsystem seven different ways.

The RAM channel gain list file multiplexer design of the A-D system offers data to memory throughput rates twice those previously available for LSI-11 based data acquisition systems, and a board architecture allowing data transfers over the Q-bus and an external path. With standard LSI-11 data acquisition systems, A-D word conversion is transferred from the A-D system over the Q-bus to memory, and transferred a second time from memory over the Q-bus to a storage device such as a disc. As the speed of a 250 kHz ADC increases, the Q-bus bandwidth can become totally involved with the data acquisition function, leaving minimal availability of the Q-bus to handle other duties, such as moving programming instructions from memory to the CPU.

The A-D system provides a feature to eliminate this constraint, a dual ported design. One A-D system port is a standard Q-bus interface so that the DT3362 can be programmed to transfer data like other standard Q-bus devices. The second port is an external port which can be used for DMA data transfers directly to a companion dual-ported memory board, the DT3369. When the A-D system external port is used to transfer data to dual ported memory, the Q-bus is needed only to move data from memory to disc. It is therefore free to devote more time to the processor and other peripherals on the system, enhancing system level performance.

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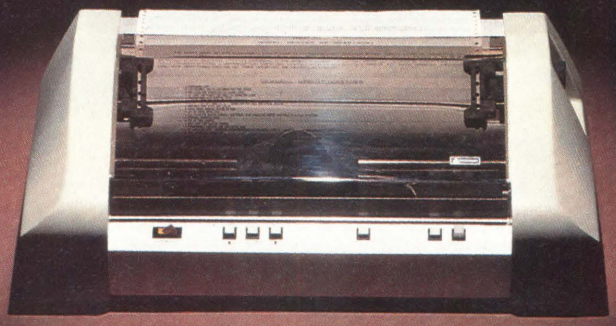
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TALKING CONSOLE MONITOR ALERTS FIELD SERVICE

A microprocessor and speech synthesizer are melded to produce a system monitor that can detect fault conditions and place a phone call for help

by Dan J. Samuel

As more industrial and commercial installations automate processes that once were entirely manual, there is greater need for reliable, independently intelligent computer systems. This is particularly true of unattended installations and those in hostile environments. Although great advances in machine reliability have occurred at the component level, it is still not possible to guarantee fully accurate operation at all times. A self contained system often requires the presence of an operator at the installation to oversee routine operations and step in if necessary when an unexpected event takes place. Around the clock monitoring can be expensive and inefficient, especially when the operator's skills are rarely needed.

One usual solution is use of a less qualified operator to monitor the equipment, a dangerous technique that often results in the wrong corrective action, with potential for increased damage to the process. Another approach is to eliminate supervision and accept instead a significant amount of downtime until a qualified operator arrives to make needed adjustments. Excessive delays can be encountered, however, if the error is not discovered immediately.

Although at first glance a modem might seem to offer a means of remote control, it is not a complete solution. There remains the need for a monitoring device that actually detects and reports failures. Without this monitor, the system must be interrogated regularly to discover malfunctions. Apart from the needless expense for operator time, interrogation and diagnosis can tie up the system, creating downtime at regular intervals. An ideal solution would be to station an experienced operator with the system at all times. Realistically, this is not always possible, especially at remote or hazardous locations.

If the problem is too complex for the ICC to solve on its own, it next can telephone an operator and report the current status of the system by means of synthesized speech.

An intelligent communications controller (ICC) can simulate the ideal problem solution in many situations. The ICC can be installed as a full-time system monitor that continually watches for abnormal events. When an abnormality is recognized, the ICC first tries to correct the problem by following stored instructions. If the problem is too complex for the ICC to solve on its own,

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it next can telephone an operator and report the current status of the system by means of synthesized speech. The operator, who otherwise need not be concerned with system operation, can then gain access to the system and supply instructions using the telephone keypad. Alternately, the operator can access the ICC through its integral modem. Using either method, remote diagnostics are run to isolate the problem with minimal downtime. Then, if a service call must be made, the serviceman knows the exact problem in advance and can bring the appropriate repair equipment and spare parts, perhaps saving an additional trip to the site.

The SLC II is one such ICC unit that interfaces to a system through an RS-232 port or a 20-mA current loop. Because it is designed for installation between the system processor and its console, the unit can interface with virtually any system (Fig 1). It issues operator commands directly to the system processor, as though they came from an operator at the console. A remote terminal can access the system as though it were the system console without interfering with normal console operation. Since most systems routinely report problems at the console, the ICC is ideally located to trap error messages and act on them.

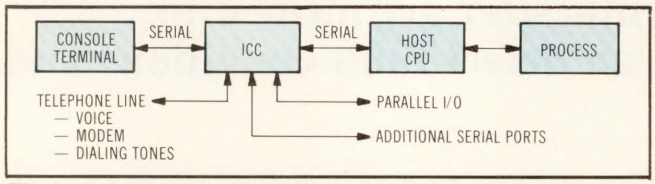


Fig 1 ICC interface. Normal operation is transparent and maintains link between console terminal and host computer. ICC acts as "switchyard" that can redirect transmissions and generate commands in response to messages from host, telephone, or ports

After trapping a problem message, the unit first tries to correct the error by issuing a sequence of console commands. It can distinguish problems that might be solved locally (eg, by restarting the system) from those that require direct operator intervention. When a serious problem occurs, the ICC can initiate telephone calls to locate an operator and communicate the problem using synthetic speech over a normal telephone line. The operator issues commands through the telephone keypad, and the ICC reports their effectiveness. It can be programmed to report errors immediately, or to accumulate messages and report them at a convenient time.

When a serious problem occurs, the ICC can initiate telephone calls to locate an operator and communicate the problem using synthetic speech over a normal telephone line.

Besides helping to maintain 24-hour support for unattended systems, an ICC can assist with remote testing and remote diagnosis. An applications engineer often must spend considerable time on the telephone, leading a customer through a diagnostic in order to isolate a problem. Frustration mounts if the customer cannot understand the instructions or interpret the results, particularly when system reliability is a primary concern. By giving application engineers direct access to the system, an ICC aids in locating problems and making repairs. Also, since the ICC console can be left attached at the installation site, customers can watch commands issued by the engineer as a tutorial in using the system.

...since the ICC console can be left attached at the installation site, customers can watch commands issued by the engineer as a tutorial in using the system.

In the interest of providing a natural interface, speech synthesis was selected as the obvious primary means of output. Research indicates that voice response systems are more effective than blinking lights or video displays. Pitch excited, linear predictive coding was chosen to give the highest available quality. Full word synthesis limits the vocabulary to about 1000 words, but it has a decided advantage over state of the art phonetic speech. In addition, the same hardware that supports full word synthesis can be used in other applications that need a larger vocabulary at the expense of speech clarity.

In the case of ICC input, speech recognition was considered, however current technologies do not recognize a significant vocabulary that is independent of the speaker, and so this option was postponed until better techniques are available at low cost. Microphone replacement, tone generator attachments for rotary dial telephones make practical use of telephone dialing tones as the usual ICC input. Combining synthesized speech output with telephone keypad input makes possible a high quality, unambiguous, 2-way interface between the ICC and the operator, with no need for additional equipment.

At unattended locations, in hostile environments, or whenever process control must continue without manual supervision, the intelligent communications controller removes any need for the operator to be present...

The ICC uses a 6502 microprocessor, five serial channels, 4k bytes of nonvolatile memory, and a 300-baud modem with automatic dial/answer capability and a tone encoding/decoding interface that connects directly to the telephone network via an RJ-11 modular jack (Fig 2). In normal operation, the microprocessor monitors all serial communication from its five physical ports. At any given time, the ICC recognizes two logical channels: the console terminal and host computer. These logical channels can be any combination of physical ports and also redefined dynamically to access different system functions.

The processor maintains a transparent link at all times between the console port and the host port. This

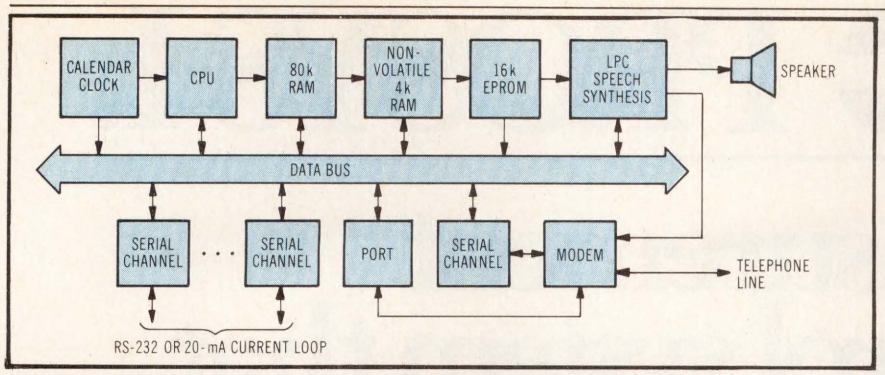


Fig 2 ICC block diagram. 6502 microprocessor monitors all communication via five physical ports that are configured as two logical channels

allows the console to retain functional control of the host. The ICC also constantly matches the input stream from the host against stored character sequences, called keys. When a key is detected, the unit immediately responds by performing a specified action that can be as simple as sending a character sequence to one or several ports, or as complex as initiating telephone calls, generating synthetic speech, and receiving directives via dialing tones. New software can be downloaded into the unit at any time through its serial channels. Once programmed, it maintains all instructions in battery backup memory to ensure system integrity.

The use of an intelligent communications controller such as the SLC II can add flexibility to any computer system by allowing simple and direct access across a voice grade telephone line. Speech synthesis makes it a versatile means of maintaining direct contact with a remote operator. At unattended locations, in hostile environments, or whenever process control must continue without manual supervision, the intelligent communications controller removes any need for the operator to be present, while providing nearly complete process monitoring and automatic control.

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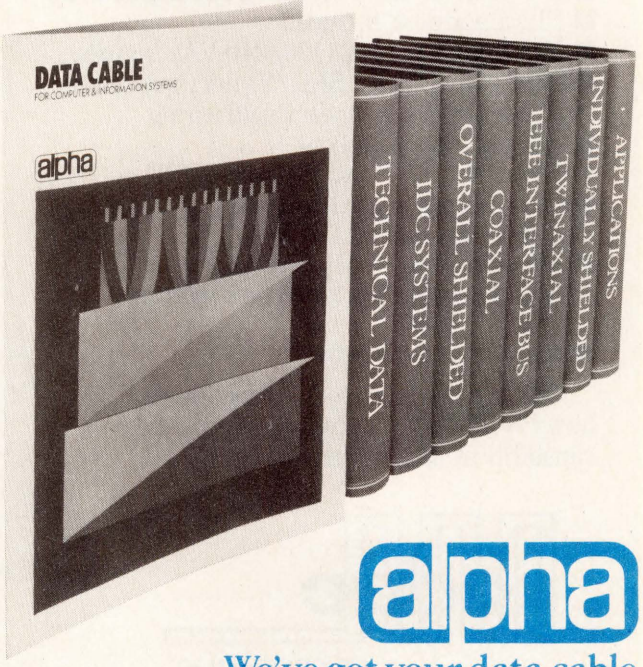
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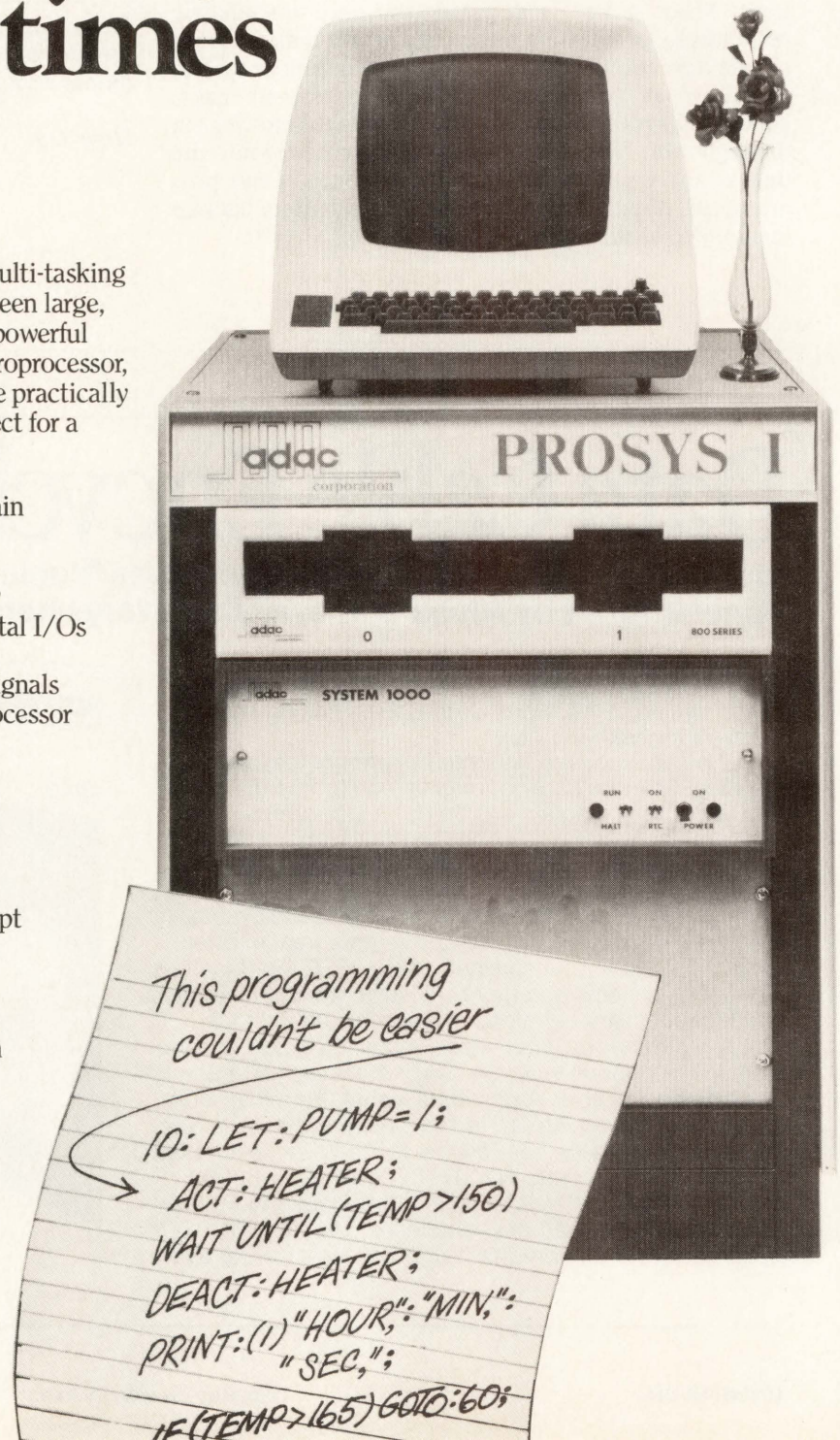
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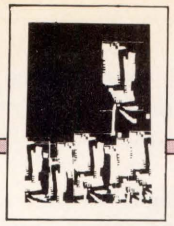
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AIRBORNE DATA ACQUISITION SYSTEM

Modest power consumption and small size of microcomputer make airborne, industrial grade data acquisition systems a viable alternative to more primitive analog recording techniques

by Dean Billing

Small size and modest power consumption recommend microcomputers in instrumentation systems. As a design element, a microcomputer can form the core of an effective and powerful data acquisition technique. A particularly interesting design is an airborne data acquisition system mounted in a Cessna 206 light aircraft and used to gather air quality measurements. The design parameters are quite restrictive because of constraints on its size, weight, and power consumption.

The Cessna aircraft was already equipped with electronic instruments and probes to measure chemical and particle pollution in the air. Previously, all data from the instruments were recorded on a simple data logger that used a 20-channel analog to digital converter and scanner. From a standpoint of accuracy and flexibility, this arrangment leaves much to be desired. The scanning pattern across the channels was not uniform enough to serve as a reliable time base. There were no data provisions for external digital input or serial data input. Some digital data had to be converted into analog signals and recorded on unused data channels. Furthermore, in order to extend the accuracy of the readings, it became necessary to determine very precise locations of the aircraft while recording in-flight data. This old data logging unit was not sufficiently precise, which contributed to the decision to develop a customized computer unit.

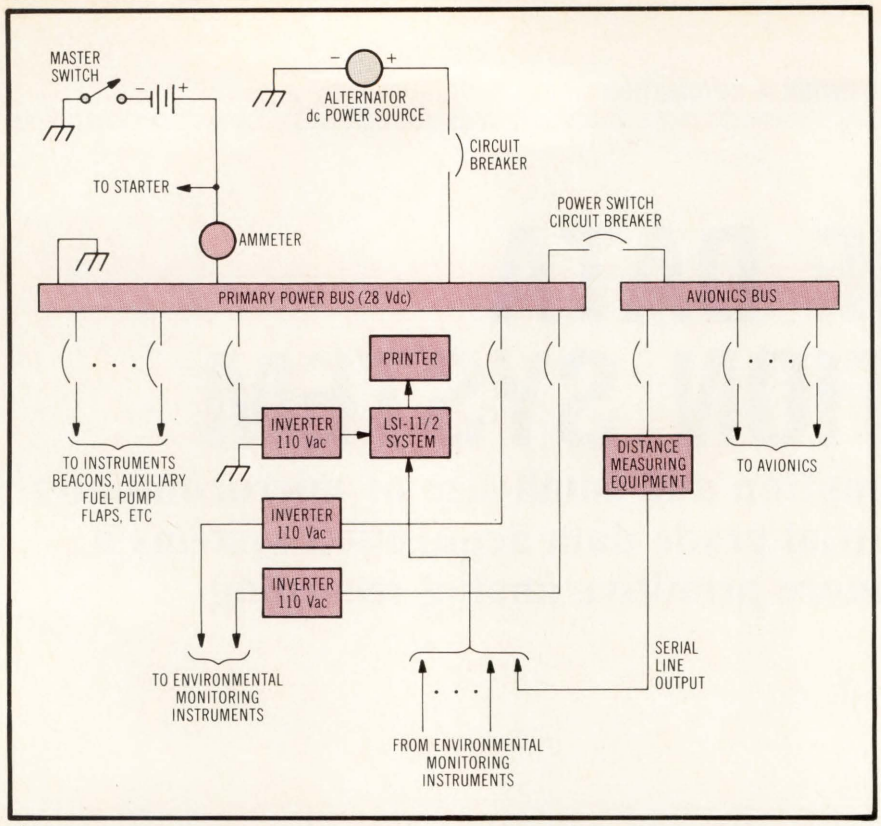
Dean Billing, owner of Solve Consulting Firm, 1815 Peterson Lane, Santa Rosa, CA 95401, is involved with software and hardware systems development for engineering companies in the northern California region. Mr Billing has 15 years experience in software development, including prior positions with IBM and Hewlett-Packard. He attended California State Polytechnic College, graduating with a BS degree in Mathematics.

Aircraft imposes design constraints

The unit has a pre-imposed weight limit of 25 lbs, (11 kg) and has to fit in a standard 19″ (48-cm) equipment rack. It has to record one hour of data, at the rate of one data reading per second, without operator intervention to change the recording medium. The airborne system requires a minimum of 20 analog channels, differential input, in the ±10-V range with an accuracy of 10 mV. Due to limited power available on a light aircraft, power consumption is restricted to not more than 150 W on a 115-V line.

The computer system slides out of its mounting on the aircraft; it can then be taken to a trailer or even connected to standard house current.

From an electrical standpoint, although the aircraft has 28-Vdc power, 110 Vac power was used to drive the unit. Airborne meteorological instruments attached to the unit also require 110 Vac for operation; in addition, this choice simplifies ground based operation. For simplicity and reliability, the data acquisition program



Airborne microcomputer system. Inverter supplies 110 Vac from primary power bus. LSI-11/2 spools data from environmental monitor and distance measuring equipment onto magnetic tape. Printer supplies hardcopy backup

is implemented in read only memory (ROM), and for ground based operation, the unit remains capable of general purpose operation.

Suitable equipment is key to success

A lightweight magnetic tape subsystem and a matching, compact microcomputer was needed. The design uses the LSI-11/2 microcomputer and a TU58 tape cartridge subsystem, both manufactured by Digital Equipment Corp. The LSI-11/2 can run the RT-11 operating system, and although it is not the usual practice, the TU58 can be used as a system device under RT-11 to run general-purpose programs using high-level languages, as well as assembly language programs. The TU58 has sufficiently light power consumption for the job, and can record one hour of data without operator intervention. Further, the entire TU58 subsystem, including two tape drives, weighs only 2 lb (0.9 kg).

As a ground based unit, the system has been used to duplicate copies of the data tapes that were recorded in the air.

The chassis for the system is an Interlock series 30, an all-aluminum case designed for strength at minimum weight, with snap-in side panels, slide-in top and bottom plates, and provisions to mount components anywhere within the case. With front and back panels machined to accept switches, connectors, lights, and displays, the case weighs only 9 lb (4 kg).

For ease of design, weight, and efficiency, switching power supplies were chosen. They are well filtered, have very low ripple and noise, and come in completely shielded aluminum cases that are easy to mount. They are rated at 75% efficiency and can operate over a wide input voltage range.

The mounting for the LSI-11/2 is a standard 12-slot Digital backplane. Along with the CPU board, 16k words of memory and a 4-line serial interface are installed in the backplane. A Digital Pathways date/time card, and 16k-word ROM card also are installed for the time logging and the data acquisition program.

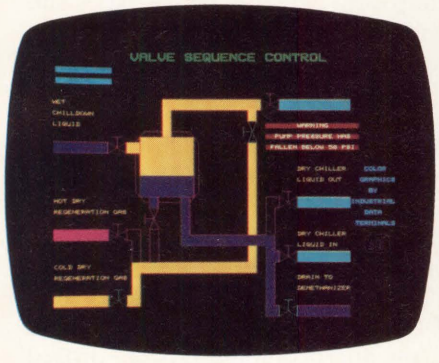
Certain design criteria were dictated by the previous data logger, since a junction box for this unit was already installed in the aircraft. The special connector to fit the junction box was wired to an ADAC analog to digital converter and its multiplexer. Another ADAC board, configured for 48 bits of digital input and 16 bits of digital output is also used: the input channels are connected to switches for tape identification code, event code, and the like; output goes to a custom-designed display multiplexer driver board.

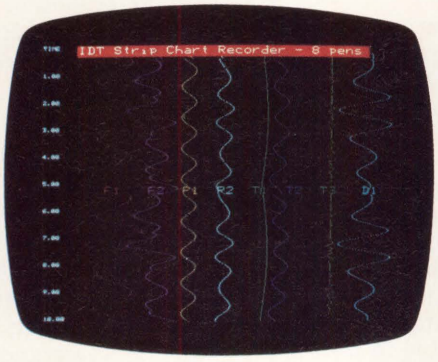
...the system has been sufficiently shielded so that there is no interference with the aircraft radio navigational instruments.

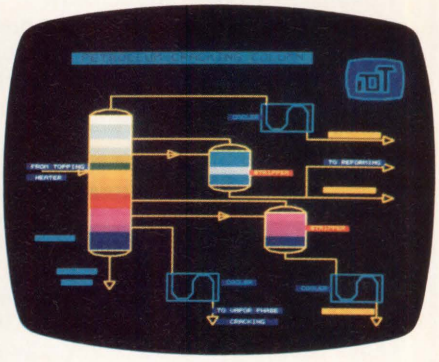
Using an MXV11-A2 chip set, a custom interface board enables either a hardwired branch to the first instruction of the ROM based data acquisition program, or bootstrapping of RT-11 when the system is used for general-purpose operations. Other custom boards are mounted external to the backplane. One contains a crystal-controlled oscillator as a system clock used for both the liquid crystal displays and as a realtime interrupt for the operating system, since the inverters on the airplane could not guarantee precise frequency stability.

The data acquisition program is a 25-task, priority directed monitor. Tasks include reading input channels, recording data, monitoring tape status, and activating the relay for the tape alarm. There are interrupt service routines for input and output to the TU58, output to the serial printer port, and for completion of analog to digital conversion. Each input/output device is double buffered to enable input/output and record processing to proceed simultaneously. Data for a tape record are buffered for eight seconds, or eight record intervals if

Bubble Breakthrough





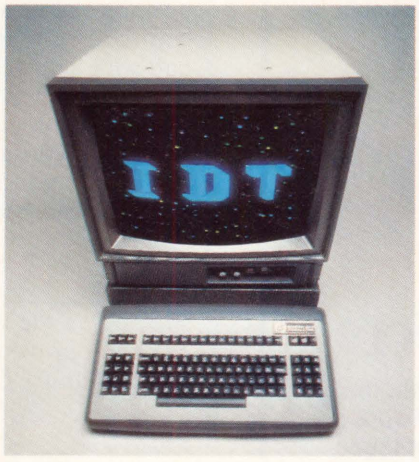


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the "record interval" switch is on a different setting. It takes slightly more than a second to write a 512-byte block of data, and because a block holds eight seconds of processing, there is no speed problem with the tape system. Data are recorded in digital blocks, not at constant speed.

By choosing a microcomputer with software and minicomputer family compatibility, and with lightweight mass storage units, it is possible to use a computer system developed primarily from off-the-shelf components that meets exacting weight, space, and power consumption limitations.

Ground based operation is easy to set up. The computer system slides out of its mounting in the aircraft; it then can be taken to a trailer or even connected to standard house current. As a ground based unit, the system has been used to duplicate copies of the data tapes that were recorded in the air. The system is used occasionally on the ground to dump data gathered on the tapes and to give researchers an immediate profile on the samples; however, data reduction is not being done currently in the field.

Performance suggests a general purpose role

To date, the airborne computer system has been used in four field operations: two missions in the Midwest and two in California. The system has collected so far approximately 150 hours of data. The unit seems to be insensitive to power fluctuations found on the lightly regulated ac bus of the aircraft inverters. Throughout the field operations, the microcomputer system proved to be reliable; it has performed as expected, and has delivered data with the required degree of accuracy. In addition, the system has been sufficiently shielded so that there is no interference with the aircraft radio navigational instruments.

Microcomputers are used successfully in a variety of portable applications. By choosing a microcomputer with software and minicomputer family compatibility and with lightweight mass storage units, it is possible to use a computer system developed primarily from off-the-shelf components that meets exacting weight, space, and power consumption limitations. Such a system need not be limited to a special purpose role, but by careful design it can be used for general-purpose applications as well.

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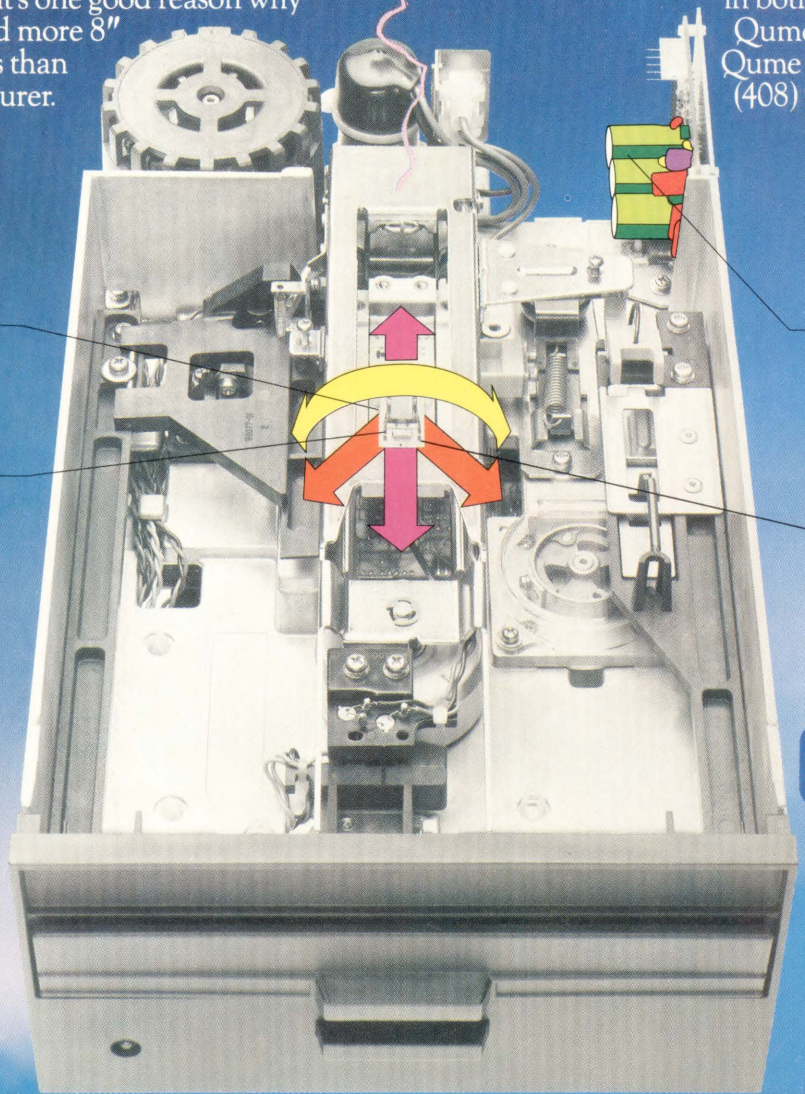
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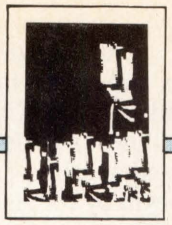
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AUTOMATED DESIGN OF COMPUTER BASED SYSTEMS

In today's printed circuit design environment, the question is no longer whether or not to use a CAD system, but how and when to use it

by Shawn Spilman, Technical Editor

For more than a decade computer aided design has reduced the time to prepare schematics and wiring diagrams, ensuring that drawings meet quality standards and freeing manpower for more creative design tasks. Once a computer aided design system has captured drawings in an intelligent data base, this information can be used to produce a net list, drilling tapes, insertion tapes, and many other design or manufacturing aids. If a design can be modified or customized to meet particular needs, the schematic data base provides a starting point for interactive development of a whole family of related products.

Digitizing

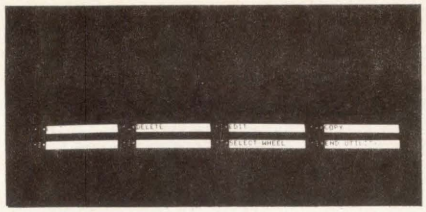
The digitizing step enters a precise description of a circuit layout or schematic into the computer data base, where it forms a numerical basis for virtually all subsequent design work. Individual points on a coordinate grid and individual line segments are basic graphic elements used to represent the circuit. More complicated elements such as closed shapes and curved lines are constructed from the basic lines and points. For example, a signal trace is entered by digitizing a path center line and assigning it a width. Most systems also treat text as a basic graphic element.

Digitized information is organized into levels within the data base. Specific data included in each level can vary. Information for each layer in a multilayer board is usually segregated into a dedicated level, as are ground and voltage plane data, drill hole coordinates, data for the pad master, component outlines, and other related information that is ultimately used to produce separate layers of artwork. Levels can be displayed individually or superimposed in various combinations. Superimposing a level of component outlines with a board outline level produces most of the information needed in an assembly drawing, for example, and the board outline level combines with drill symbols to form the basis for a detail drawing.

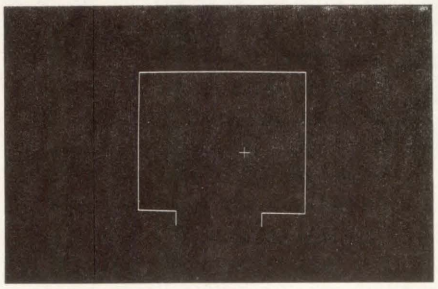
Accuracy of the digitized information is ensured by using the same grid for each level in the data base and accepting only exact grid coordinates, which guarantees that all layers are always in precise registration. Conductor width is also precise, and a drill hole will be accurately positioned within its pad since both use the same coordinates. Restricting trace ends and vertices to exact grid points does not reduce flexibility because grid spacing can be changed at will.

Placement

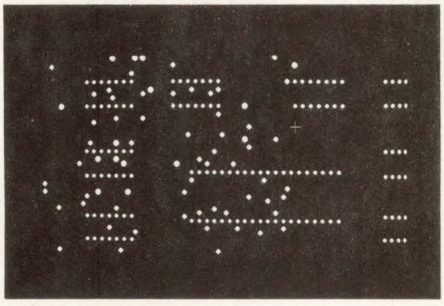
After digitized schematic and printed circuit board (PCB) geometry information have been entered into the data base, individual components must be positioned on the board. Designers perform manual placement through a trial and error procedure that takes many iterations to achieve the uniform signal flow that is needed to optimize subsequent design steps. During each trial iteration, a manual layout designer must keep track of all the various gate or component alternatives, along with any physical constraints imposed on part locations.



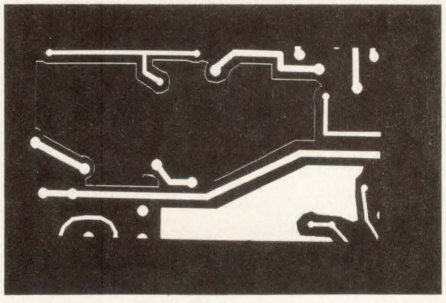
Interactive prompting begins session



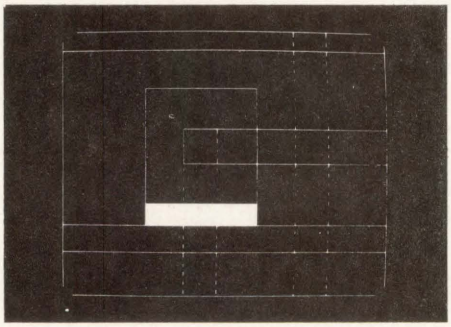
Operator enters PCB outline



Digitizer simplifies pad positioning



Creating ground plane



Design rule checks verify minimum spacing

Using a computer aided design (CAD) system, designers instead rely on interactive programs that manipulate the digitized schematic and data from the design library to work toward the simultaneous goals of minimum conductor length, minimum complexity, and uniform part density. The programs begin by roughing out an initial placement scheme that allocates gates to integrated circuit packages and is optimized to use the fewest interconnections. Under direct operator control, software next improves on the trial layout by exchanging individual parts and groups of parts. At the lowest level, devices are "reassigned," or moved from one component package to another. A higher level of interchange swaps the positions of entire packages or even neighborhoods of packages.

After each exchange at either level, the software evaluates layout complexity by counting the number of interconnections that cross arbitrary horizontal and vertical partitions. It backs out of any exchange that increases complexity by producing more crossings and retains any exchange that leads to fewer crossings. When the number of interconnections crossing partitions is not affected by an exchange, additional partitions can be added to split the board into smaller regions and refine the evaluation process.

Designers can evaluate a trial placement scheme by viewing a *rat's nest* display that diagrams the components in their sites and shows interconnects by means of straight lines passing directly from pin to pin. For manual refinement of an automatic layout, rat's nest displays help to identify congested areas and suggest changes that might reduce clutter. Using a process called *rubber banding,* designers can drag components across the display, tracking them from point to point while the CAD system stretches and contracts the interconnects to maintain the signal continuity of a dynamic rat's nest display. Most large CAD systems offer the rat's nest capability; however, only systems with raster displays can perform rubber banding.

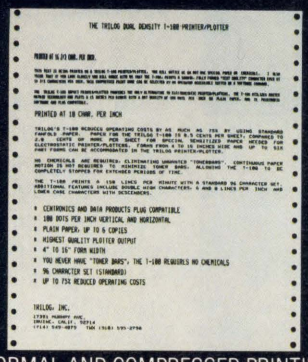
Automated placement consumes substantial amounts of computer time but generates a near optimal placement scheme with relatively little manual intervention. The length and complexity of interconnections are minimized, upon completion of initial placement, and the location of every component package is known. Gates are assigned to packages at this stage, discrete components are positioned, and straight lines that run from pin to pin represent all interconnection wiring. These results form a starting point for routing the interconnections.

Routing

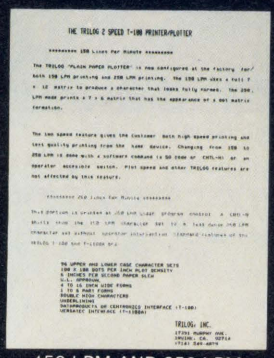
Routing is by far the most tedious and time consuming operation in a manual PCB design. Most CAD systems apply a sequence of router algorithms to optimize signal connections according to designated criteria such as maximum success of automatic routing, minimum total connector length, limited trace density, a minimum of feed-throughs or "vias," or best state from which to complete routing by hand. They also accept such constraints as tooling regions that must be avoided. Although few designs allow fully automatic routing, 90% success is not unusual, and interactive aids help to complete any connections that remain to be found.

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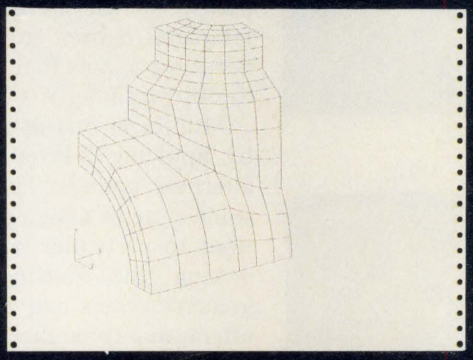
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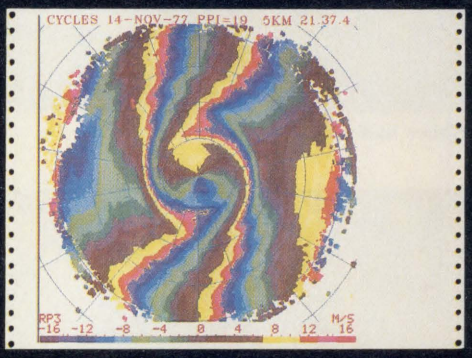
NORMAL AND COMPRESSED PRINTING



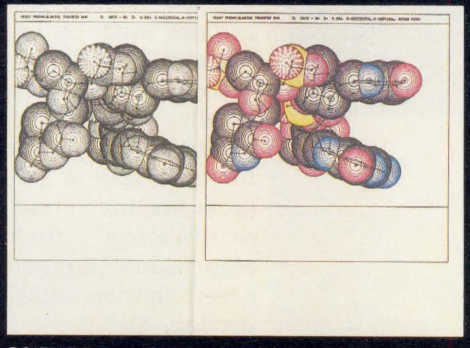
150 LPM AND 250 LPM



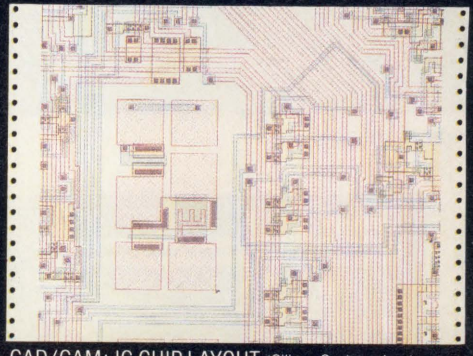
HI RES. STRESS ANALYSIS (PDA Eng.)



RADAR WEATHER MAPPING



SCIENTIFIC: MOLECULAR STRUCTURE (MIT)



CAD/CAM: IC CHIP LAYOUT (Silicon Systems Inc.)

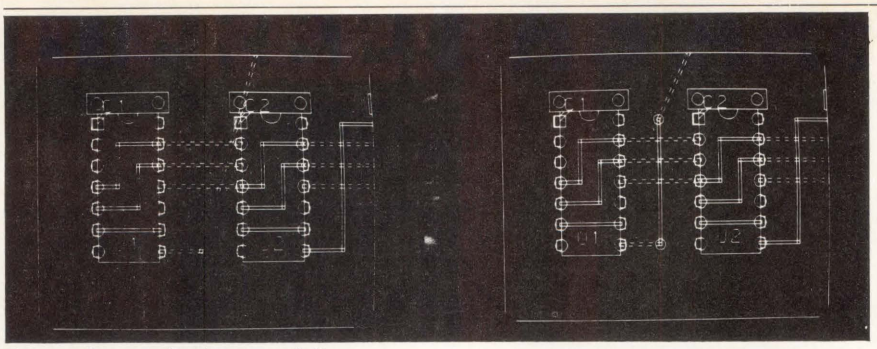
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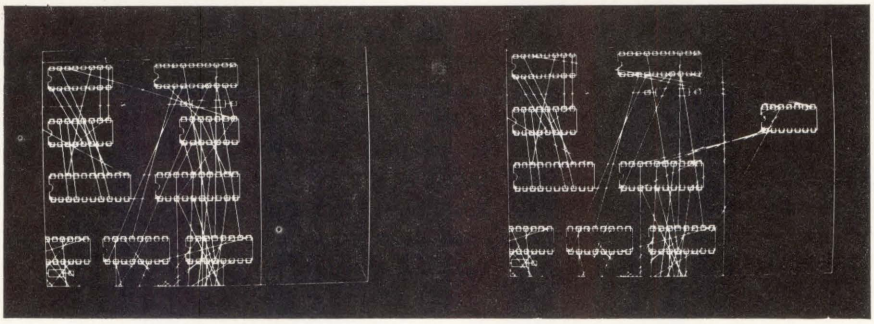


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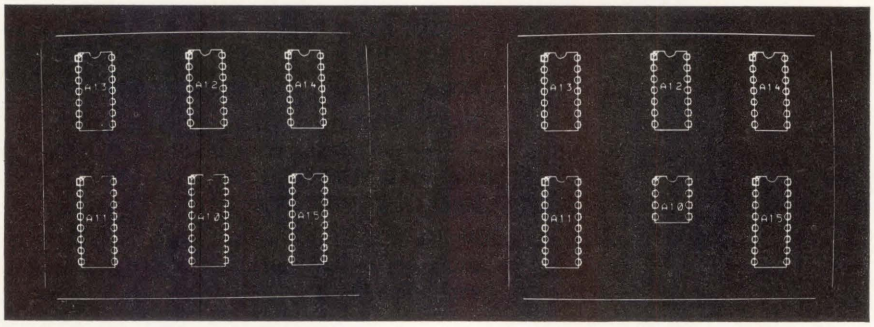
CIRCLE 93 ON INQUIRY CARD



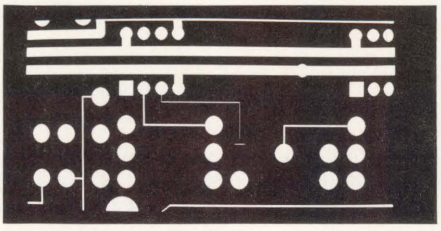
Interactive conductor completion



Rat's nest and rubber banding



Automatic component change



Interconnecting pads

A typical 3-stage routing package first uses a *strip connection* or "channel" program to locate long horizontal or vertical paths on a single layer. Strip connection handles major bus runs, short "in-line" signal paths, most power or ground traces, and runs to external connectors. Next, a *fast line* program roughs out the bulk of a routing task by using horizontal traces for connections on one side of the board and vertical traces for connections on the other side. An *exhaustive maze* algorithm completes the routing process by performing a comprehensive geometric search to make connections that were not established earlier.

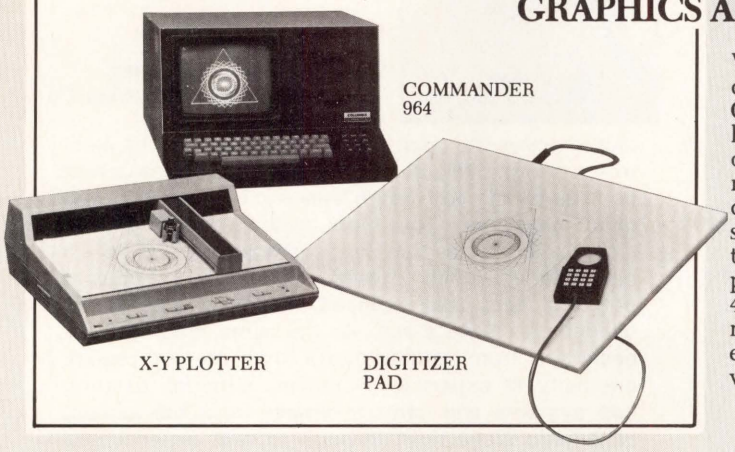
Algorithms can be applied repeatedly, and in various sequences, to yield a high rate of connection success. Rerouting occurs automatically whenever the path for an interconnection must intersect a trace that was defined earlier. Any number of paths might be erased to make a troublesome connection, and other traces might be erased to reroute these displaced paths. Although there is no assurance that ripping up paths to back out of an impasse will improve routing success, occasional backtracking to remove an obstructing trace generally pays off. Other routine algorithms apply squeezing techniques that shove aside bundles of traces to make room for additional paths, or use libraries of wiring templates chosen to give easy connection patterns that are least likely to obstruct later work.

Multilayer boards are best routed by applying 2-layer techniques to alternate pairs of layers. Although some systems assign certain connections to particular layers before invoking the routing algorithms, greater success can be achieved by attempting to connect every lead on every layer. Any leads that remain can be interconnected by hand, perhaps using an interactive rip-up routine and relying on the router software to check for errors. Finally, clean-up processing can modify the layout without regard for optimization constraints to improve manufacturing yield or reduce production cost. Clean-up algorithms typically straighten paths, shorten paths, increase path spacing, and convert 2-layer interconnects to use only one layer.

A design must be revised frequently during the various stages of development, refinement, and implementation. Although rarely needed in the early stages of PCB layout and routing, interactive editing functions become progressively more valuable as work proceeds. Some editing capabilities help to complete portions of a design that the CAD system failed to handle automatically. Layer discrimination and signal highlighting, for example, are used to squeeze in any signal runs that the router could not complete. They point up a critical CAD benefit: the ability to move design elements instead of erasing and redrawing them. Other editing commands will add, delete, or change specific entries in the design data base, such as components or text.

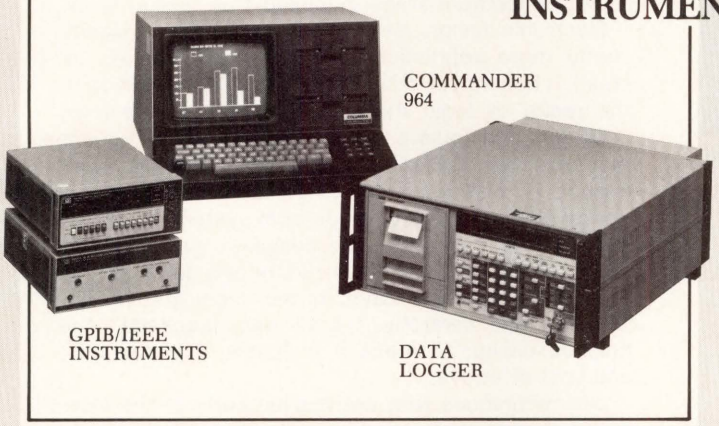
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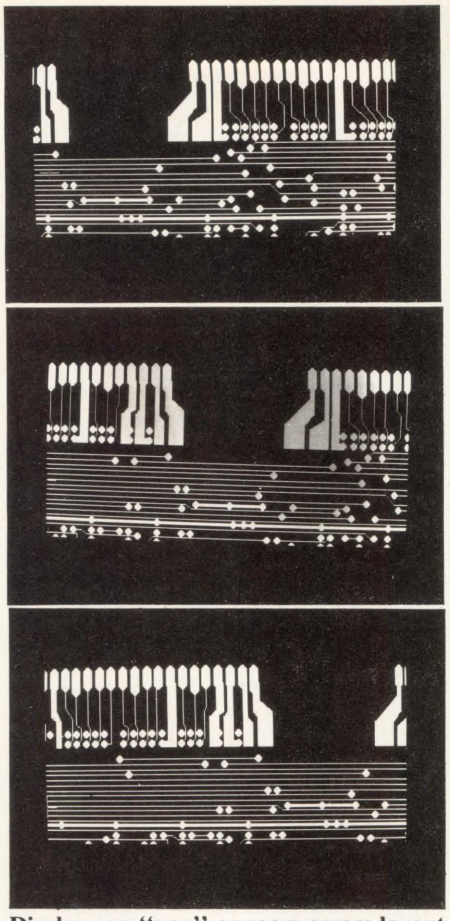
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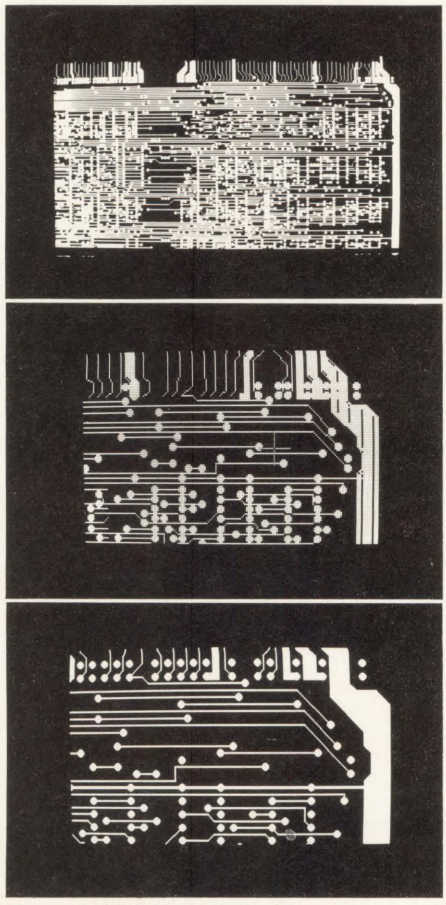
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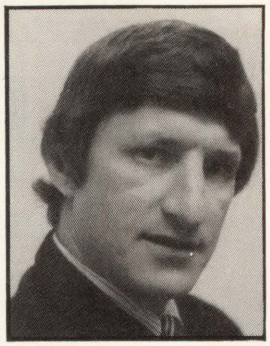


Display can "pan" or roam across layout



Zoom (middle) and magnify options expose detail

"removes the most serious bottleneck"



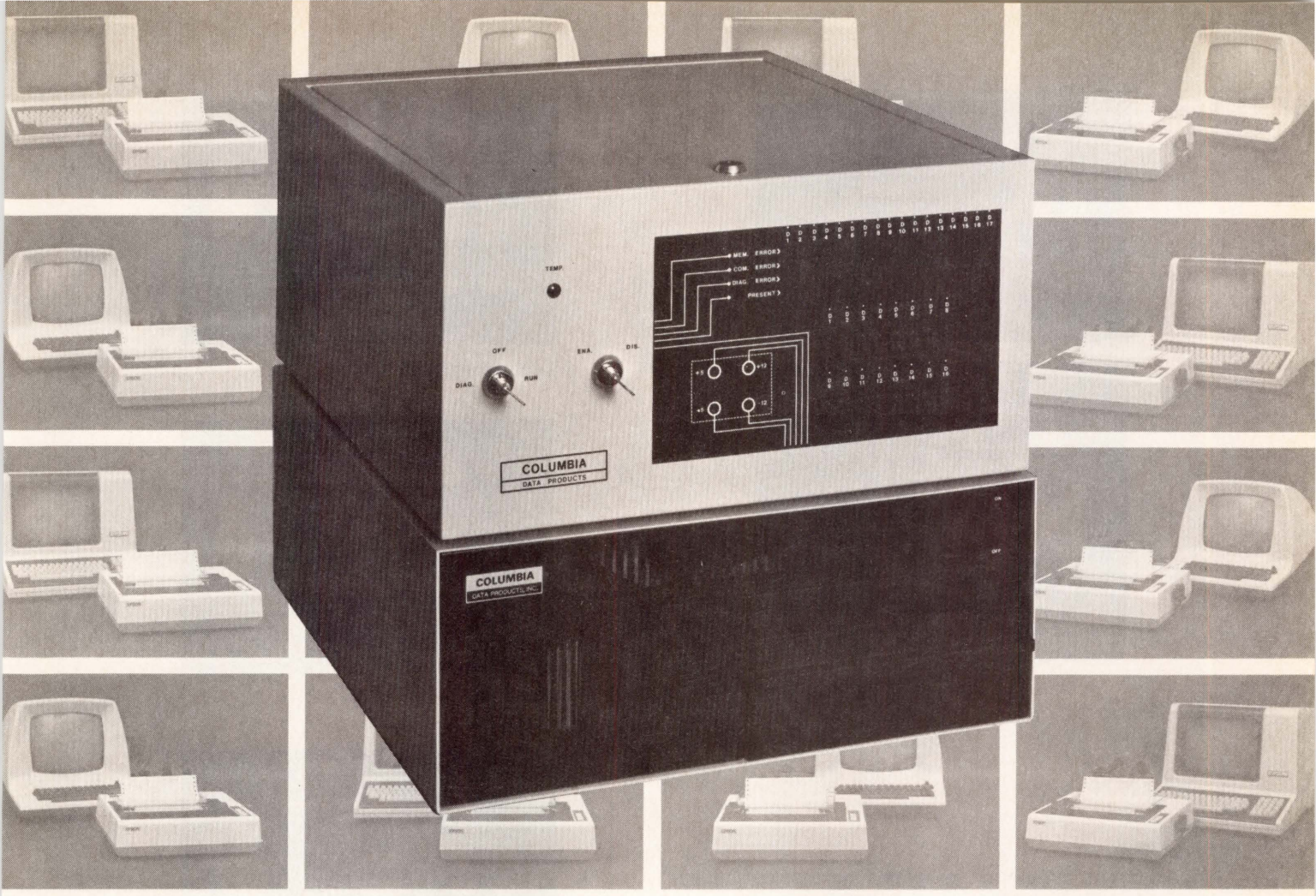
David R. Ryan
Vice President, Marketing
Gerber Scientific Instrument Co

CAD removes the most serious bottleneck in the electronic design cycle by automating drafting tasks that once involved hand drawn lines and by handling most of the repetitive layout work, tedious checking, revisions, and updates that almost always occur before a new product goes into production. It provides a powerful tool that reduces the time and outlay needed to create a PCB. At the same time, it frees designers from routine tasks that do not require creativity or expertise. However, although existing CAD systems will carry a project from the earliest schematic stage right through to final artwork and documentation, the major benefits are realized late in the design cycle and well downstream from the creative, conceptual stage involving true design work.

Electronic design automation has not grown significantly more sophisticated in the past decade; instead, it has moved from the circuit design level up to the realm of logic design. Many of today's logic designers manipulate block diagrams in a process that often resembles computer programming. They occupy a relatively high-level niche in the overall design hierarchy that extends from system architects down to technicians. Logic designers perform their work near the top of the hierarchy and quite early in the design process. Later in the cycle and further down in the hierarchy, technicians "package" the finished design to make it buildable, maintainable, and cost effective.

CAD techniques that are applied early in the electronic design cycle tend to be complex and highly specialized. An automated system that carries a design past the block diagram stage by deriving connection data, for example, would probably constrain a random logic design to the use of one circuit family. It might rule out the use of programmable logic arrays or microcode alternatives to random logic. Ultimately, the system could inadvertently propagate obsolete technology: instead of designing a product to fit the job it must perform, there is a tendency to design the product to fit the CAD system.

A better approach is to view electronic product evolution as a logic design process followed by a packaging process. CAD aids packaging efforts through automated checking and other new capabilities, faster revisions, a chance to apply more criteria for optimization, and an opportunity to bypass the troublesome wirewrap prototype. Designers who are not yet convinced that CAD systems do enough—and do it well enough—to justify their use as a logic design tool can still enjoy almost all CAD benefits in the final stages of an electronic design process.



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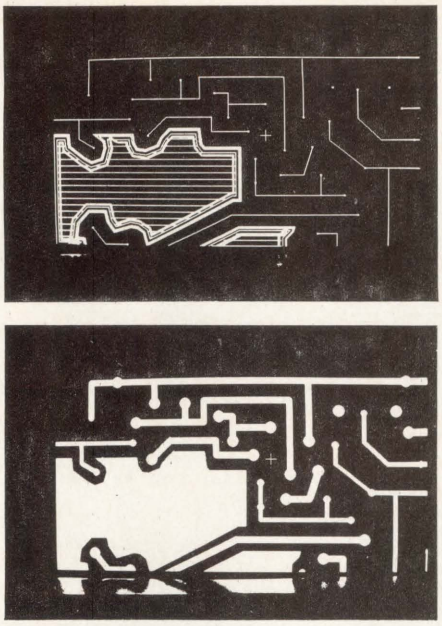
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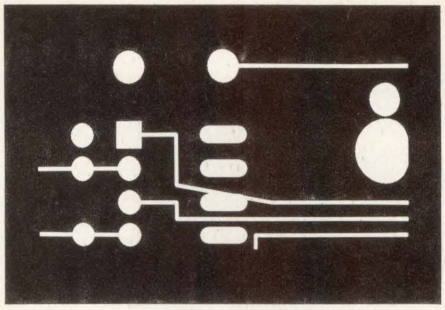
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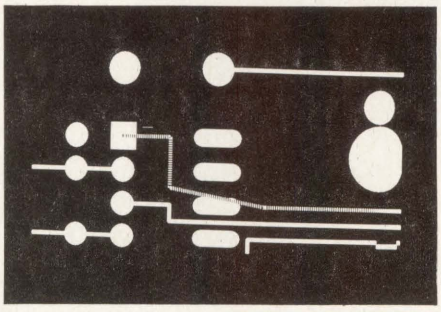
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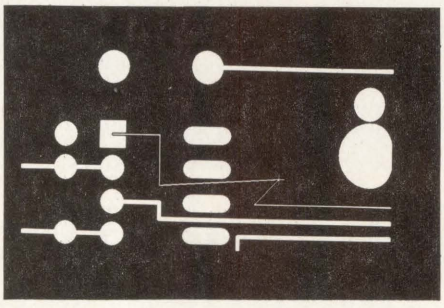
Draw-at-width feature helps establish clearances



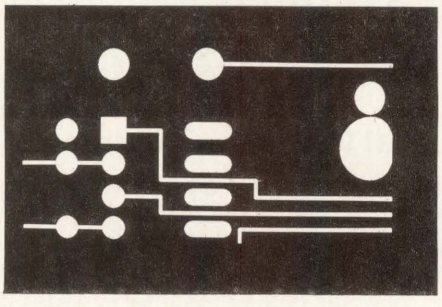
Line through pad



Find line



Rubber-band line



Locate new position

Simulation

Digital circuit simulation programs increase confidence in a schematic and help to uncover design errors at the earliest possible stage. Although design verification is a primary simulation goal, most digital simulation packages also verify that the circuit can be tested, generate test pattern data, and calculate test program effectiveness. Simulation begins with a functional logic check that neglects gate delays and provides a rough analysis of high level design integrity. A detailed verification stage next examines the circuit more closely. Nominal and worst case timing are analyzed; race, hazard, and spike conditions are identified; and a realistic picture emerges to indicate how the device will work after it has been built. Confidence developed by a digital simulation program during design verification leads to fewer design revisions and reduced engineering change orders late in the design process.

Tasks performed by a digital simulator are not complicated, but for typical circuits containing the equivalent of up to 100,000 gates, they do require substantial computing power. The circuit and its derived net list are needed as input. Most simulators identify four logic states: true, false, high impedance, and undefined. During simulation, the program accepts an input vector of logic states, which it places at the inputs of appropriate gates. One gate delay period later, it checks for first level changes at gate outputs. If any changes are found, the program advances another gate delay period and checks for changes at the next gate level. A simulation run most often tests only a few circuit functions by analyzing a few hundred input vectors that exercise those functions. If results indicate correct operation, a subsequent run continues to test additional circuit capabilities.

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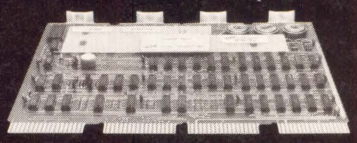
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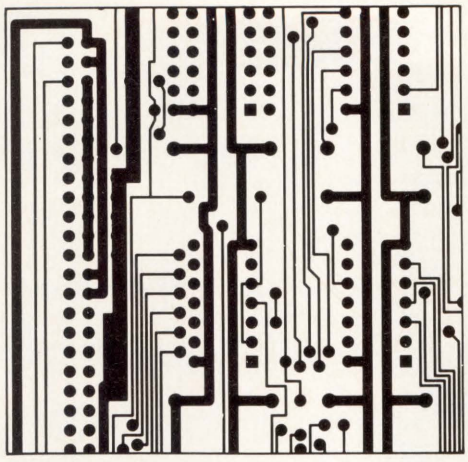
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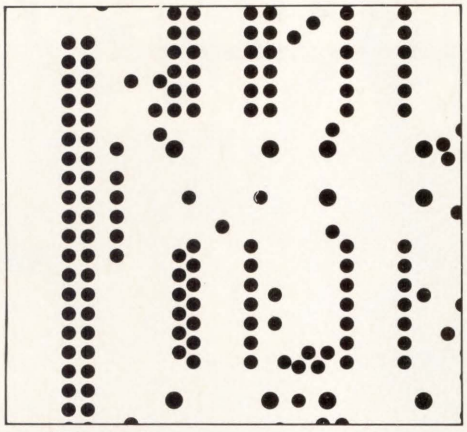
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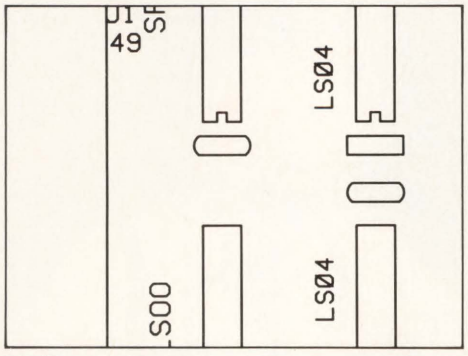
CAD data base produces full-spectrum output



artwork master...

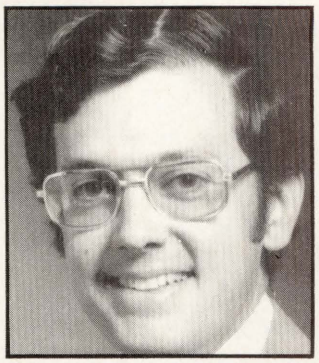


...solder mask...



...silkscreen master...

"a starting point for every subsequent process"



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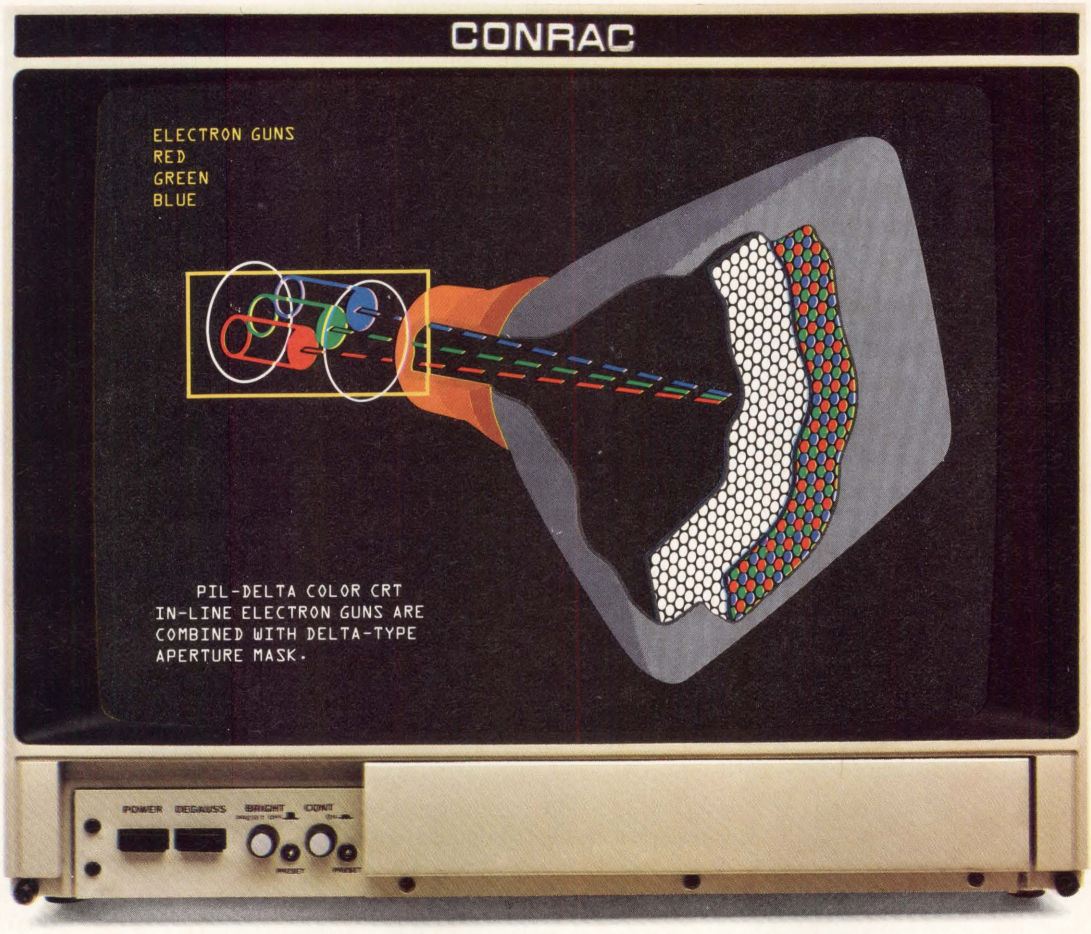
CAD technology is used to design products that touch every aspect of our modern world. From conception through product definition to computer aided production, CAD systems streamline mechanical design and drafting, industrial plant design, cartography, integrated circuit design, and more. Most CAD systems serve many different application areas with the same basic hardware and identical core software, changing only the high level software to adapt to a specialized environment. Basically, at the lowest level, CAD systems store and manipulate lines in a graphics data base. These lines can represent the electrical, mechanical, geographic, or other properties of a product. Within the data base, lines assume appropriate characteristics that customize the system to a particular application.

CAD has had relatively little impact on the way engineers have always applied sound judgment and experience to make design decisions. Instead, its major benefit is a 4:1 or better reduction in turnaround time and a substantial cost savings achieved by automatically enforcing design rules, performing repetitive tasks, and checking for mistakes. With CAD, prototypes are more apt to work correctly the first time, and products can be manufactured to closer tolerances. Its use routinely trims a conventional six-month design cycle to six weeks or less.

For electronic products, a CAD system takes the tedium out of creating schematics by replacing the drafting table with a digitizer, cathode ray tube display, electronic pen, data tablet, and keyboard. Designers communicate with the system using a simple English language vocabulary. They can quickly add, delete, move, or modify drawing elements such as lines, arcs, symbols, and text. Commonly used parts and standard subassemblies can be called up from a customized library. The finished schematic becomes a starting point for every subsequent process to complete the design and to manufacture and support the part. Furthermore, once entered into the CAD system data base, it is easily incorporated into other design projects.

Designers who were at first concerned that CAD systems would constrain their output instead find that CAD gives engineers the same automation technology that draftsmen have long enjoyed. Placing flexible, automated tools directly in the hands of designers leads to a better quality product that is easier to build and test. Not only is the product brought to market sooner, it is invariably more reliable as well. By relieving design engineers of repetitive, tedious, and error prone tasks, CAD systems give them more time to be creative with their unique skills.

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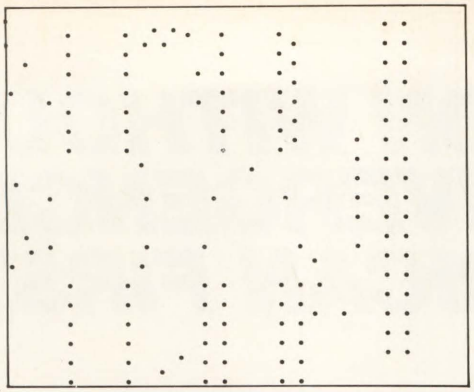
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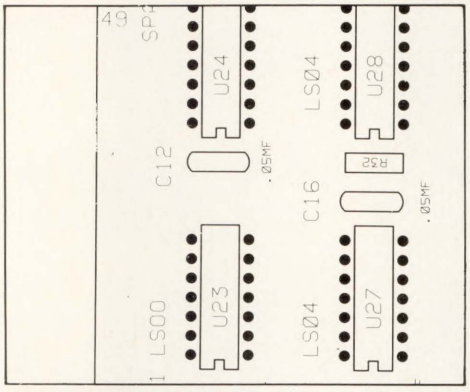
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REFERENCE DESIGNATOR	MANUFACTURERS PART NUMBER	COMPONENT DESCRIPTION
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C2	6547971	33MFD 10V CAP
CR1	1N2283	2283 DIODE
CR2	1N2283	2283 DIODE
CR3	1N2283	2283 DIODE
CR4	1N2283	2283 DIODE
CR5	1N2283	2283 DIODE
CR6	1N2283	2283 DIODE
Q1	4522510	2N5819 TRANSISTOR
Q2	4522230	2N2102 TRANSISTOR
Q3	4522230	2N2102 TRANSISTOR
Q4	4522230	2N2102 TRANSISTOR
Q5	4522230	2N2102 TRANSISTOR
Q6	4522230	2N2102 TRANSISTOR
Q7	4522230	2N2102 TRANSISTOR
R1	5541009	20M OHM TRIM POT
R2	5542198	500 OHM TRIM POT
R3	7650074	5K 1/4 W RESISTOR
R4	7650074	5K 1/4 W RESISTOR
R5	7650095	500 OHM 1/4 W RES
R6	7650095	500 OHM 1/4 W RES
R7	7650095	500 OHM 1/4 W RES
R8	7650081	30K 1/4 W RESISTOR
R9	7650072	2K 1/4 W RESISTOR
R10	7650071	1K 1/4 W RESISTOR
R11	7650074	5K 1/4 W RESISTOR
R12	7650074	5K 1/4 W RESISTOR
R13	7650095	500 OHM 1/4 W RES
R14	7650095	500 OHM 1/4 W RES
R15	7650095	500 OHM 1/4 W RES
R16	7650081	30K 1/4 W RESISTOR
R17	7650072	2K 1/4 W RESISTOR
R18	7650071	1K 1/4 W RESISTOR
R19	7650074	5K 1/4 W RESISTOR
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Business Manager of Integrated Manufacturing Systems Prime Computer Corp

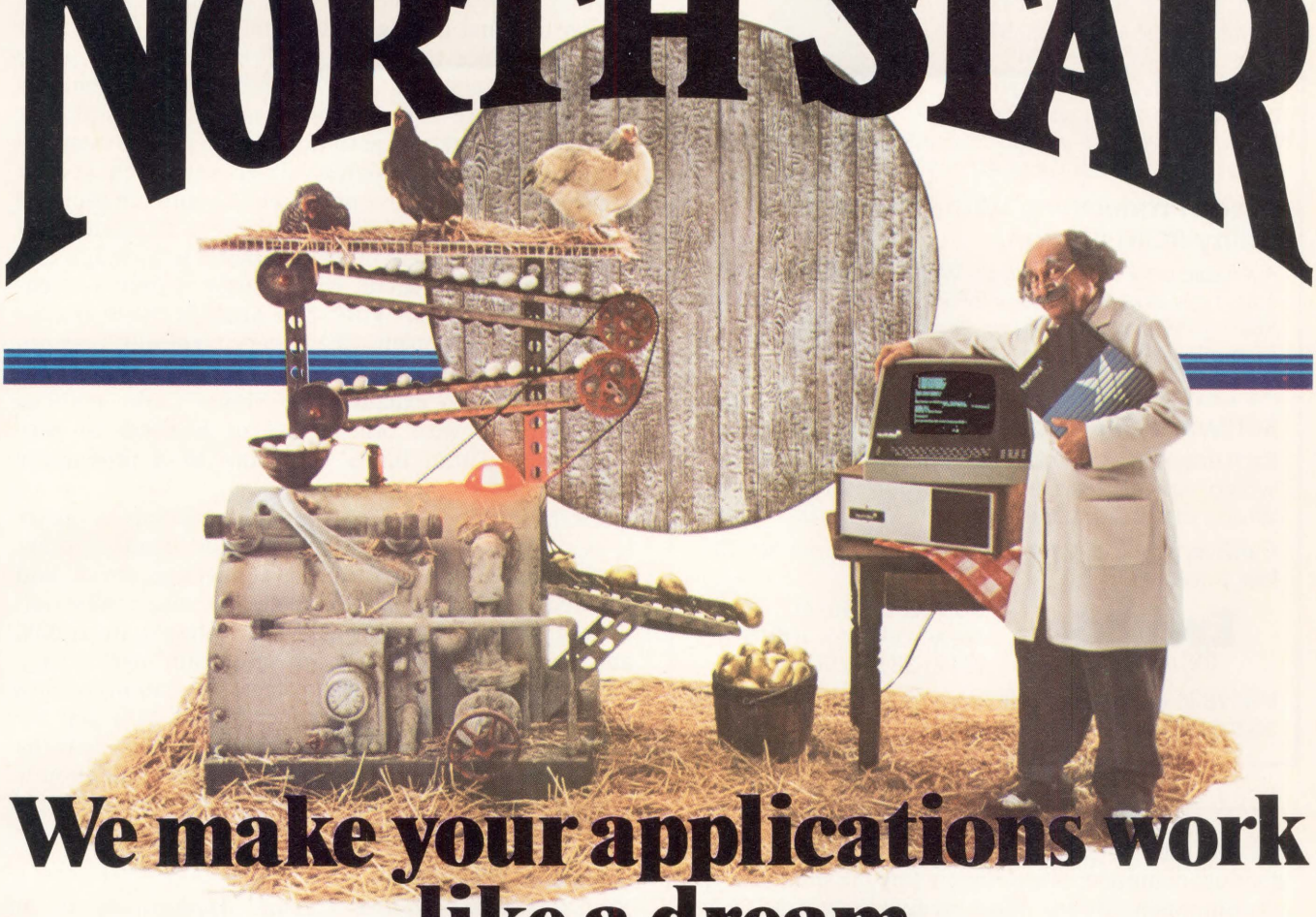
To succeed in today's competitive marketplace, a high technology product needs two attributes: it must offer significant added value, and it must have unique traits or features. Both attributes must be visible so that customers clearly see the value of the product to them and the unique features that distinguish it from competing products. Value and distinguishing characteristics are best added to products at the design stage. Better design tools lead to greater added value and more visible features that can give any product a competitive edge in the marketplace.

Low price offers both significant value to customers and a unique, visible difference from competing products. Historically, manufacturers invested in capital equipment to realize economies of scale that drove prices down by making products less expensive to manufacture. Modern technology changes before economies of scale can be realized, however, and a product that relies on capital expenditure for its competitive edge can become obsolete before turning a profit. In sales jargon, it will have missed its market window.

Since design tools do not rely on economy of scale, they are particularly important for products with steep technology curves. These high technology products need an accelerated design cycle that gives them a wider market window. CAD tools are as basic as typewriters for semiconductor houses, electronic circuit manufacturers, and many original equipment manufacturers. Of course, as with a typewriter, an off the shelf CAD system gives a design equal potential to succeed but does not guarantee a competitive edge. To get the jump on its rivals, a manufacturer needs design tools that are better than those of its competitors. In today's international market, worldwide competition presents almost every manufacturer with this problem.

Design tools differ even among competing designers because they are closely integrated with manufacturing and every manufacturing environment is unique. Components of a design tool kit come from many sources: CAD system vendors, software houses, universities, and anywhere that researchers have a vested interest in making new technology easier to apply. As the need for a wider market window overlaps the design cycle with manufacturing, and as designers assemble more extensive tools to give their designs a competitive edge, a basic CAD workbench needs greater flexibility to integrate tools and components from many different sources.

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Data used to predict or model the operation of individual components are supplied by the simulator from its component library. Most medium and large scale integration components can be modeled by equivalent NAND gate circuits. Complex parts instead require functional models that designate the particular output produced by every possible input. In either case, the number of component models, their accuracy, and the ease of component library updates all are important simulator characteristics.

Along with design verification, which establishes the correct operation of a circuit, most digital simulation packages perform fault analysis to evaluate test data and assess reliability at the earliest possible stage. Some programs can model many different faults in parallel. Many include a fault dictionary containing known fault types and their manifestations. Along with the standard stuck-at-one and stuck-at-zero faults, all handle more complex conditions such as signal pin shorts. When simulated output fails to match expected results and a fault is identified, guided probe data can be used to direct node-by-node examination of a prototype. Comparing probe data from each node with expected data from the test probe data base can isolate and perhaps identify the fault.

Analog circuits are much more difficult to simulate than digital circuits because their inputs and outputs are complex values that vary continuously. Although analog circuits tend to have fewer inputs and outputs than digital circuits, analog signals involve many more parameters such as voltage, current, frequency, and phase. Parameters are not constrained to discrete values and often cannot be expressed precisely. Nonetheless, valuable simulation capabilities do exist for analog circuits in the 300- to 500-part range with up to about 200 nodes.

Conventional analog simulation programs that have been used since the 1960s perform dc analysis (node voltages for constant power and input), ac analysis (linear response for sinusoidal input), and transient analysis (linear response to impulse, step, and ramp input). They typically examine voltage and current at each node over time, and give only limited approximations of nonlinear operation. Sensitivity analysis calculates output changes when one input parameter is varied; it can be used to tune a circuit with respect to inputs or environmental factors. Worst-case analysis tracks output changes as component values vary, typically between their upper and lower limits. For large circuits that cannot be simulated exhaustively, Monte Carlo methods are combined with other types of analyses to vary parameters within limits according to a probability distribution.

Established benefits of simulation include a higher level of design integrity than through breadboarding, virtual elimination of wiring or connection errors, and reduced checkout time. Most designs also realize improved manufacturing yield, fewer design iterations, and greater reliability through more thorough testing. When integrated into a CAD process, simulation requires minimal extra input and supplies output data that are useful during subsequent design and manufacturing steps. Many designers believe that circuit simulation is the major area of enhancement in future CAD systems for electronic design.

Additional information

CAD/CAM for Printed Circuit Applications is an audiovisual course that offers eight 50-minute color video lessons, each with written exercises, application studies, and reading assignments. It describes fully integrated CAD/CAM systems for PCB design and fabrication in great detail; illustrates each step in the CAD process with extensive practical examples; and includes step-by-step instructions for determining CAD/CAM applicability or effectiveness, evaluating vendor systems, and performing a cost/benefit analysis. This highly recommended reference can be rented for two months at $2359, which includes 15 sets of participant study materials that students will want to keep for future reference. Contact Integrated Computer Systems, 3304 Pico Blvd, Santa Monica, CA 90405, or call 213/450-2060.

Acknowledgment

Technical background and insight into industry trends were supplied by Arthur H. Reidel, vice president of program development at Applicon, Inc, and by David H. Miller, industry marketing manager at Applicon, Inc. This article would not have been possible without their help.

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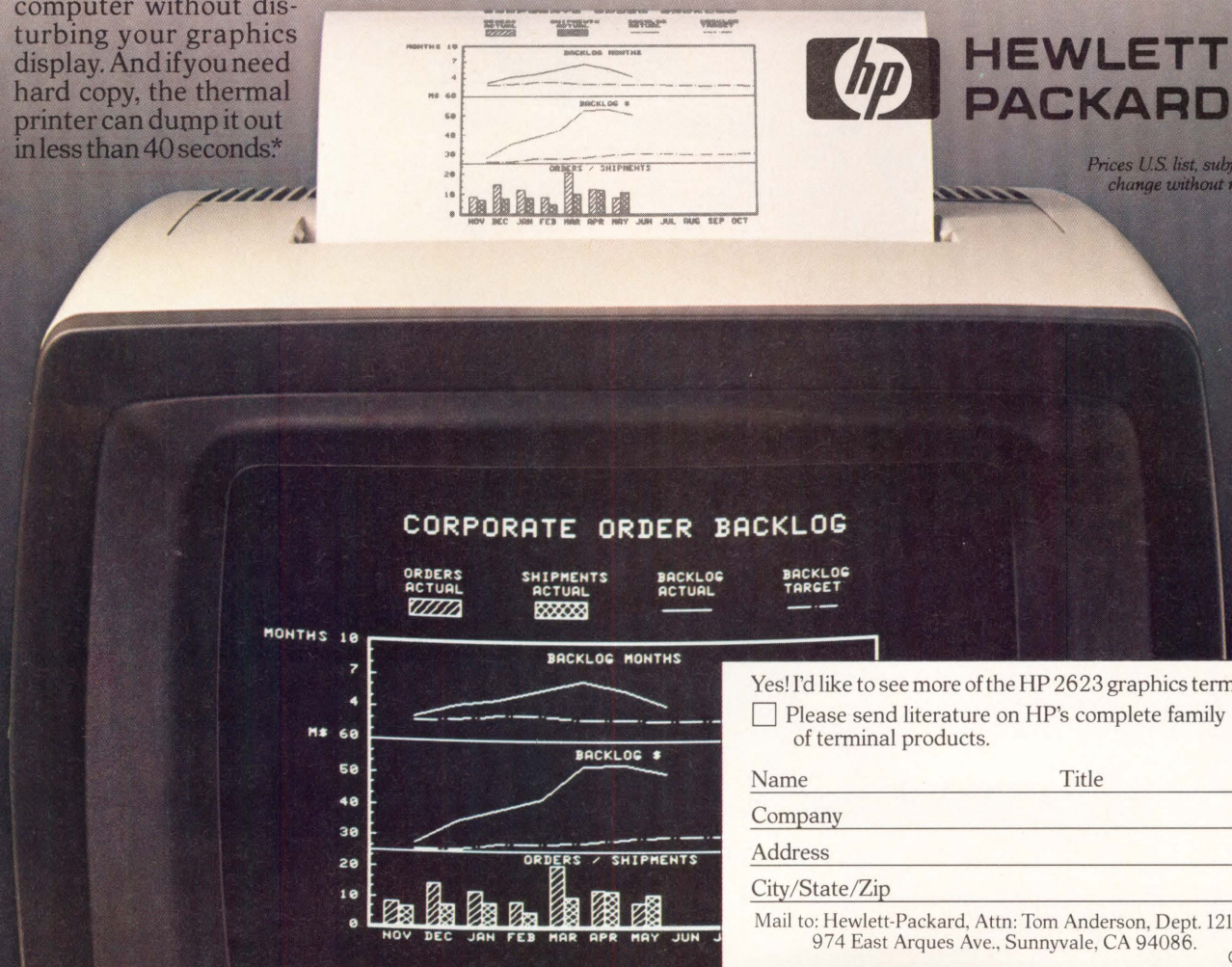
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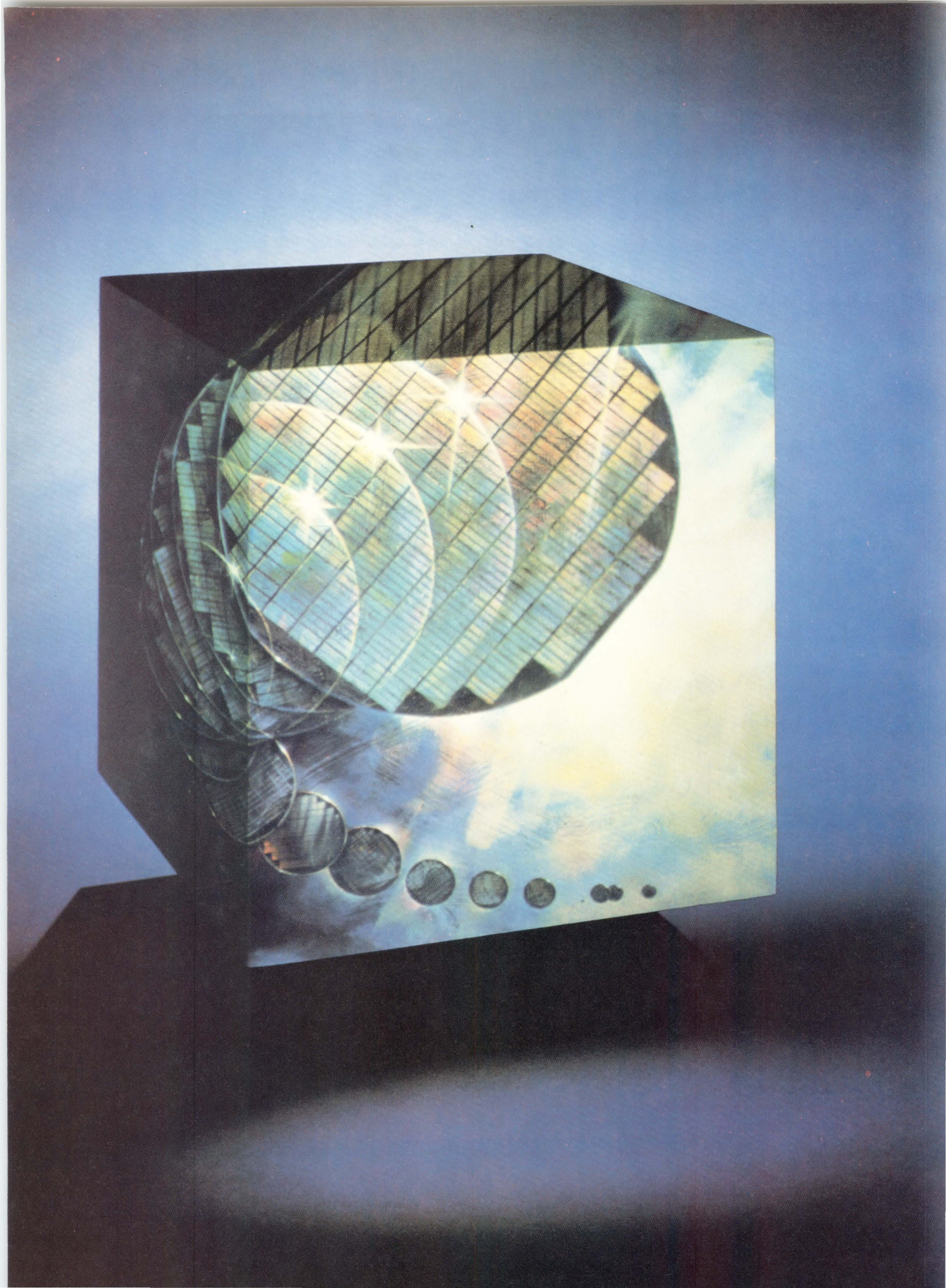
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IMS1421-50	4K x 4	40ns	50ns	600mW	NA
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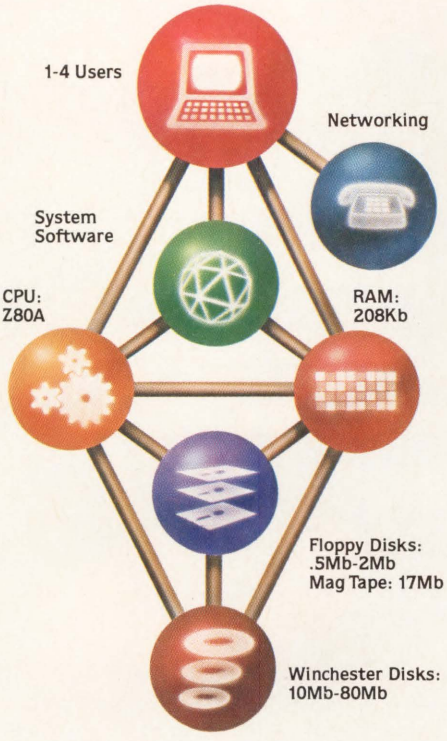
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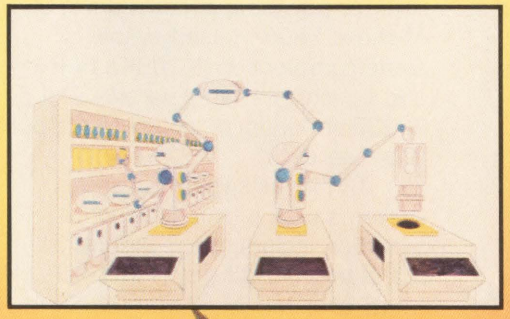
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FLEXIBLE PROCESSOR EXTENDS DESIGN OPTIONS

The concept of a microprogrammable building block permitting user access to the controlling microcode results in an adaptable CPU architecture that can be tailored and refined to fit the application

by Anthony Lake
Philip Herman, Jr
Michael Kraley

Different computer applications often need specialized machine architectures to obtain optimum performance. For example, a communications processor and a timesharing system host may have entirely different instruction sets, memory systems, and input/output configurations. However, when a common hardware base can be used for both, development, production, and maintenance costs are minimized. Microprogramming solves the problem of custom versus shared computer architecture. With microprogramming, the processor instruction set, memory, and input/output system are individually optimized for each application, resulting in lower cost and higher performance.

Although most computers today are designed around a microprogrammed processor, few make it easy to specify and change the microcode. In a user microprogrammable computer, the processor microcode resides in dynamically alterable random access memory (RAM) instead of in conventional read only memory (ROM). The microinstruction format and processor architecture are well structured and precisely defined. Also, extensive software tools support microcode design, test, and maintenance.

Advantages of a user microprogrammable design are increased flexibility, ease of development, and better application performance. Allowing changes to the microcode extends both the application base and the useful lifetime of the system. A user microprogrammable processor is a key feature of the microprogrammable building block (MBB) computer from BBN. Consequences of allowing user access to microcode include the extra cost associated with providing both software and firmware development tools, the need to initialize microprogram memory on power-up, the higher cost and lower density of RAM, and the extra complexity introduced by an added level of control. For these reasons, most conventional computers fix their microcode in limited ROM or inaccessible RAM. Some systems adopt a compromise that provides a small microcode RAM called writable control store, but this allows only small changes to the basic architecture. The system design most similar to the MBB is the Xerox Alto. Although not available commercially, it is a flexible testbed architecture—partly because of its RAM based microcode and support tools.

Minimizing the amount and complexity of input/output (I/O) hardware is, of course, an important goal in computer system design. Particularly in a data communications environment, developing and maintaining complex I/O represent a large part of total system cost.

Anthony Lake, a computer scientist with Bolt Beranek and Newman Inc, Computer Systems Div, 10 Moulton St, Cambridge, MA 02238, is presently working on the applications of VLSI to computer communications networks and multiprocessors. He was involved in research and development of the MBB and other computer applications at BBN. Mr Lake holds the BS EE & CS degree from the Massachusetts Institute of Technology.

Philip Herman, Jr, a computer scientist at BBN, was a principal architect of the MBB system, and is now involved in advanced system design and development for that and other computer systems. He received the BSEE and MS EE & CS degrees from the Massachusetts Institute of Technology.

Michael Kraley is a senior scientist at BBN and leader of the MBB development group. He is now working on VLSI design aids and advanced multiprocessor architectures. Mr Kraley holds AB and MS degrees in applied mathematics from Harvard University.

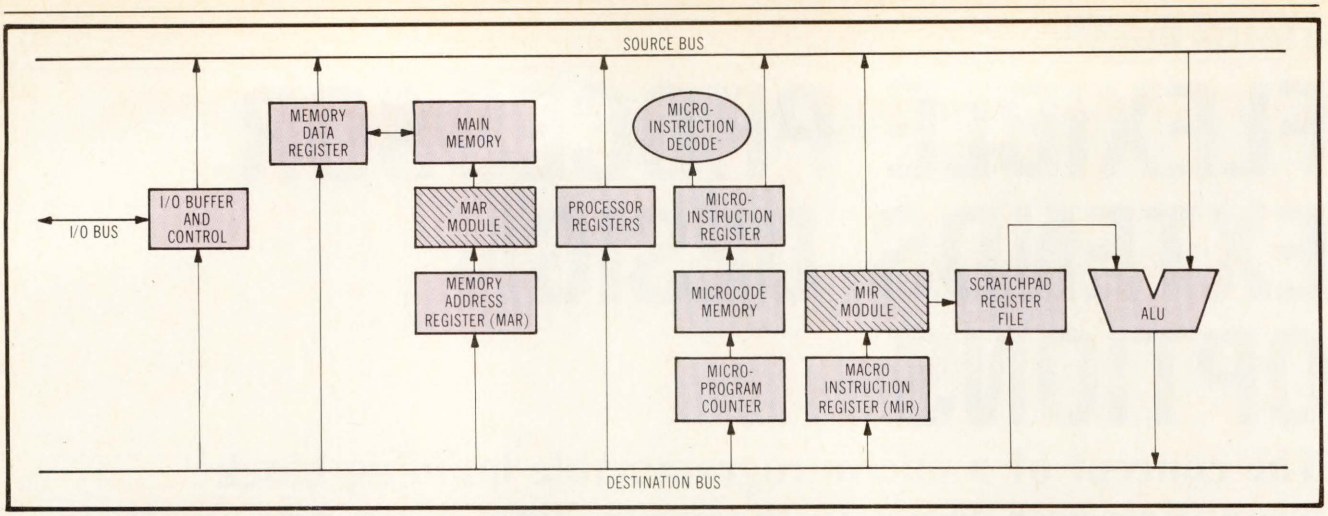


Fig 1 Processor block diagram. ALU gates source bus and register input to destination bus. Internal registers include dedicated status and control registers that interface to memory and I/O subsystems

Mainframes can afford high speed hardware to relieve the processor of I/O tasks, but a more economical approach performs complex I/O functions in the processor. Although this approach runs counter to the current philosophy of using distributed intelligence, it is cost effective on the MBB and on other recent systems, such as the IBM 4331-1. The MBB allows designers to put most complex I/O functions into microcode, while relying on available large scale integration interface circuits for low level functions to ensure high performance.

Microprogram simplicity is vital to success

The MBB processor data path loop centers on the arithmetic and logic unit (ALU), which takes as input the source bus and register file (Fig 1). The result of an ALU operation is gated onto the destination bus. Internal processor registers include the general purpose scratchpad register file and the dedicated system status and control registers, which provide the firmware interface to I/O and memory subsystems.

All microinstructions have the same 32-bit format (Fig 2). In a typical microinstruction, executed every 125 ns, a selected source gates its content onto the source bus, where it combines in the ALU with the selected word from the register file and the designated operation is performed. The result is then routed to a selected destination and perhaps to the register file, a deliberately narrow register-transfer format that is one key aspect of the MBB's microprogrammability.

Each microinstruction can execute conditionally, depending on processor status (eg, ALU result zero or negative, interrupt pending, or exceptional condition). In parallel with microinstruction execution, the next microinstruction is fetched from the address contained in the microprogram counter. Since the microprogram counter is also a destination, the full computational facilities of the machine can be used to control microprogram sequence.

A large number of scratchpad registers facilitates context switching and I/O emulation. Instead of requiring a long microinstruction to specify any of the 1024 registers, 16 "global" registers may be accessed in each microcycle, along with 16 "local" registers in one of 64 different register blocks. A base register determines the local register block that microcode process or routine is using. Different routines may use different register blocks, thus implicitly preserving register contexts.

Word size and bandwidth present significant tradeoffs

Most 16-bit computers can directly address a memory of up to 64k words. Enlarging word size to 32 bits more than doubles processor and main memory hardware costs, because of circuit pin and board space limitations. A compromise word size of 20 bits allows 1M-word virtual memory space, which is significantly larger than that of a 16-bit machine yet without a significant increase in system cost.

For areas of macromachine emulation that consume large amounts of micromachine bandwidth, application hardware support improves performance greatly. The MBB allows application specific hardware in two specific operations: macro instruction field decoding and main memory addressing. The first application module, a macro instruction register (MIR), increases performance by doing simple decoding, masking, and shifting of the instruction to be emulated. For instance, suppose that the processor registers available in machine language are mirrored by microcode in the scratchpad register file. To emulate a multiple-register architecture, the microcode must select a specific register in a macro instruction's register fields. Since masking and shifting

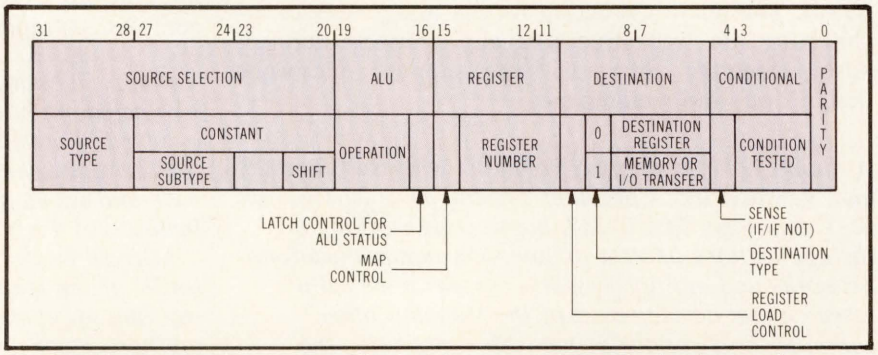


Fig 2 Microinstruction format. Vertical format used by all microinstructions mirrors CPU architecture shown in Fig 1

Common technique simplifies processor design

Microprogramming replaces random processor logic with memory elements containing instructions that specify the sequence of actions the processor hardware performs during execution of a macro instruction. Several fast microinstructions implement, or emulate, the execution of the macro, or machine level, instruction. For example, a macro instruction that adds the contents of a processor register to a location in main memory might be implemented by a sequence of microinstructions to fetch the memory data word, add it to the register, store the result back in memory, and prefetch the next macro instruction from main memory.

A wide (or horizontal) microinstruction of greater than 48 bits allows many operations to occur in parallel on each microcycle. It can therefore achieve high performance, but is difficult to develop and maintain. A narrow (or vertical) microinstruction of 16 to 48 bits could encode mutually exclusive control operations into a microinstruction field; it requires more complex decoding of the instruction to generate load and enable pulses, but is easier to develop.

Microprogrammed logic offers several advantages over random logic. Structured, low cost, and dense memory arrays replace costly random logic. Adding memory improves microprogramming performance and flexibility. System specification can be delayed until late in the design cycle, and modified easily in the field by changing microcode memory contents. Custom, or special purpose, adaptations are easily made. Diagnostics are easily embedded in the processor. Finally, a single general purpose machine can emulate many different processors or other hardware controllers, reducing documentation and training costs.

Microprogramming is not appropriate in elementary devices and in complex processors that must have a cycle time much less than 50 ns. Until recently, memory costs were a deterent to microprogrammed designs, but the availability of large capacity, high speed, low cost, and low power memories has motivated interest in the theoretical and practical aspects of microprogramming.

would consume many microcycles, a special path from the MIR to the register selector is worth the cost. Because register fields occupy different locations in different instruction formats, an application-dependent module chooses the proper MIR bits for register selection.

The MIR board also helps with macro instruction decoding. It hashes selected fields of the macro instruction to address the entry in a 1k- x 12-bit dispatch table that holds the microcode address of the appropriate emulation routine. Thus, a single microinstruction can perform an arbitrary multipath dispatch based on fields in the macro instruction. Several types of dispatch can be specified; for example, one determines addressing mode and one identifies the operation code. Dispatch memory can also be used for fast lookup of macro instruction parameters.

The second application module occupies the logical path between the memory address register (MAR) and the main memory system. An application MAR decoder can thus implement appropriate functions for address translation, memory protection, and memory management. These functions are important in large programming systems, such as a timesharing system, but may not be needed in a dedicated communications processor. The small amount of decoding hardware in both the MIR and MAR application modules greatly assists the microcode in specific macromachine emulation and increases usable performance. In addition, both boards can verify or diagnose certain functions noninvasively when testing the processor.

Memory hierarchy reflects layers of control

At the micromachine level, the 1k- x 20-bit register file and up to 16k x 32 bits of fast microcode memory provide both temporary data and state storage, and microprogram storage, respectively. Macro instructions and data occupy up to 1M words of comparatively slow and inexpensive main memory. Disc storage and communication network interfaces perform higher level distributed computation and storage tasks. For efficient emulation, the MBB hierarchy also includes macro instruction dispatch memory and provision for address mapping hardware.

Microcode memory is partitioned into a small programmable read only memory (P/ROM) and a larger microcode RAM. It is 32 bits wide, including 1 parity bit, and has a 55-ns access time. The 1k- x 12-bit dispatch memory has a 30-ns access time and permits emulation code dispatch to any address within a 4k block of microcode memory.

The 64k- or 16k-byte dynamic RAM chips used for main memory must be refreshed every 2 ms. Dynamic memory provides significantly higher density, lower cost, and lower power consumption than static memory. Runtime system firmware, rather than expensive specialized hardware, refreshes memory. Driven by a 100-μs system clock routine, refresh consumes approximately 3% of the machine's processing power. The other major issue in memory design is use of error detection and correction techniques. Six extra bits are included with each 20-bit memory data word to detect double-bit and correct single-bit errors.

Microcode occupies both nonvolatile P/ROM and volatile RAM. Nonvolatile code acts as a system bootstrap and the kernel of a multitask operating system. The loader routine initializes all writable memories: RAM microcode storage, main memory, dispatch memory, and the ALU scratchpad registers.

Hardware performs only basic tasks

I/O hardware in the MBB performs only such tasks as data clocking, voltage level or serial-parallel conversion, and the request of a microinterrupt after transferring a unit of data. Microcode maintains the finite state machine for the device, transfers data to or from

Communications processor saves time and space

The interface message processor is a packet-switch processor for advanced computer network applications. Hardware for it first became operational in 1969, and the 16-bit minicomputer it was based on is now obsolete. Over the last decade, Advanced Research Projects Agency (ARPA) network communications software has been the subject of extensive research, development, and testing. One important application of the MBB was to replace the original network hardware in a way that would preserve this investment in communications software. In addition, a variety of other communications processors based on the original minicomputer have been developed. These include a terminal interface processor for interfacing terminals to packet networks and a satellite image message processor for use in general purpose packet satellite networks.

The C/30 communications processor is an MBB configured to emulate the single-accumulator minicomputer used as the original ARPA network computer. As the C/30 was intended to both replace and coexist with the original node computers, careful attention was paid to the physical and functional compatibility of the C/30, as well as to cost/performance improvements. Physical compatibility is achieved by the lower power, space, and weight requirements of the C/30. Both systems support 63 terminals, 4 network lines to other processors, and multiple host computer interfaces.

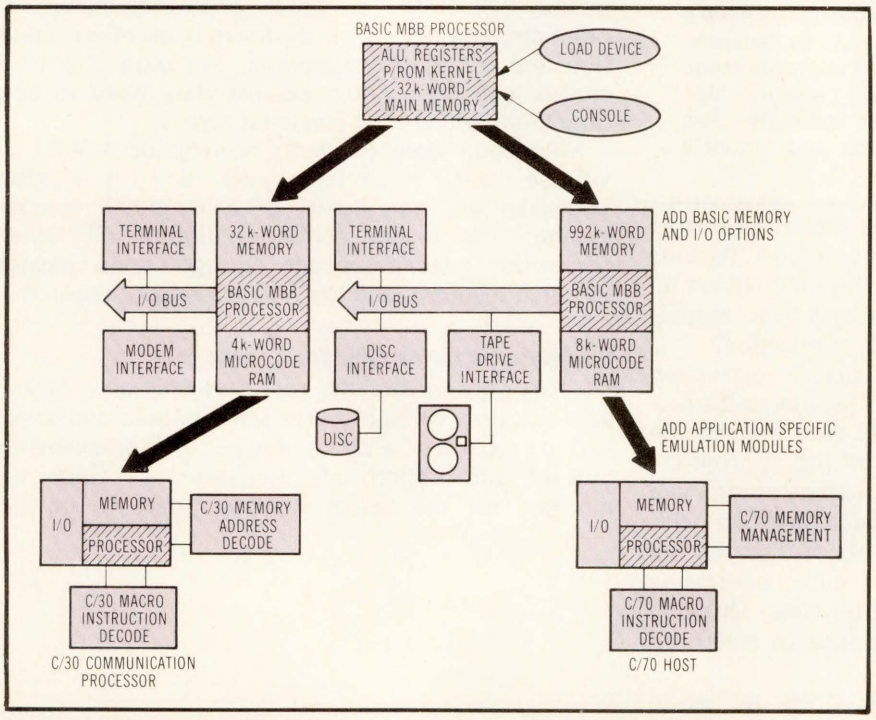
Loading and running unmodified binary versions of the existing interface message processor and terminal interface processor macro programs on a C/30 have demonstrated that the goal of directly emulating the original processor has been achieved. The microprogrammable architecture of the MBB also allows improvements in the instruction set, memory, and I/O architecture of the communications processor, via simple changes in RAM based microcode. Overall performance of the C/30 is somewhat better than that of the original interface message processor, at one-third to one-quarter of the price, one-tenth the power consumption, and one-fifth the physical size.

C machine executes high level language

Rather than implementing a system based on an existing minicomputer assembly language, a new system was developed for efficient execution of high level languages. The C/70 is an MBB provided with firmware to execute any intermediate instruction set close to the C high level language. A typical hardware configuration, with 1M bytes of memory and memory management support, is shown in the Figure, where it is contrasted with a C/30 communication processor configuration to illustrate the high degree of common modularity between these very different systems.

C/70 architecture is well suited to the support of C and other high level languages. Of particular interest is the subroutine and function calling mechanism. Since the C/70 has 1024 hardware registers available to the microcode, register saving is done simply by designating a new set of registers for the macro program to use. Should the macro program require more registers, they are cached in main memory. This is important because of the high density of subroutine calls and returns found in C and other high level language programs. The C/70 is equally well suited to other high level languages; FORTRAN 77 is available, while BASIC, Pascal, Ada, and other languages are being considered for implementation.

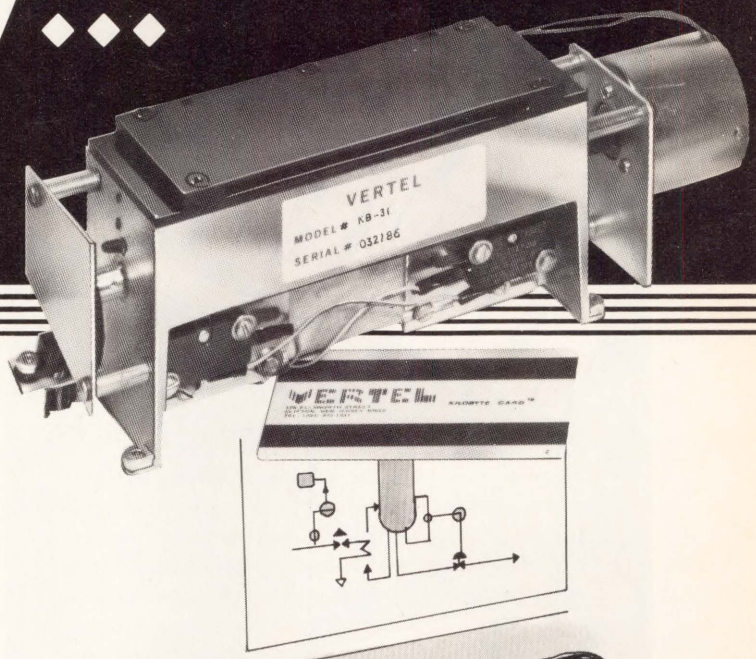
The technique of creating an intermediate language tailored both to a high level language and to the microarchitecture that implements it results in a high performance machine at a reasonable cost. Programmers can take advantage of the programming ease of the high level language with less inefficiency. Also, microprogrammability of the underlying processor allows moving critical portions of the operating system to microcode. Consequently, C/70 performance compares to that of machines selling for two to three times the cost.



MBB processor serves different applications by supporting different architectures

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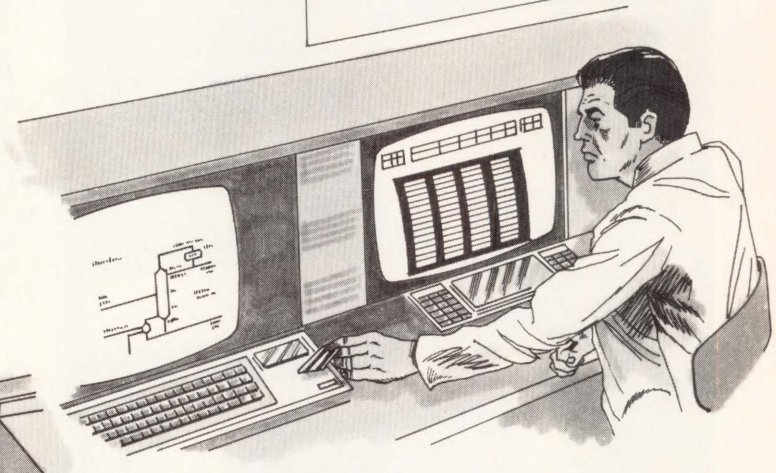
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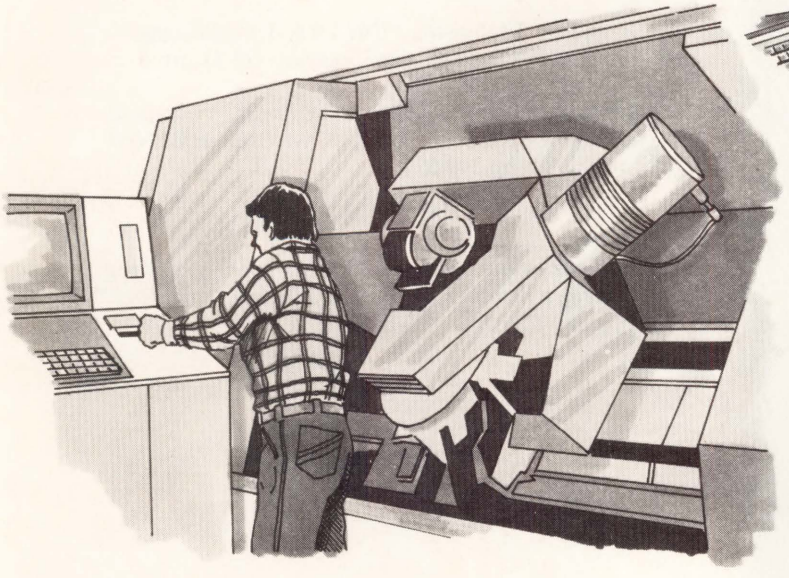


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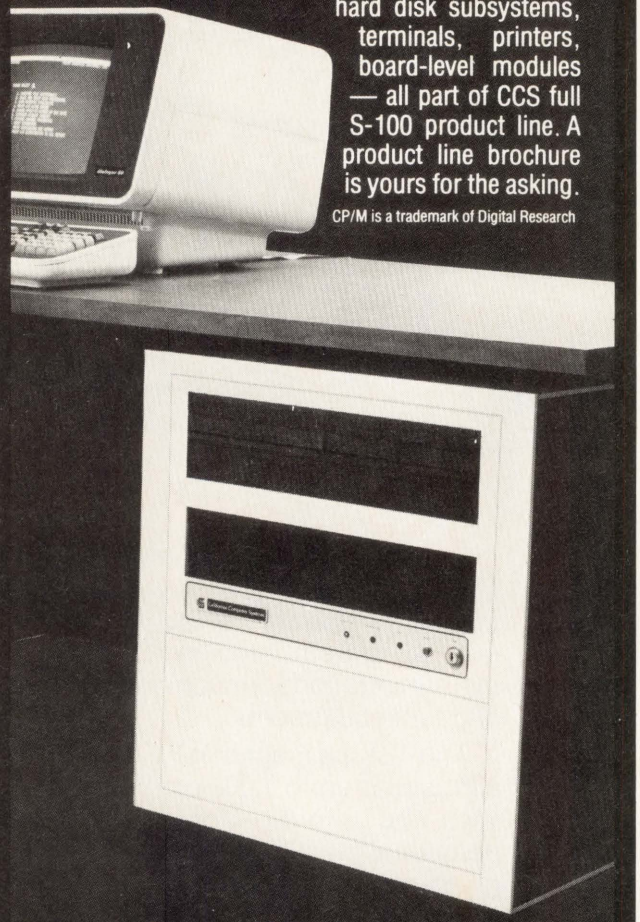
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memory, reports status, and performs word assembly or disassembly, padding, and checksumming. The large register file gives each I/O device its own block of registers. This style of microcoded I/O, where the fast central processor can be amortized over multiple tasks, is considerably cheaper, easier to develop, and easier to support than the corresponding hardware.

I/O emulation is not always a trivial demand; as much as half the processor bandwidth may be nominally budgeted to support the I/O system, leaving the other half for instruction emulation. This bandwidth tradeoff is allocated dynamically, based on the instantaneous I/O processing requirements of the machine. Dynamic bandwidth allocation conflicts with the trend toward distributed control and intelligent peripheral controllers, but it provides a simple, flexible, and cost-effective approach to applications that must support many different peripheral devices.

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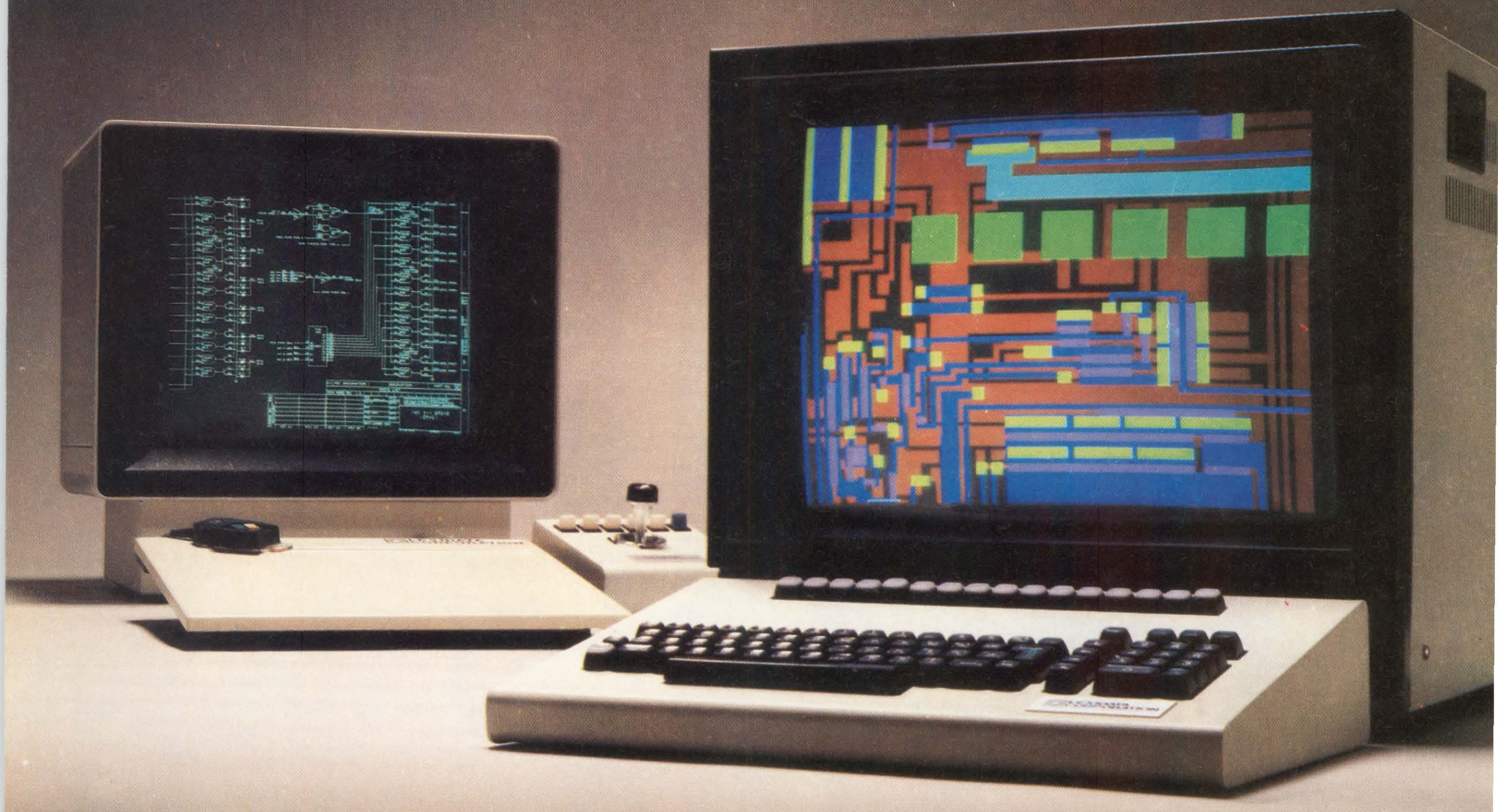
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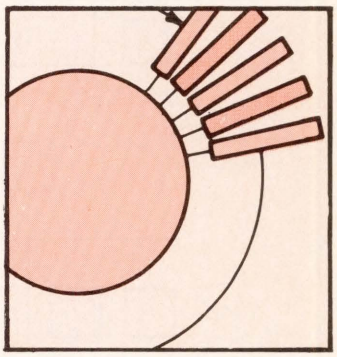
The combination of a powerful 16-bit microprocessor with a high speed ECL bus yields a versatile, reliable, and economical multiprocessor system

by Mario P. Zoccoli and
Arthur C. Sanderson

Multiprocessor architectures have been studied extensively and found to have potential advantages in reliability, speed, and throughput for specific applications.[1-6] In practice, however, the high cost of unique hardware and software design often offsets the potential benefits. The proposed multi-microprocessor bus system combines ease of expansion, software reconfigurability, and reasonable cost. The basic design principle is a high speed emitter coupled logic bus shared by all processors, memories, and peripherals, such that each device has access to the bus during every processor clock cycle. Increasing system versatility and improving cost effectiveness in the implementation of multi-microprocessor system design are the goals of this bus design.

Multiprocessor bus architectures

Key factors in the design of multiprocessor systems are their processor interconnection scheme and their capacity to share resources (including memory). Various bus architectures have been developed to achieve these goals. The three principal processor interconnection schemes are multiport memory, crossbar switching, and common bus. A multiport memory system of processor communication [Fig 1(a)] has been successfully implemented in the Univac 1100/80, the IBM 30/65, and IBM 370/168MP, the University of California at Berkeley PRIME, and the General Instruments/Mattel Intellivision. The principle of this interconnection is simple. Processors deposit information in a memory location which is accessible to another processor, which then reads the information from the memory. To avoid memory bottlenecking (attempts by different processors to simultaneously access the same memory location) memory modules are typically accessible to only a select group of processors. Communication among processors that do not share a common memory is cumbersome and requires routing through a third processor.



Among the other problems that arise in multiport memory systems are the high cost of memory control, the large amount of memory space wasted, slow communications limited by the memory port design, and inadequate resource sharing due to the tradeoff between interconnection costs and ease of information transfer. Multiport memory works best for small systems, for example, those with fewer than five processors.

Crossbar switching of system elements has been used in the Burroughs D-825 and B-7700 and the Carnegie-Mellon University C.mmp system. The basic principle

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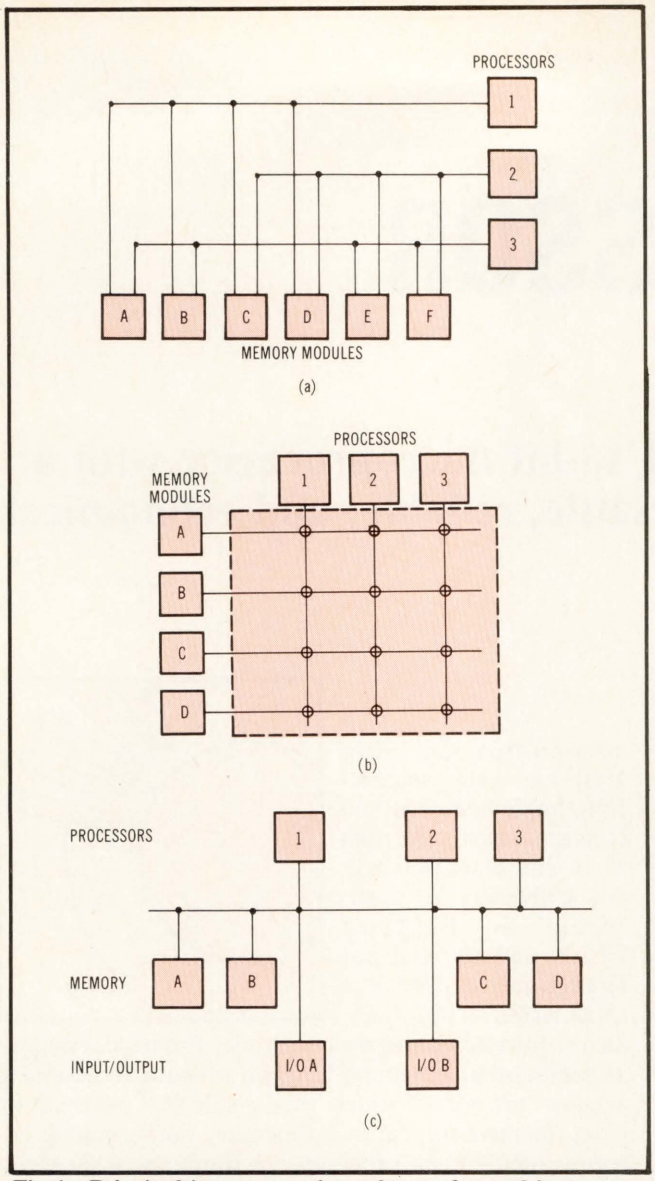


Fig 1 Principal interconnection schemes for multiprocessor systems. In multipoint memory system (a), processors place information in memory location accessible to another processor. All functional units are joined by single crosspoint in crossbar switch system (b), and system components transmit information along same communication path in common bus system (c)

of this interconnection is shown in Fig 1(b). All functional units are connected by a single crosspoint, allowing for multiple simultaneous connections as long as these connections are mutually exclusive. Crossbar switching is very fast and provides high memory utilization capability, but it requires complex hardware which grows at the rate of n^2 for n devices. Although this method achieves high communication rates, the system size is usually fixed since the switching system is difficult to expand. For large system use, crossbar switching is costly because of the extensive switching hardware required and associated power consumption.

The common bus multiprocessor interconnection scheme has been implemented on the Microdata Micro 1600D, the Control Data Cyber-76, and the Tandem 16 NonStop. This type of interconnection involves relatively simple hardware, allows convenient system expansion, and is inexpensive. Fig 1(c) shows the basic principle of this scheme in which all functional units pass information along the same communication path. The simplicity of this interconnection also has a disadvantage in that the common bus becomes a potential system-wide failure point. This scheme works best when only a few processors are involved, since the bus bandwidth does not increase as more processors are added. For example, processors may require a bus access on the average of once every seven clock cycles; therefore, as the number of processors on the bus exceeds seven, the overall system performance will level off or even decrease as more processors are added.[7] This occurs because the bus is simply unable to keep up with the increase in communication requests which accompany the addition of processors. In effect, the common bus becomes a throughput bottleneck. An even more critical problem occurs during block transfer of information on the bus, since this may force processors to idle indefinitely.

Multiport memory is inherently wasteful of memory and results in inadequate resource sharing. Crossbar switching is fast and provides the greatest memory utilization capability, but is difficult and costly to expand. A timeshared common bus is easy to expand but is currently limited by low bus communication bandwidth. The Rotary Access, Parallel Implementing, Digital (RAPID) Bus system described here combines the ease of system expansion found in the timeshared common bus with the speed and large system power of crosspoint switching.

RAPID Bus design

The RAPID Bus system design combines the power and low cost of microprocessors with the high speed data communication capabilities of emitter coupled logic (ECL). The most important innovation of the system is the processor interconnection scheme, which uses a high speed ECL common bus shared by all processors, memories, and peripherals.

Using the high speed F100K-ECL (Fairchild) allows each processor to have a dedicated time slot to access the bus during *every* processor clock cycle. Since the processor has access during every clock cycle, no time is ever wasted waiting for the bus to be free. As far as each processor is concerned, the bus is always free. The basic hardware configuration of the RAPID Bus system is shown in Fig 2. All clocking of the ECL high speed timeshared bus is transparent to the microprocessor. This is possible because of the speed difference between the microprocessor and the F100K-ECL. The processor clock cycle lasts 250 ns, and the ECL is capable of latching data from the system bus in less than 10 ns. Using this ECL communication design, the RAPID Bus operating system is capable of a variety of microprocessor organizations.

The RAPID Bus system allows processors to run synchronously and share bus communication without interference. The synchronous nature of the system is directly tied to its reconfigurability, since pipeline, hexagonal array,[7] hierarchical, and independent architectures can be achieved by reconfiguring the communication flow pattern in software. In the standard, independent operation mode, each processor (up to 25)

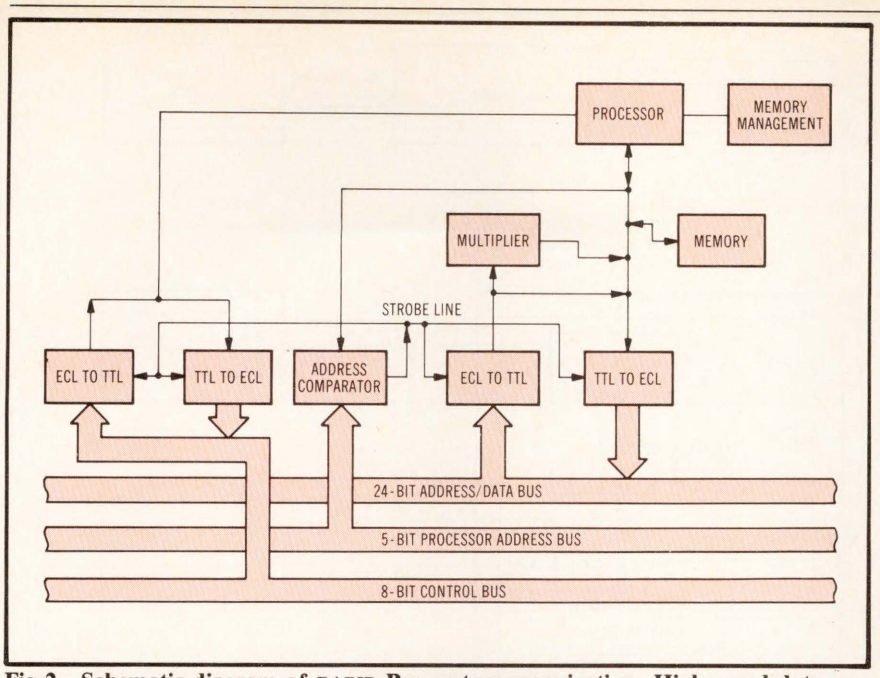


Fig 2 Schematic diagram of RAPID Bus system organization. High speed data transfer among system elements is provided by use of ECL latching and bus driving system. Each processor is given dedicated system bus communications window during every processor clock cycle. This is possible because of speed difference between F100K-ECL and processor

is assigned to an address from 1 to 25; the master bus clock counts, and each processor is allowed a turn on the bus lines when its number is reached. The entire count takes 250 ns, or 10 ns per processor for a 25-processor system. With this system, each processor can access any semiconductor memory module via the same common bus without a wait cycle. If a pipeline reconfiguration is appropriate to the processing task, a setup program which manipulates the address in the processor comparator block may be called. This is accomplished by alternately loading the processor identification system—first, to acquire an instruction while other processors are executing the same instruction, next, to acquire data or constants, and finally, to allow operationally adjacent processors simultaneous bus access to permit information transfer from processor to processor along the pipeline. All of this can be done without wait states because of the high speed of the system bus.

In addition to speed advantages over standard bipolar logic, ECL has unique transmission characteristics which make it suitable for high speed, high reliability, high integrity data communication applications. Typically, ECL outputs are able to drive 50-Ω loads and the F100123 Hex Bus Driver will drive a 25-Ω load. These low impedance, high current lines are highly noise immune, and the noise immunity is extremely important for high density communication applications. The low output impedance and high input impedance of the ECL allow fanouts of 200 gates. This is superior to bipolar transmission lines now available and is well suited to the present application.

A transmission difficulty arises in any system where output impedances differ greatly from input impedances. The difficulty could be overcome by passive termination of the transmission lines. This approach, however, would require that one know the total load of all the inputs, and this in turn would limit the ability to alter the number of system components on the bus. The use of an active terminating circuit solves the problem. Each terminator is a bilateral clamp acting as a low impedance source which sinks current at the voltage out high level (V_{OH}) and sources current at the voltage out low level (V_{OL}). In the transition region between V_{OH} and V_{OL} the terminator has a high impedance and thus has minimal effect on signal rise times. This clamping action limits overshoot and ringing in situations where load impedance is not fixed. The entire F100K series is voltage compensated, making its noise margin insensitive to power supply variations and transients.

An important consideration is the transmission speed along the bus lines. With a typical capacitance load, transmission time loss will be approximately 1.4 ns/ft. To minimize this kind of loss, all circuit boards are arranged in a wagon wheel pattern with ECL drivers and latches at the edges as shown in Fig 3. This arrangement provides the highest possible board density with the shortest average communication distance between boards. Communication lines, instead of crossing the hub of the wagon wheel, travel around the inside from one edge connector to the next. To ensure proper clocking, a processor reference clock is distributed from a central clock physically located just below the center of the hub. A method of onboard clock synchronization using phase locked loops is discussed under "Timing and synchronization."

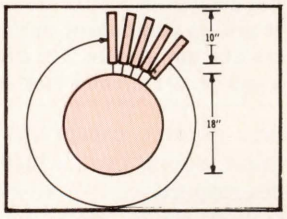


Fig 3 Physical layout of RAPID Bus system. To minimize bus communications delays, processor, memory, and I/O boards are arranged in wagon wheel pattern, providing least distance between system components. To further limit time delays, all ECL components are located as close as possible to edge connector of each board

RAPID Bus operation

Fig 4 shows the RAPID Bus design and communication flow in more detail. Although the system concepts are not limited to the choice of hardware, it illustrates the operation of a specific design example. The Z-8001 microprocessor is used as the basic processing unit. The Z-8000 series provides a family of very large scale integration (VLSI) components for memory management, input/output (I/O) manipulations, and resource sharing. In particular, the Z-8010 memory management unit provides flexibility in code segment relocation and memory protection. The Z-8001 operates at 4 MHz with three or more clock cycles per basic machine cycle. Although the majority of operations require fewer than 20 clock

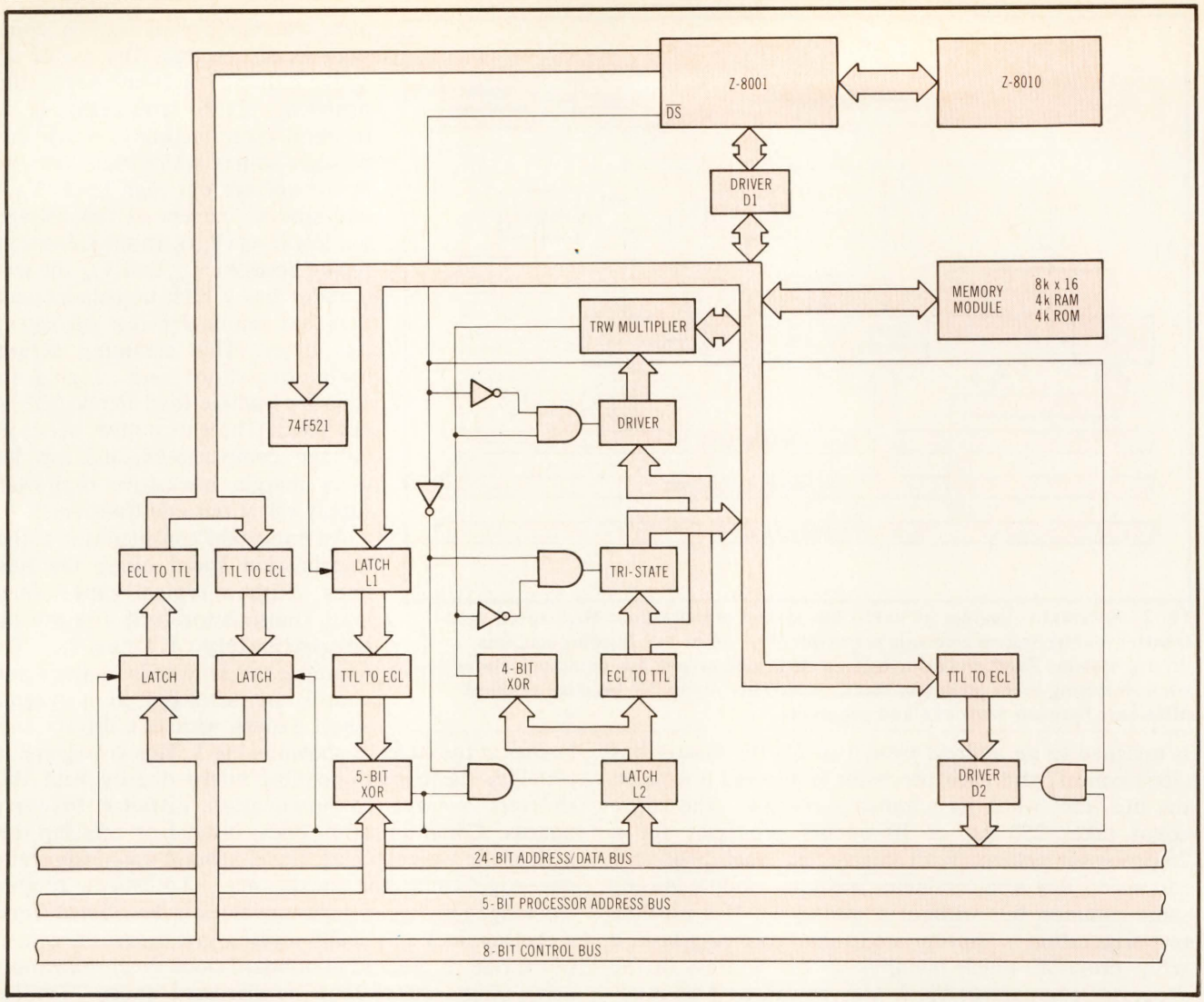


Fig 4 RAPID Bus hardware design. System of transparent latches enables processor board to communicate with any other system component during every processor clock cycle. TTL to ECL and ECL to TTL conversions are carried out using 10124 and 10125 Fairchild F10K series ECL. Information transfer onto and from system bus is strobed by having F100K-ECL latches and drivers recognize processor's time slot from 5-bit processor address bus and then packet switch this information between system components

cycles, notable exceptions are the multiplication and division operations, which require 75 and 100 clock cycles respectively for 16-bit computations and 287 and 728 clock cycles for 32-bit calculations. Because these computation times would represent a substantial drawback for many applications, each Z-8001 has a resident TRW MPY-16HJ multiplier. The function of the TRW chip is made transparent through a series of Fairchild 74FXX fast advanced Schottky transistor-transistor logic (TTL) gates. The TRW performs 16 x 16 multiplication in 150 ns, and with processor loading, the entire operation is completed in 11 to 24 processor clock cycles.

The panel describes a typical offboard fetch by the processor, illustrating the RAPID Bus communication scheme. The basic approach includes a system of data acknowledgment on the control bus to ensure that data are acquired by the intended receiver before the sender discontinues its output. The entire bus system includes parity checking to guarantee the integrity of bus communications, and the system of comparators and latches makes the high speed rotary nature of the bus transparent to the microprocessors and memories. To handle peripheral interface to the high speed bus, a peripheral interface adapter board is used. (See Fig 5.) The latching for this board resembles that of the memory module with the added multiplexing to handle four transfers on the same edge connector. After latching, the information is handled by a Z-8038FIO general purpose microprocessor interface that provides elastic buffering between the central processing unit (CPU) and the asynchronous peripheral. The device also provides a 128-word-deep buffer which cuts interrupt servicing overhead. In addition, it is capable of simultaneous independent read and write operations, which means that the CPU can write a byte of data into the FIO without disturbing a simultaneous read operation involved in peripheral service.[8]

Performance evaluation

A better understanding of the efficiency of the RAPID Bus system is possible through a comparison with its nearest relative, the conventional common bus. In the common bus, an arbitration method is necessary to inhibit simultaneous bus access by multiple processors and to assign priority to processor access. RAPID Bus

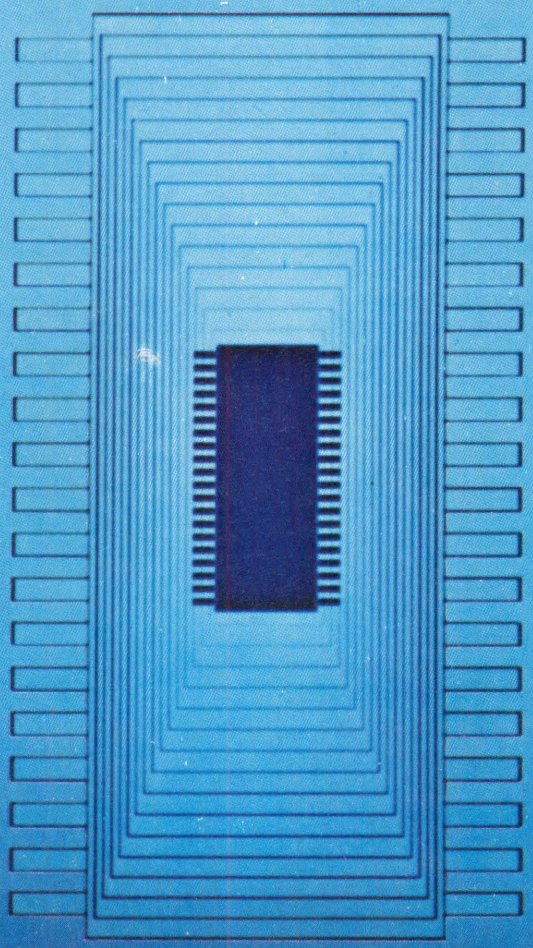
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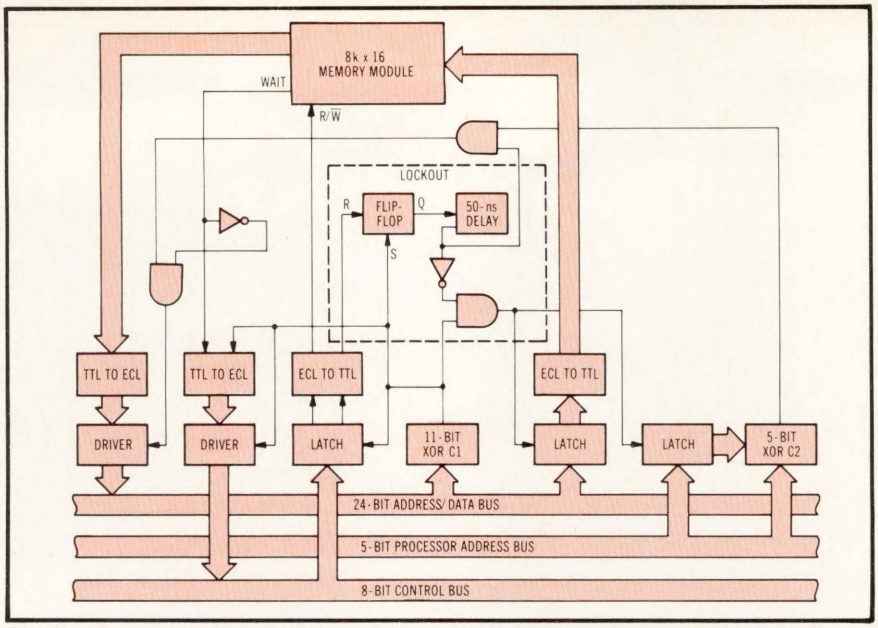


Fig 5 Memory module communication system. Like processor units, system's remote high speed memory boards also have ECL bus interface, which includes high speed ECL comparator that recognizes system requests within its address space. When such requests occur, memory board must latch contents of 5-bit processor address bus. This allows board to remember which processor made access request, which in turn allows system components to communicate with one another by simple simultaneous bus accesses every time processor's home address comes up

does not require arbitration and priority setting because processors, instead of requesting bus access, are given a dedicated slot on the bus during all processor clock cycles.

In the conventional common bus, expansion capabilities are severely limited by bus contention. With RAPID Bus an appropriately linear increase in throughput up to 25 processors is achieved. Fig 6 shows a comparison of the two bus types for throughput versus the number of processors. This performance

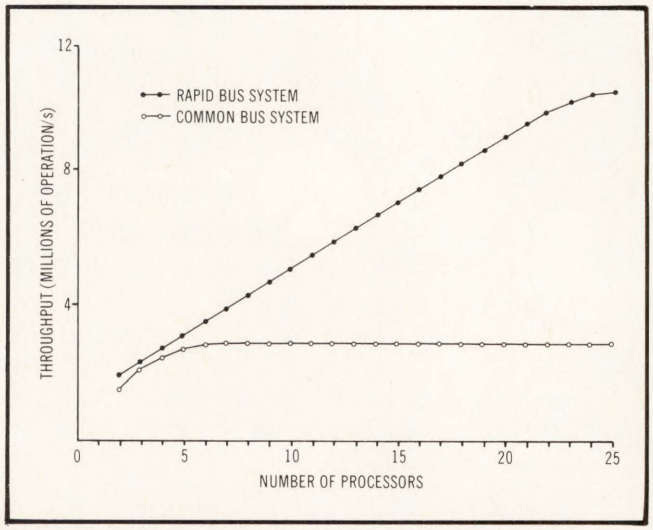


Fig 6 Comparison of RAPID Bus and common bus system throughput. RAPID Bus system exceeds throughput of standard common bus system by utilizing synchronized access to high speed time shared system bus

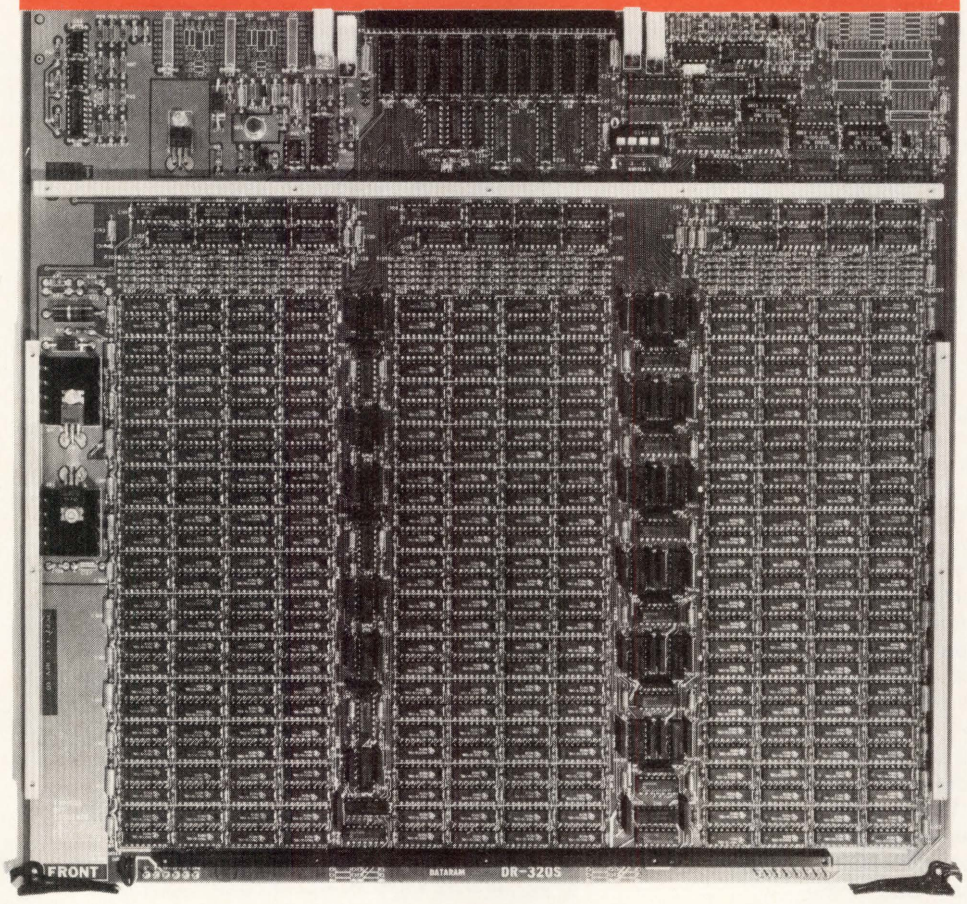
evaluation is based on a simulation using the system timing model shown in Fig 7. The system has p processors, r I/O devices, and a total of M kilobytes of primary memory divided into M modules. Whenever a job comes into the system, if there are already D jobs in the system, or if the available memory is not big enough, the job will be queued in the outside wait queue. If there is adequate memory and an available processor, the new job will enter the service box and queue in the processor queue for the first service. When the job gets a processor, it will be served for a certain amount of time nonpreemptively until it requests an I/O operation; then it will proceed to the I/O queue and wait for an I/O operation. Following the I/O, the job will depart the shole system with a probability $1 - \sigma$, or return to the processor queue with a probability σ, and the cycle will be repeated.

This type of analysis assumes that job arrival is a Poisson process.[9] Movement through the processor is based on the exact timing of the Z-8001 microprocessor, and timing measurements include memory fetch transactions. Transition from waiting queue to processor queue and from processor queue to I/O queue is also determined by communications bandwidth. This is the primary difference between the two systems. Fig 6 shows that in a comparison of the RAPID Bus and conventional common bus system, the bandwidth of the former is higher than the demand up to 25 processors. It may be observed in Fig 6 that the RAPID Bus system facilitates graceful increases in throughput by the simple addition of processor boards, a feature of the system that allows modular expansion as system requirements increase. The modular expansion capability is compatible with a "building block approach,"[10] which has been found to reduce design time and cost for customized systems with varying degrees of complexity. This modular, building block approach also helps to simplify the complex operating system software usually required for multiprocessor systems.

Reliability

The RAPID Bus system is tolerant of processor failure, but as with the conventional common bus, it is very sensitive to bus failure. When a single processor is lost, it may result in a decrement in system operation, or a simple reduction in throughput, but a catastrophic failure is unlikely. The use of microprocessors and the low cost of each subsequent processor module make it feasible to have an extra board ready to replace a failed processor automatically. To reduce the effects of bus failure, a dual redundant bus has been used to minimize the possibility of system failure due to bus failure. In addition to the bus, most single-point hardware has been made fail-soft by redundancy.

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Typical offboard fetch by processor

1. The processor places the program counter (PC) on its Address/Data lines.
2. This information passes through the D1 bidirectional bus driver to the onboard system bus.
3. If the address is found to be greater than 1FFF, the reference is offboard.
4. Offboard references are routed to the TTL to ECL translator and then to the D2 bus driver. This bus driver has an output low level more negative than normal ECL outputs, which allows an emitter follower output transistor to turn off when the termination supply is -2.0 V, and thus presents a high impedance to the data bus. This is similar to the operation of a tri-state bus driver.
5. The bus driver is enabled when two conditions are satisfied: the processor $\overline{DS}$ line signals a processor SEND, and it is the processor's turn on the bus.
6. The processor's time on the bus is determined by comparing the 5-bit processor address loaded in latch L1 with the 5-bit word on the processor address bus. When the processors are operating independently, each processor resides at a unique address.
7. When the processor's dedicated time slot is recognized, the D2 drivers are enabled and the board sends address information on the 24-bit system address/data bus, and it sends control signals on the 8-bit system control bus. In the present example, an important control signal sent by the processor would indicate that this is a READ operation.
8. These signals travel to all system components, and the address request will be recognized, for example, by a memory module like the one shown in Fig 5. Comparator C1 of the memory module signals that the 11 most significant bits of the system address match the address space of this module. This comparator then strobes all of the memory module's latches and sets a flipflop. The output of this flipflop is delayed by 50 ns and inverted and ANDED with the original output of comparator C1. This flipflop circuit produces a hardware lockout, which prevents any other processors from entering any request addresses into the memory module until it has completed the present transaction and has received a processor RECEIVE ACKNOWLEDGE on the control bus which resets the flipflop.
9. In addition to locking in the 13 least significant bits of the address request, comparator C1 also strobes a latch which captures the 5-bit processor address bus lines. This is essential so that the memory can now "remember" which processor made the request and can in turn continue to access the bus at the appropriate times to pass status information until the transaction is completed.
10. After the initial contact, comparator C2 sends a strobe out every time the 5-bit processor address comes up. This is ANDED to the non-inverted output of the 50-ns delayed flipflop. This AND gate ensures that no confusion will occur when an attempt is made to output old data while the memory module is attempting to acquire the address information.
11. While the memory module is accessing the correct address, a WAIT is provided on the control bus every time the processor address comes up.
12. When ready, the memory module will discontinue the WAIT and send the data back to the requesting processor. The requesting processor will acquire the data on its L2 data latches.
13. The processor sends a RECEIVE ACKNOWLEDGE back to the memory module on the system control bus, and the memory module resets the lockout flipflop.

Included in the RAPID Bus system is a hardware and software failure detection system. Each processor module has local diagnostics, including invalid op-code detection. Generally, an internal "self check" approach has been taken to failure detection. Routine checksumming of critical tables and codes ensures the integrity of vital memory areas and communication paths. The self check approach has an advantage over the global operating system check approach, whose drawback is that it requires time to isolate the processor at fault when an error is detected. Thus, the self auditing system with the global operating system acting in a supervisory capacity was chosen. Parity is provided on all bus lines to validate communications on the high speed bus.

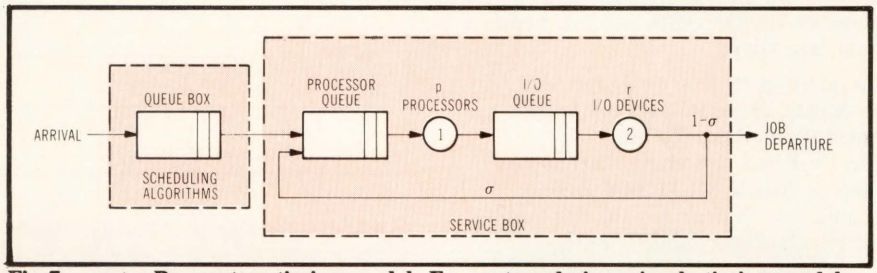


Fig 7 RAPID Bus system timing model. For system design, simple timing model with p processors, r I/O devices, and total of m kilobytes of primary memory divided into M modules is used. Whenever job comes into system, if there are already D jobs in the system, or if available memory is insufficient, job will be queued into wait queue for later running

The processing modules also include a Zilog Z-8010 for memory management. One of the many capabilities of this chip is that it detects errors such as attempts to execute data or overflowing an area set aside for a stack.[11] As exemplified by the RAPID Bus system, the design of more versatile, high speed systems requires a concomitant increase in fault detection and correction capabilities. The RAPID Bus system utilizes a combination of

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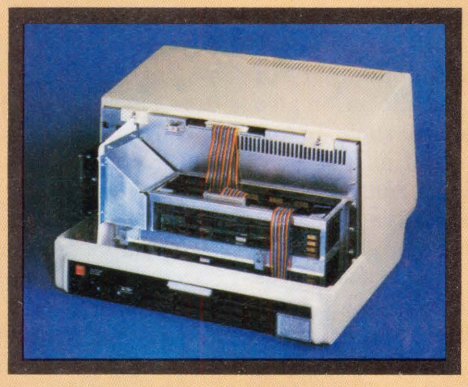
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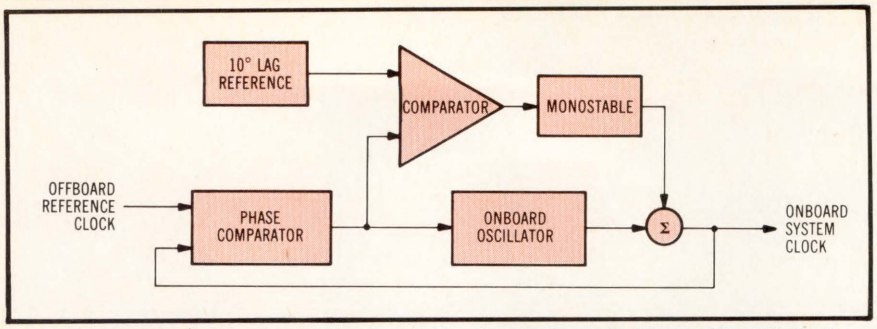


Fig 8 Block diagram of PLL synchronizing circuit. System detects "lost" clock pulses and enables all processors to remain in continuous synchrony, thus eliminating major problem of previous synchronous multiprocessor systems. System works by comparing onboard clock to offboard clock reference. When errors occur, system of comparators and monostables makes necessary corrections

hardware and software techniques designed to provide effective fault correction with minimum operating system overhead. A system simulation indicated that fault and deadlock detection and correction overhead reduces system throughput by only 1.3%.

Timing and synchronization

Multiprocessor systems may operate either synchronously or asynchronously. In a synchronous system, the processor clocks are in step such that relative timing of concurrent operations is always known. Although synchronous operation typically requires extensive hardware design, large increases in throughput may be achieved by tightly coupled concurrent pipeline or array operations. Such tightly coupled systems typically have a fixed configuration, which limits versatility. Examples include the Control Data STAR (a 2-pipeline processor), the Texas Instrument ASC (a 4-pipeline processor), the Illiac IV (a vector processor), the Cray 1 (a vector processor), and the Goodyear STARAN (an associative processor), which operate on data by their content rather than their address.

The RAPID Bus system is able to operate either as a set of independent processing units or as a tightly coupled system. In the independent mode, the system divides the total job stream into a set of substreams. These substreams are then dynamically allocated to various processors. The dynamic allocation system requires greater operating system overhead than a prearranged allocation system, but greatly increases equitability of job sharing among processors. Dynamic allocation also makes the system more failure tolerant since prearrangement would result in a total loss of all tasks assigned to a failed processor. The independent mode of operation is especially appropriate when the system is handling a general multi-user job load.

To provide the overall versatility in a synchronous system, a highly sophisticated clocking system has been developed for the RAPID Bus. A single timing pulse generated at a central location and distributed throughout the system is sufficient for the independent operating mode, but does not suffice for any of the various tight configurations where the information flow must be strictly predefined and interruption of the flow along any point would cause failure. In particular, interruptions in a high density communications environment occur frequently because of "lost" pulses and transmission noise. To avoid this type of system vulnerability, a phase locked loop (PLL) synchronizing circuit has been developed.

The basic principle of the synchronizing circuit is shown in Fig 8. Each processor has an onboard clock and a PLL synchronizing circuit. A reference clock is generated at a central location and is distributed to all processor boards. This reference is then compared with the onboard clock. If the onboard clock differs from the reference clock in phase, a voltage proportional to the difference is generated. The sign of this voltage indicates the direction of difference. This voltage is fed into the onboard clock generator circuit which updates the clock appropriately to pull it back in phase with the reference. Also included in the system is a comparator which detects differences greater than a 10° reference phase angle lead and activates a monostable pulse generator. The principle of this substream is that if an onboard clock has not been generated within 10° of the reference, then the clock pulse has been "lost," and a pulse must be generated to replace it. Further, since the centrally generated clock is only a reference if this clock is lost, the onboard clock continues on its own.

A fully functional version of the system was constructed. Tests show that the system is capable of handling a reference clock with additive noise up to a 6-dB signal to noise ratio. The system could also handle an onboard clock which is purposefully varied at random by ±8° and which is also interspersed with lost pulses on a random basis averaging one lost pulse per 24 pulses. The PLL synchronizing circuit corrected these difficulties and generated a stable output.

Conclusion

The RAPID Bus system design is aimed at the development of a parallel processing unit capable of high throughput at reasonable cost. The basic approach is to use available microprocessor processing units with associated support chips, couple them with a high speed ECL bus, and synchronize processors using a new PLL system. Currently, all of the hardware principles have been tested, and a 3-processor prototype system is under construction, using fast TTL logic to facilitate development. Principles of a software operating system designed to optimize job allocation have been outlined, with many of the important operating system routines being duplicated in the processor board's resident high speed read only memory.

The prototype RAPID Bus system will be used as an experimental system to investigate parallel implementations of realtime signal processing and interactive control tasks. Such tasks have wide applicability where the cost and development time associated with unique hardware design may not be justified, but where parallel processing and control of complex systems could provide significant benefits. Examples include medical monitoring applications where large quantities of data must be processed routinely, but where specific types of signals may vary widely. The system is also well suited

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Acknowledgments

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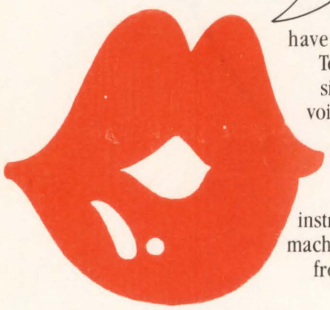
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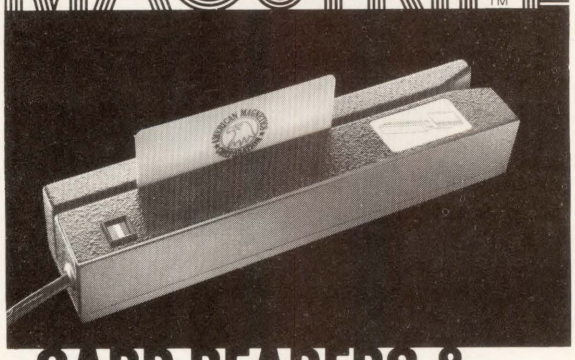
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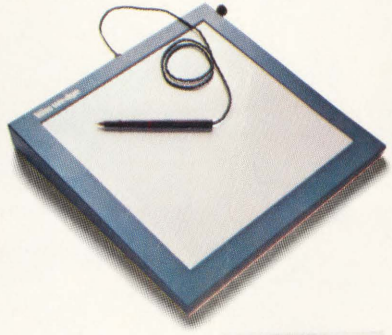
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ARRAY PROCESSOR SPEEDS DATA CONVERSION

Treating the exponent and mantissa of a floating point number as a single 16-bit number provides the speed benefits of integer handling while still achieving the wide dynamic range of floating point representation

by Ching-Ming Lai

Analog signals are sometimes digitized into a floating point format to encompass a large dynamic signal range. However, data are often processed as integers to achieve maximum computing speed. The minicomputer is capable of converting data from a floating point format to integers, but its format conversion speed is often too low for applications that demand fast realtime signal processing. A special technique for achieving fast data conversion uses an array processor that forms part of a realtime signal processing system. The format conversion speed, when the array processor is used, is on the order of 100 times that of most minicomputers.

A typical example requiring the fast data format conversion is in a data acquisition system of a computerized X-ray tomography scanner where a floating point analog to digital converter (FPADC) is used to collect wide dynamic range data at a high sampling rate. In such a system supplied by Analogic, the FPADC digitizes data into 16 bits, with the two most significant bits (MSBs) representing the exponent. Bit patterns of 00, 01, and 10 are used as "pseudo" exponents to encode the amplifier gain at 64, 8, and 1, respectively.

The gain is automatically selected, depending on the analog signal magnitude. During a high-resolution image scan, as many as 600 data arrays are collected. Each data array, containing 512 data points, is processed in a series of calculations before it is mapped onto a matrix that represents the visual image.

To complete image reconstruction in seconds, a special computer system is used. A typical system consists of a minicomputer, an array processor (such as the Analogic AP400), and other specialized hardware that processes data as 24-bit integers. Upon acquisition of projection data, the 16-bit floating point data must be rapidly converted into a 24-bit integer array before they can be processed for image reconstruction. It is desirable for the conversion time not to exceed one-tenth of the total processing time for a data array. That is, the conversion time must be in the order of 1 μs per data point. The host minicomputer itself cannot achieve this data format conversion speed.

The array processor can convert the data at very high speed by treating the converted integer value (the true value) as a transfer function of the floating point data. The floating point data are treated as a 16-bit number, where the exponent is combined with the mantissa as if it were part of the mantissa. In the Figure, the two MSBs of the 16-bit number, which represents the exponent in the floating point format, divide the function into four segments. The fourth segment, with the exponent bit pattern 11, is not shown since it is not used.

The transfer function can be calculated just like an ordinary function such as a trigonometric, logarithmic, or polynomial function. Utilizing a unique high speed technique in the array processor, a function, F(X), is approximated by linear segments. Each segment is characterized by a slope, M_k, and an intercept on the y-axis, b_k, where k designates the MSBs of X (the coarse value of X). Thus, a set of the parameters, namely, (M_1, b_1), (M_2, b_2), . . ., (M_n, b_n), defines the function in an n-segment approximation.

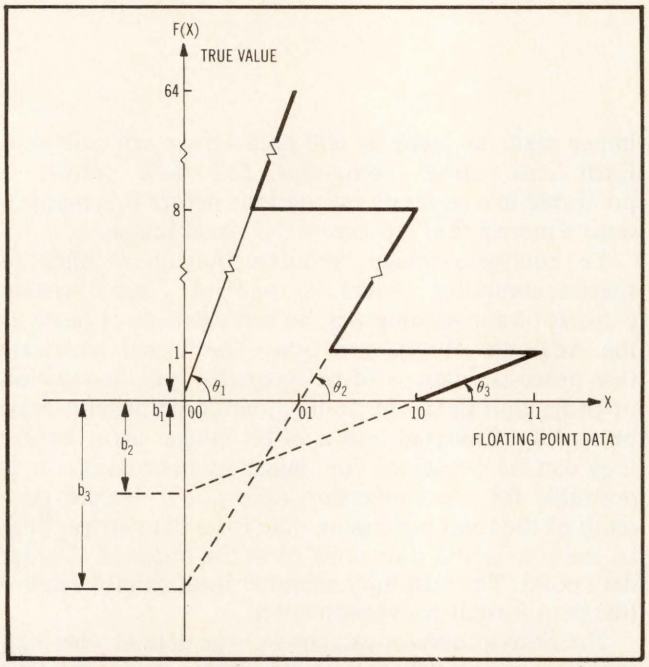
When these parameters are stored in the array processor as a lookup table, the array processor calculates

Mr Lai is a principal engineering physicist with Analogic Corp, Audubon Road, Wakefield, MA 01880, where he is involved with the development of advanced medical imaging systems and the applications of high speed computer systems. He holds a PhD degree in physics from the State University of New York at Stony Brook, where he was responsible for developing the nuclear magnetic resonance imaging system.

the function value by referring to the lookup table. As when performing a routine calculation, the array processor relies on an arithmetic pipeline unit to achieve high speed computation for the data array. Operating in the lookup table mode, the array processor loads the starting addresses of the data array X and the lookup table into address registers of the arithmetic pipeline.

When the calculation begins, the MSBs of X are fetched as an offset address, k, to obtain its corresponding M_k and b_k values in the lookup table. In the subsequent steps, as the data move further down the arithmetic pipeline, X is operated on by M_k and b_k to generate a linear interpolated result $Y_k = M_kX + b_k = F(X)$. In the meantime, the next item in the data is fed to the arithmetic pipeline for execution. The operation sequence continues until the last item in the data of the array comes out of the arithmetic pipeline. At this point, the computation of the function array F(X) is complete.

When this technique is applied to the transfer function just described, the lookup table will consist of three slope/intercept pairs (tan θ_1, b_1), (tan θ_2, b_2), and (tan θ_3, b_3). Since each segment of the transfer function, which describes the value of the 14-bit mantissa, is a linear function, the value calculated by the linear segment approximation is actually the exact result of the data format conversion.



Relation between floating point data and equivalent integer value. Floating point data, treated as single-word number with exponent in MSBs and mantissa in LSBs, are plotted against horizontal axis. Normalized integer, representing true value of floating point data, is vertical coordinate. Exponent, encoded in two bits, is pseudo exponent. Transfer function is linear within each segment, although discontinuities occur at segment boundaries. There are two vertical breaks in plot to accommodate wide dynamic range of function

When it is desirable to scale the converted integer arrays by a common factor A, the lookup table values are multiplied by this factor. In addition, correction can be made for the offset error, e_k, of each amplifier gain by applying it to the intercept parameter. The conversion equation becomes $F(X) = A[M_kX + (b_k - e_k)]$.

One pass of the data array through the arithmetic pipeline is required to complete the data format conversion for the array. In the AP400, the arithmetic pipeline has four parallel computation sections. The computation time required per data point through each section is 1.92 μs. For this data format conversion application, data are alternately directed to sections 1 and 2. Section 3 contains the corresponding slope/intercept parameter pair for the data in section 1. Likewise, section 4 has the parameter pair for section 2.

This pipeline configuration has the advantage of allowing two data points to be processed simultaneously. The data format conversion time, including the scaling factor and the offset correction, is 0.96 μs/point, which is within the 1-μs/point limit for the aforementioned imaging application. The minicomputer, which requires more processing time, uses a program to separate the MSBs and branches to a subroutine to obtain its corresponding gain factor and offset value. In a PDP-11/34 minicomputer, this step takes about 20 μs. The multiplication of the gain factor by the data takes approximately 30 μs, even when the minicomputer is equipped with an extended instruction set. Another 10 μs is needed to add the data to the offset value. The scaling factor can be implicitly included in the gain factor and the offset values without directly multiplying the data.

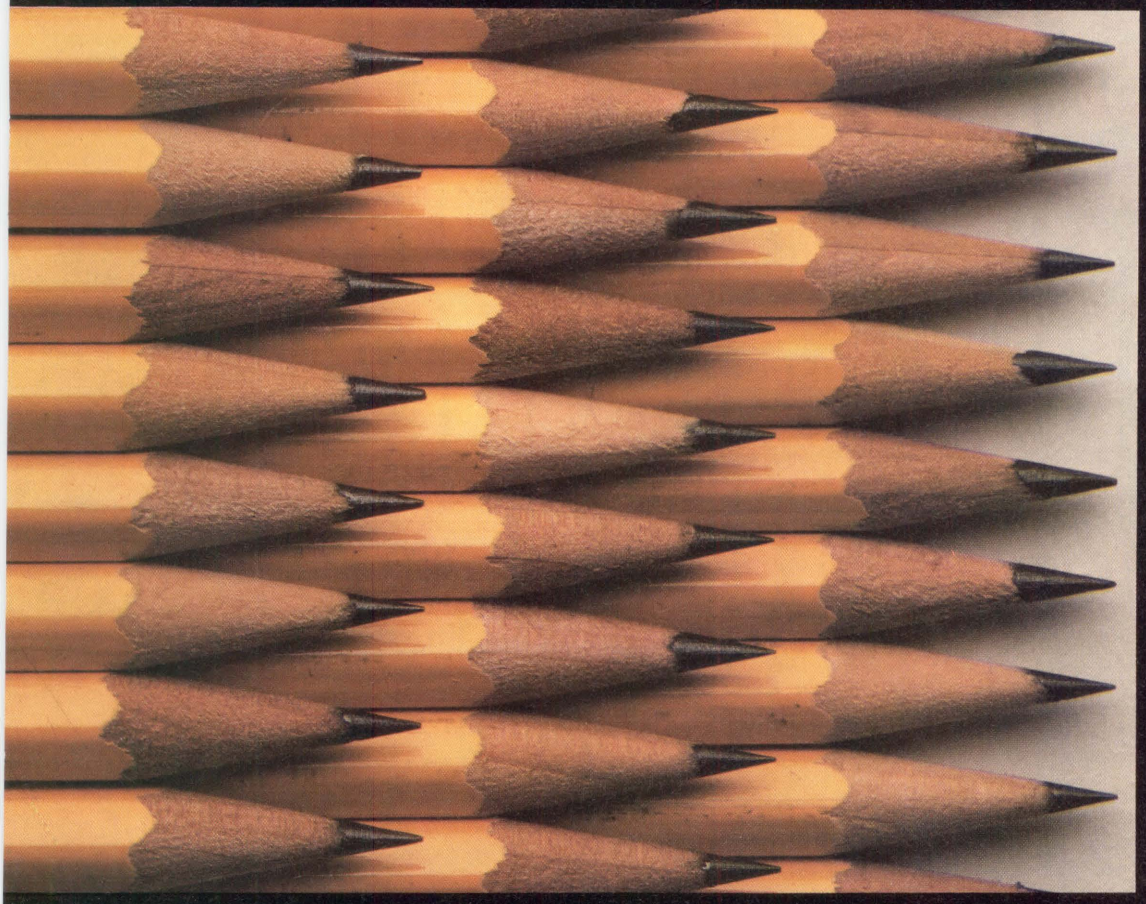
The total data format conversion time using the minicomputer is approximately 60 μs, or about 180 μs without an extended instruction set. If the computer is an LSI-11/03 minicomputer, the data format conversion time is twice as long. In this specific example, all gain factors and the scaling factor are powers of 2; therefore, it is possible to replace the multiplication by a bit shifting operation to reduce execution time. However, this is not necessarily the general case and therefore the multiplication method must be used for estimating the data format conversion speed.

The method described demonstrates that the array processor is about two orders of magnitude faster than a minicomputer in converting the data format. This method is also applicable to the conversion of other floating point data formats, such as the format with a "true" exponent instead of the 2-bit amplifier gain factor.

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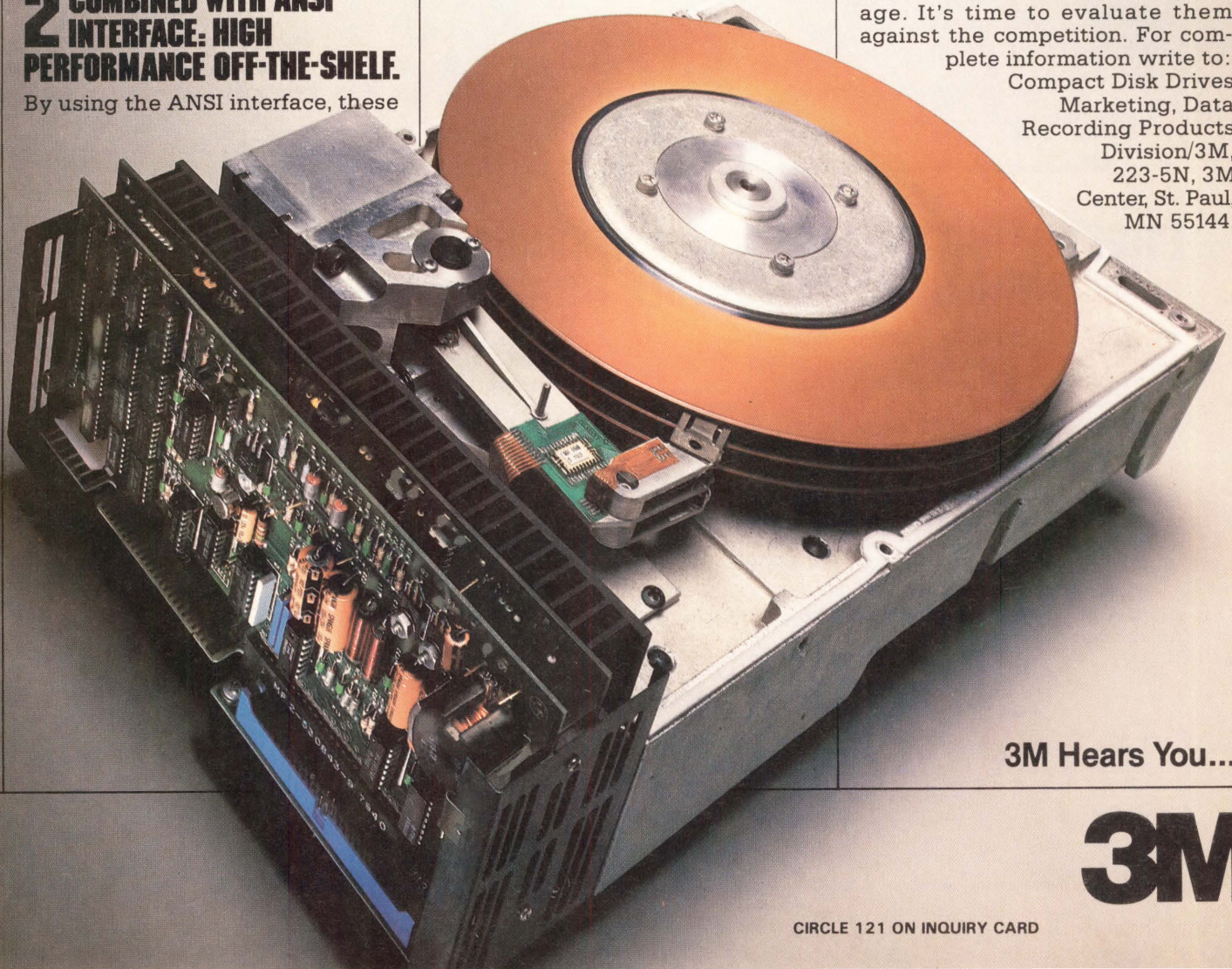
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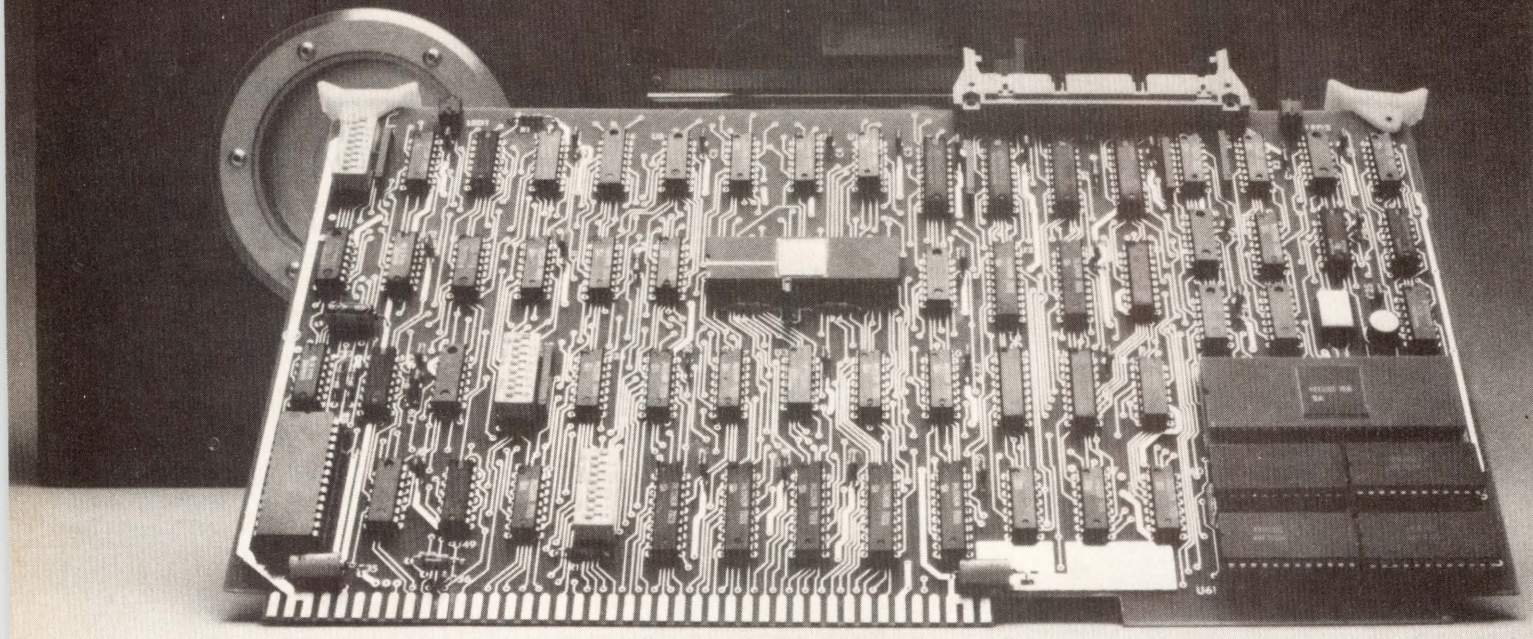


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by Joseph H. Deal

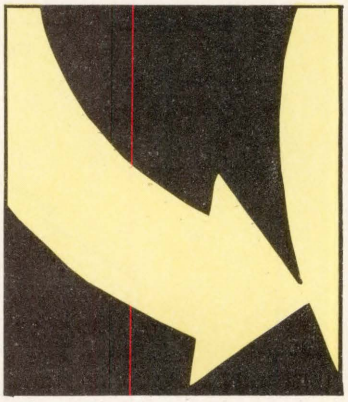
Time division multiple access is a key technology in the future of satellite communications. Advantages include more efficient use of satellite capacity than that of the traditionally used frequency division multiple access technique. It also provides for simpler, more flexible earth station design, and is directly compatible with digital terrestrial transmissions. Such advanced digital signal processing as forward error correction, digital speech interpolation, and data encryption can be used. Finally, the system is easy to operate and maintain.

In the United States a number of common carriers have made the transition from frequency division multiple access (FDMA) to time division multiple access (TDMA). American Satellite Corp, Germantown, Md, was the first to use TDMA in commercial service with TDMA earth stations in New York, NY, Los Angeles and San Francisco, Calif, and Dallas, Tex. Another carrier, RCA American Communications, Inc, Princeton, NJ, has implemented TDMA operation between Washington, DC, and San Francisco, Calif.

Joseph H. Deal is general manager at Aydin Microwave Division, 75 E Trimble Rd, San Jose, CA 95131, where he formed the digital telecommunications operation. Mr Deal has also managed satellite communication projects at COMSAT and developed the DIOS open-loop method of TDMA synchronization. Before that, he was professor of electrical engineering at Old Dominion University, Norfolk, Virginia.

Operation

In TDMA transmissions, all stations accessing a satellite transponder share the transponder in time by transmitting their traffic in bursts. These bursts of carrier signals are transmitted through the transponder in sequence and do not overlap (Fig 1).



In a typical arrangement for TDMA operation (Fig 2), the central office contains the voice digitizing equipment, the multiplexing equipment, and half the digital radio link, that typically operates at 78M bits/s in the 6- or 11-GHz band. The remote earth station contains the opposite half of the digital radio link and demultiplexing equipment to extract the individual T1 channels. These channels form the basic input to the TDMA terminal, which operates at a burst rate of 62M bits/s via a 36-MHz satellite transponder. At this rate the TDMA terminal can accommodate 40 T1 channels.

Satellite common carriers are moving from FDMA to TDMA technology.

Burst and frame structures

Bursts and frames are structured as shown in Fig 3. Within the frame, a burst is designated as a reference to enable transmit burst synchronization by using a loopback, feedback, or open-loop method. The receive burst synchronization is implemented by creation of detection apertures accurately positioned in time with respect to the frame reference time. All of these functions are

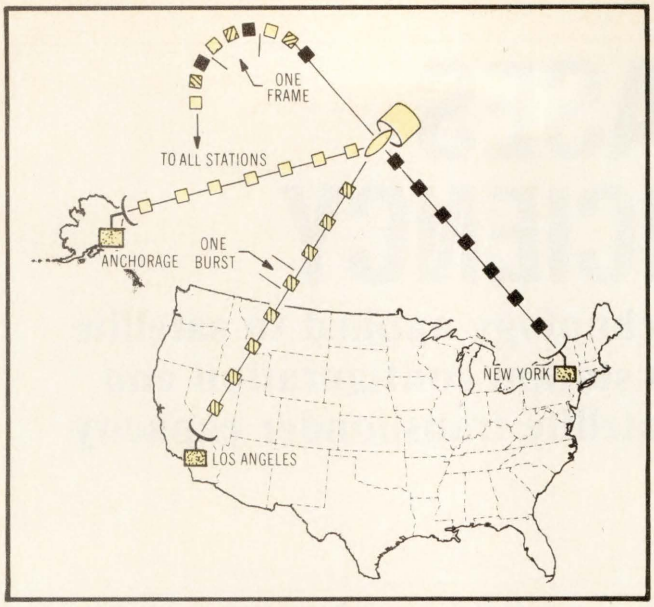


Fig 1 TDMA concept. Bursts of carrier signals are interleaved through satellite and are retransmitted to all earth stations

performed by the TDMA controller discussed under system configuration. Carrier burst length is variable, depending on the capacity requirement of the earth station. It begins with a preamble that includes the synchronization sequence, the unique word, and the station identification code. The unique word is a special bit pattern that, when detected, identifies the start of the burst data. The terrestrial interface module (TIM) follows this preamble. Up to 30 TIMs can be accommodated by the TDMA terminal developed by Aydin.

Terminal services capability

Any combination of data, voice, and video services can be handled by the TDMA terminal. Data rates include the common T1 and T2 rates—1.544M and 6.3M bits/s, respectively. Voice channels operate at a 64k-bit/s rate. Video service includes both teleconferencing and broadcast quality transmissions. Demand assigned multiple access (DAMA) techniques may be performed on any combination of the above to provide increased efficiency in satellite transponder utilization. In DAMA operation, satellite capacity is made available on demand of the end user. This is in contrast to preassigned operation, where satellite capacity is fixed and does not vary with the actual channel usage.

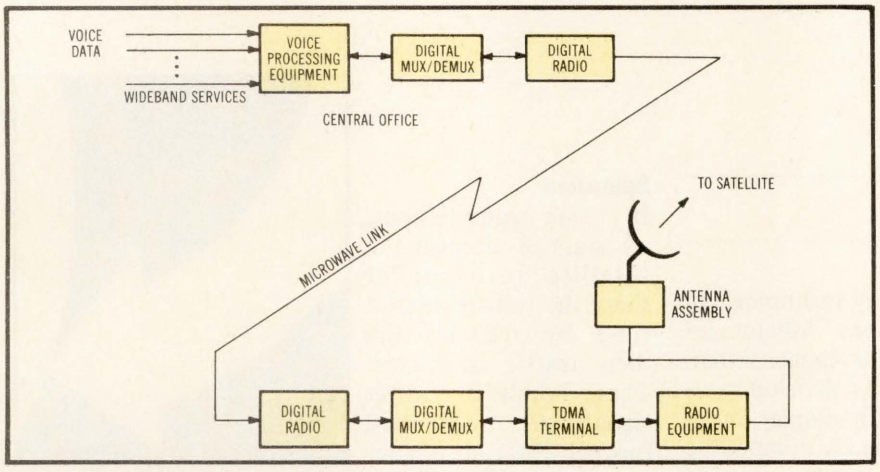


Fig 2 Typical terrestrial configuration for TDMA operation

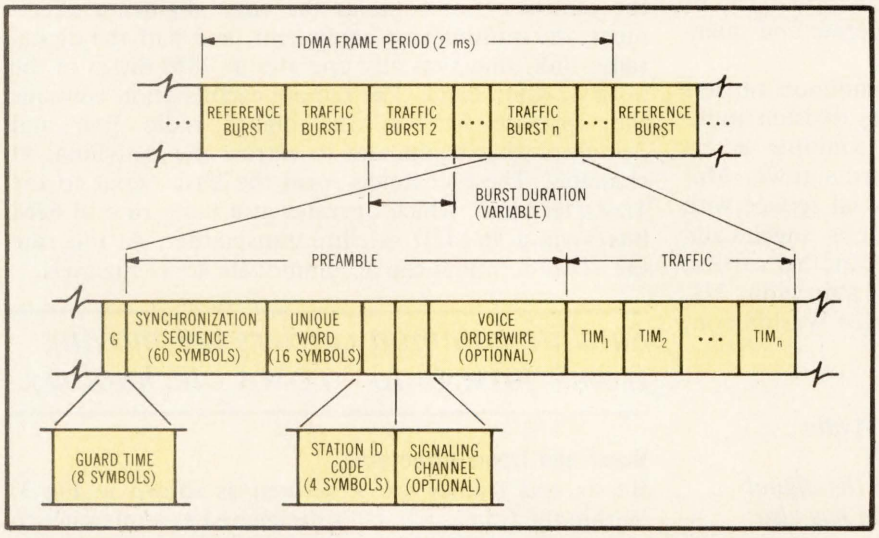


Fig 3 Frame and burst structure. Typical TDMA frame period is 2 ms with boundaries of 750 μs to 20 ms

TDMA system configuration

A block diagram of the Aydin TDMA terminal is shown in Fig 4. It may be considered in three sections: terrestrial interface, controller, and modem. The terrestrial interface section consists of the terrestrial switch matrix, the TIM, and the TIM bus. An optional orderwire module is also included in this section. The controller section is the heart of the TDMA system. It consists of the TDMA controller and the optional forward error correcting (FEC) and data encryption units. The modem section comprises the TDMA modem and equalizers; this section also includes the optional transponder hopping switch. Transponder hopping is a technique by which a single TDMA terminal can access several satellite transponders in one TDMA frame. This increases the effective network capacity by the number of additional transponders used.

TIM functions include: compression/expansion buffering; redundant bus interface and switchover circuitry; bit stuffing; onboard fault detection and reporting to the control microcomputer; address recognition and online and offline testing capabilities. TIM transmit and receive configurations are quite similar (Fig 5).

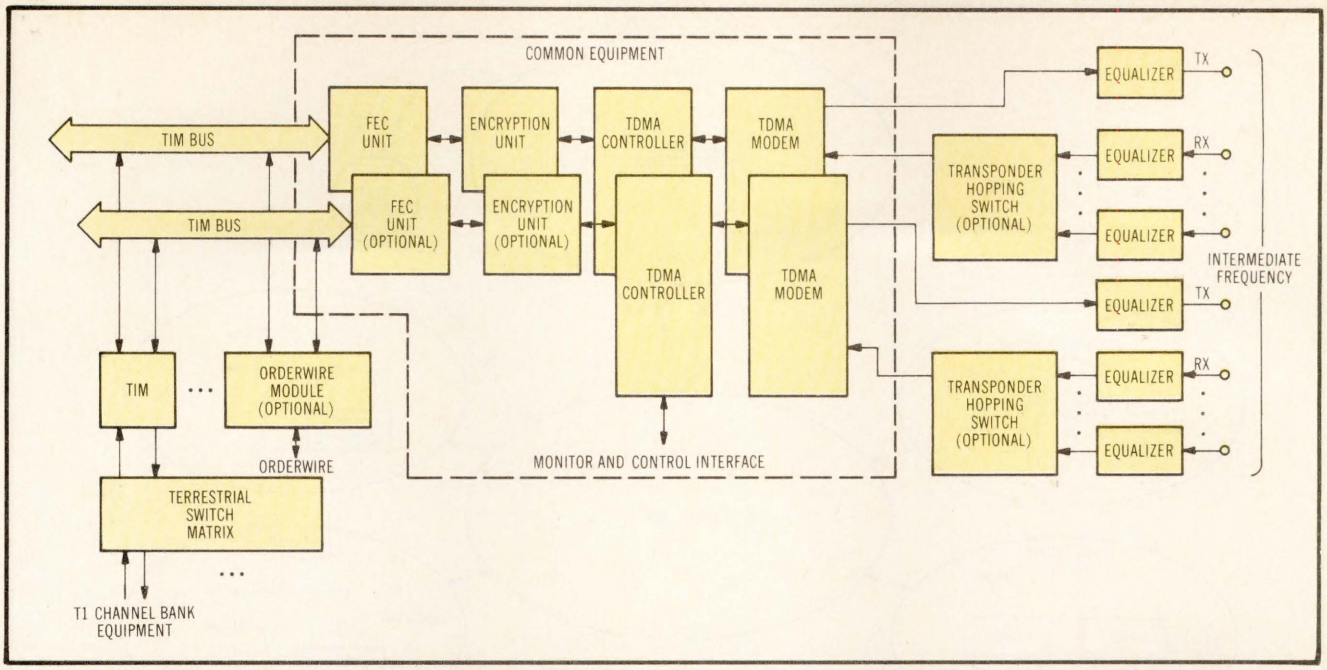


Fig 4 Redundant TDMA terminal configuration. Terminal design is optimized for unattended operation. It accommodates remote monitor and control with automatic redundancy switchover. Monitor and control can be performed via satellite using signaling channel in burst preamble or via terrestrial lines

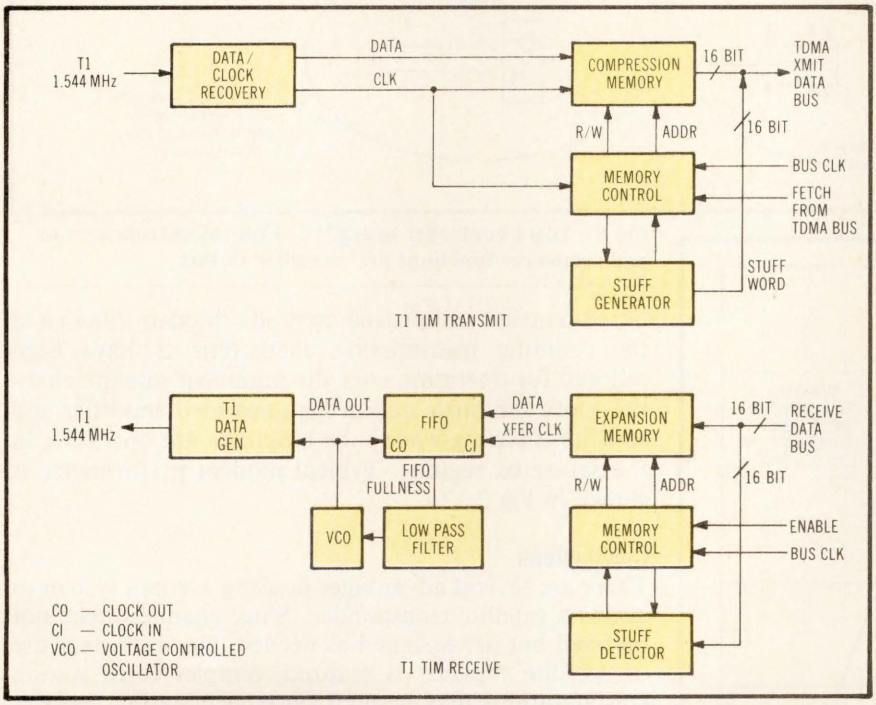


Fig 5 TIM transmit and receive sections. Receive side includes phase-lock loop for bit timing recovery

The TIM bus is a 16-bit wide data path that allows the system great flexibility. It provides a simple arrangement for adding TIMs to the system, allows TIM timing to be insensitive to propagation delays to and from the controller section, and provides compatibility with a wide variety of LSI circuits. The TIM bus also allows the TIMs to be selectively addressed, greatly simplifying burst and channel multiplexing/demultiplexing.

The TDMA controller is the heart of the system in that it is microprocessor controlled and centralizes the transmit and receive functions. It controls the following housekeeping functions: burst synchronization processing; fault detection and isolation; communications with other controllers; operator interface; and management of the high speed controller. High speed control is accomplished through a part of the controller called the sequencer (Fig 6). Sequencer functions include high speed control, measurement of timing and high speed events, and recognition of special event occurrences.

Two optional units are included in the controller, the FEC and the data encryption unit. Initially, the FEC is a rate 7/8 codec using a modified Hamming block code; rate 3/4 and 1/2 codecs are also available. As applications may require, other code rates will be available at the high speed ports along with the convolutional coding technique on individual terrestrial ports. The data encryption unit will be provided as a plug-in module, and will conform to the National Bureau of Standards Data Encryption Standard.

The TDMA modem consists of three principal sections, modulation, demodulation, and synchronization, implemented on three plug-in modules. The modem has been optimized for burst operation through the nonlinear channel, and synchronization designs are

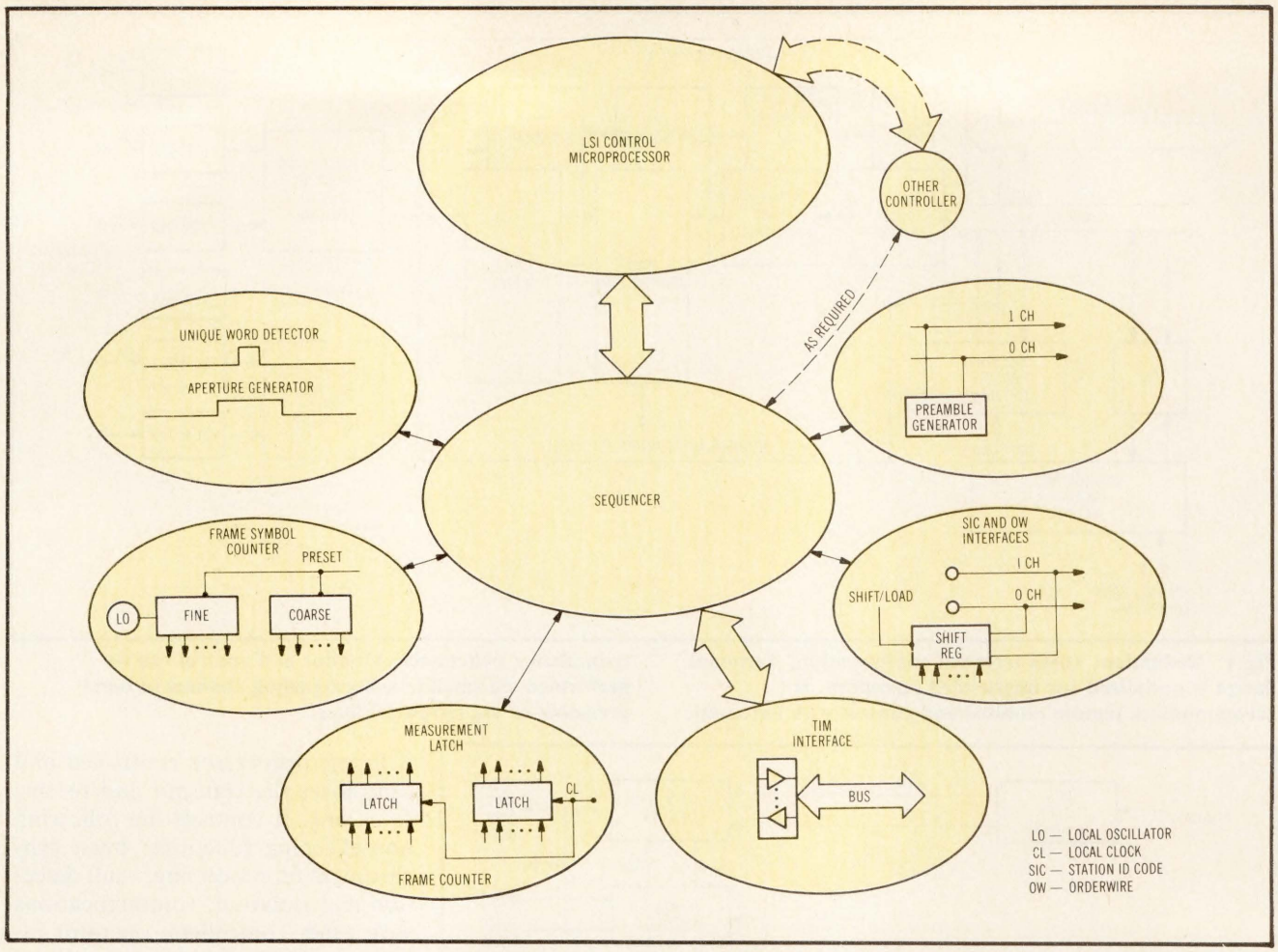


Fig 6 TDMA controller operation. Control microprocessor and sequencer functions are described in text

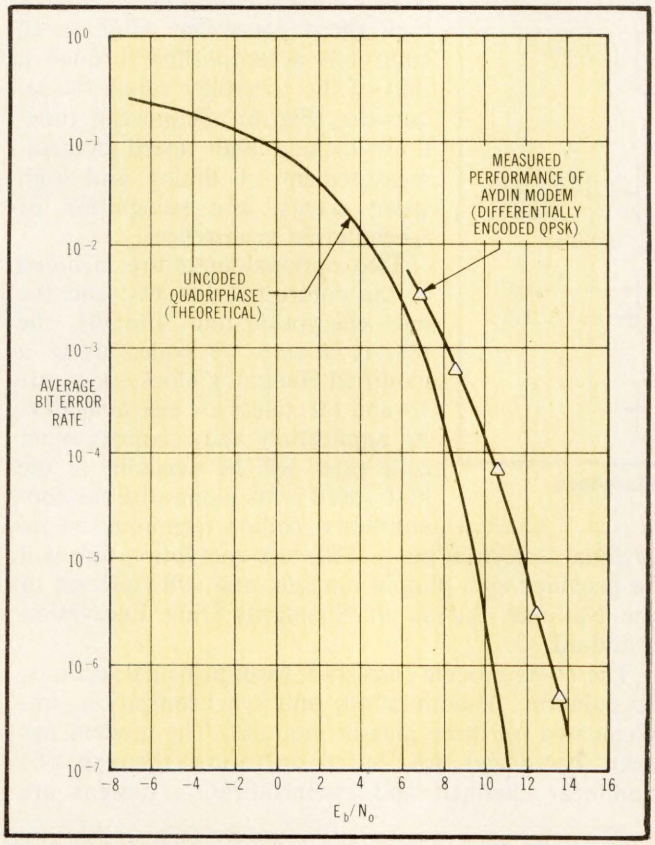


Fig 7 TDMA modem performance. Graph shows continuous mode bit error rate performance of TDMA modem prototype. E_b/N_o is energy per bit to noise density ratio

based on tried and proved methods. Modem filters and the resulting transmission characteristics have been tailored for operation over the nonlinear satellite channel. Both the earth station high-powered amplifier and satellite traveling-wave tube amplifier are operating in the saturated regions. Typical modem performance is shown in Fig 7.

Conclusions

There are several advantages in using a TDMA system to access a satellite transponder. Since channels need not be fixed but are assigned as needed, more efficient use of satellite capacity is realized. Simpler earth station configurations may be used since each station requires only one transmitter and receiver. The TDMA system is also compatible with currently used digital terrestrial transmission techniques, and can handle advanced digital signal processing.

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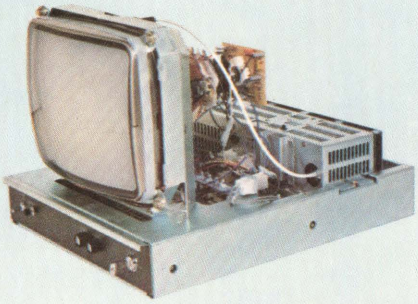
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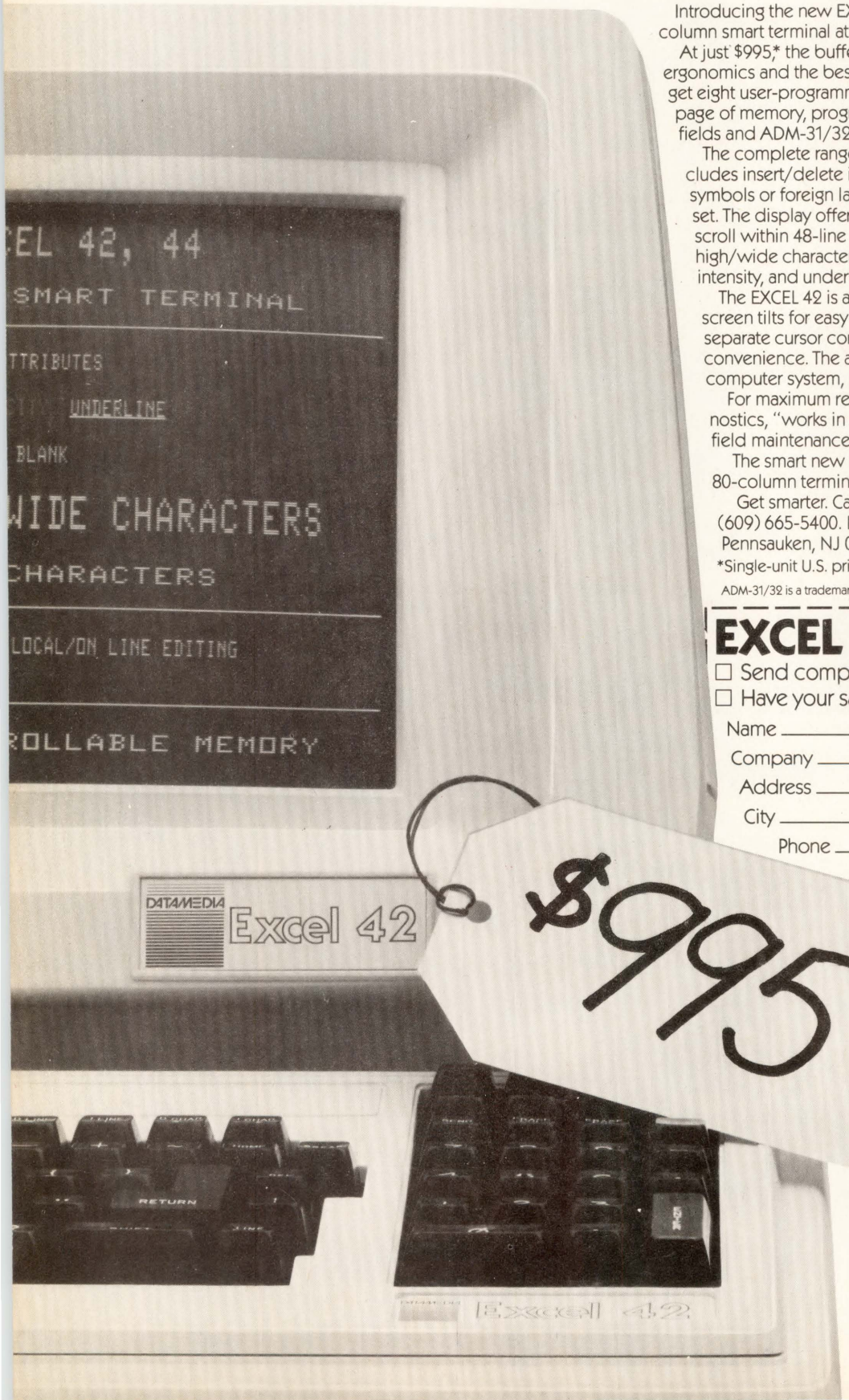
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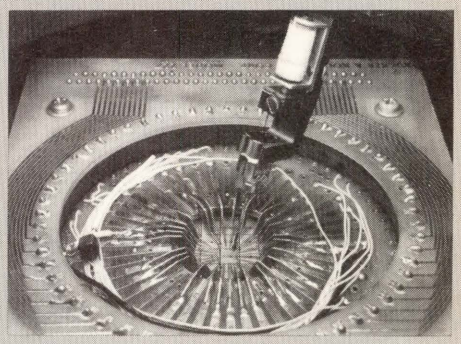
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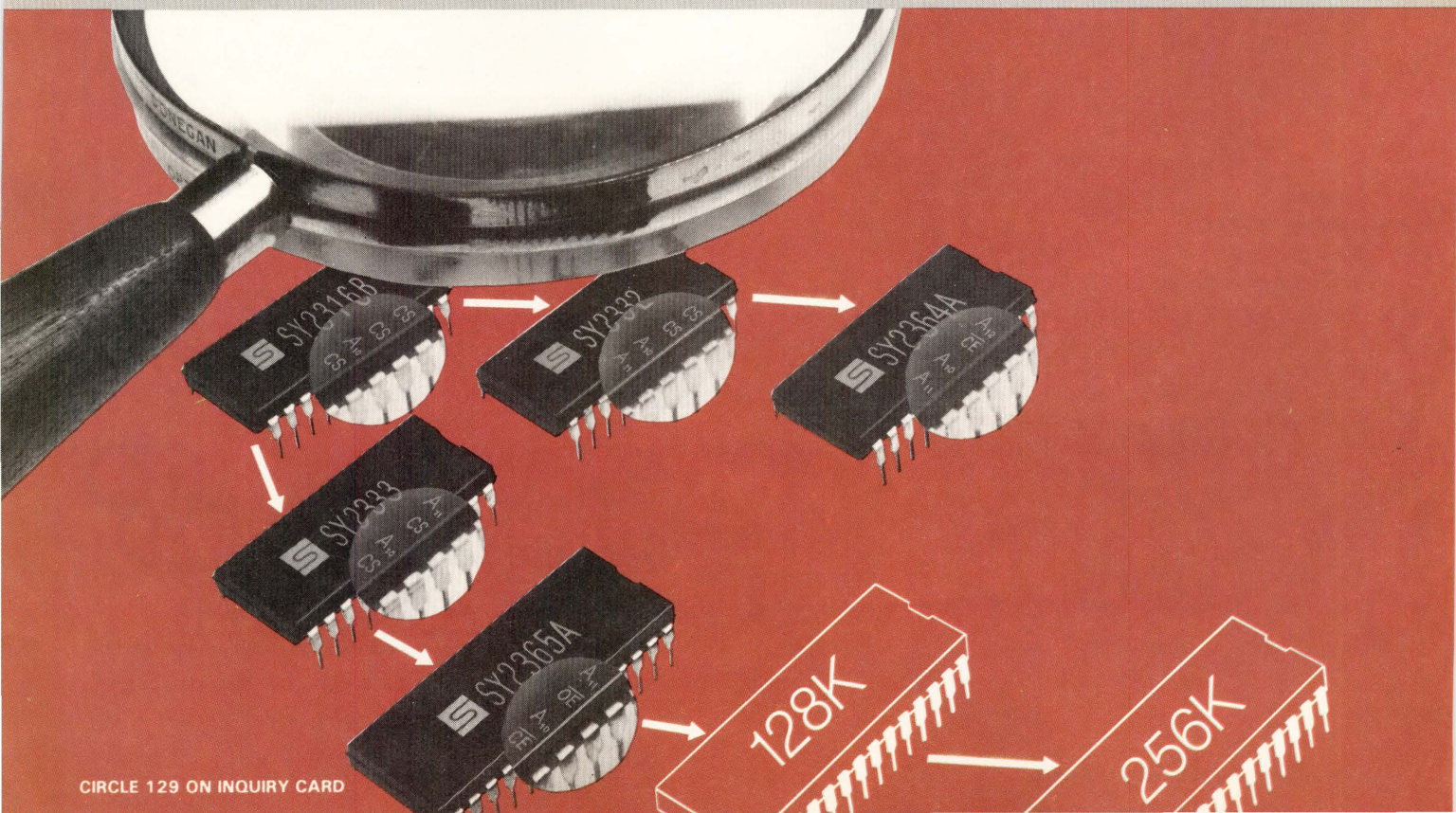
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LASER SCRIBING ON MAGNETIC DISC

Laser technique manufactures "bad" discs for calibrating disc test equipment

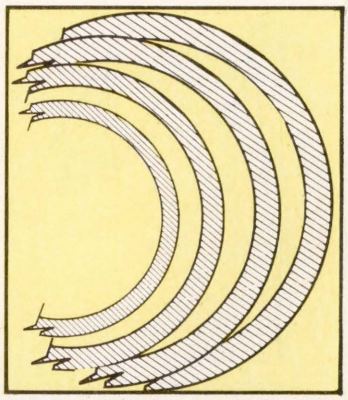
by Sam R. Cowan and David L. Peterson

Lasers can etch closely controlled voids in the oxide coating of a magnetic disc. These voids can then help correlate and calibrate disc error testers and disc glide testers. They are superior to other means of tester calibration because they account for both the read/write head characteristics and the electronics. A C-shaped laser scribe can correlate error testing even when the testers differ.

One way to generate an error standard magnetic disc is to choose a disc at random, test it on a calibrated tester, and count the number of missing, or extra, pulses that result. Defects on this kind of error standard disc stem from its manufacturing process. The number of errors will vary from disc to disc, and it will be difficult to find another sample with a similar error count. The rate of change—or slope—of the error count also varies drastically from disc to disc. Error slope is defined as the change in error count per unit change in detection threshold. Production discs selected as error standards can vary in error slope by a factor of several hundred. Another problem with using a production disc as an error standard is that its error count changes over time. Constant handling and testing will add errors to the disc in an unpredictable fashion.

Sam Cowan is manufacturing engineering manager, Head/Disk Depart for Storage Technology Corp, 2270 S 88th St, Louisville, CO 80027. Mr Cowan holds a BS degree in physics and mathematics from Nebraska Wesleyan University.

David Peterson is a quality standards engineer Disk Div, for Storage Technology Corp, 2270 S 88th St, Louisville, CO 80027. He previously was an instructor of physics and mathematics at the University of Colorado at Boulder, from which he received a BS degree in engineering physics and an MS degree in physics.

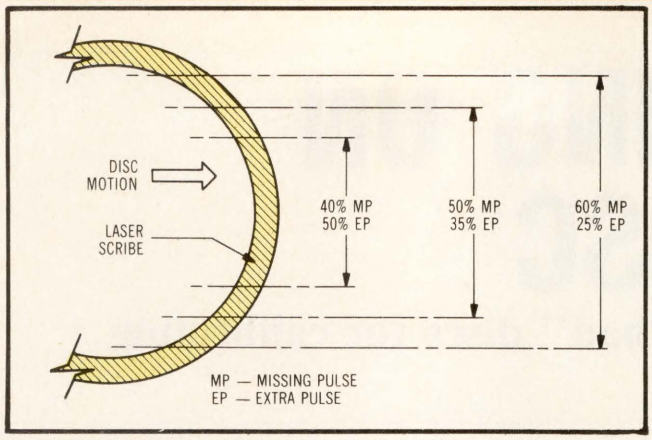


To avoid the problems caused by using a random production disc, the error standard can instead be built by placing predetermined errors on a relatively good disc. These predetermined errors involve a semicircular laser scribe of constant width that extends right down to the aluminum substrate. (See the Panel.) When the recording head first encounters the scribe, it is positioned at the center of the semicircular arc where the effective scribe width is 0.5 mil (13 μm). This represents a signal loss of 25% when compared to the total track width of 2.0 mils (50 μm). As the head moves across the scribe, the amount of missing oxide compared to track width approaches 100%. Then, as the head moves to the other end of the scribe, the missing pulse percentage falls until there is again 75% signal remaining.

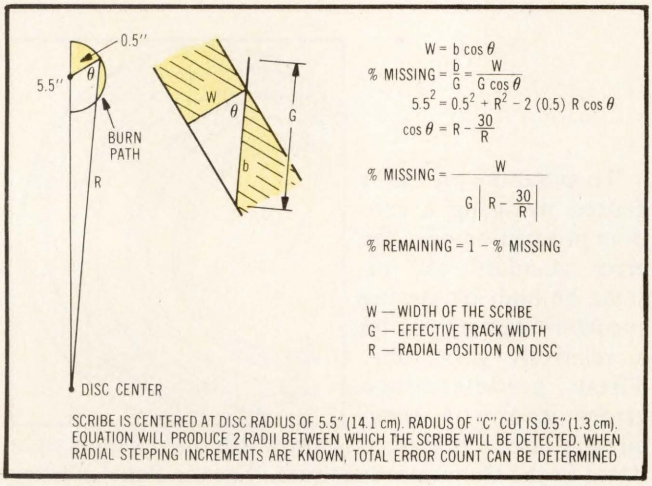
A C-shaped laser scribe can correlate error testing even when the testers differ.

If the detection threshold is set to 60%, a properly calibrated tester will detect this scribe at a radius shown in the Panel. It should continue to detect the scribe as an error on every track until it comes to the corresponding radial position on the other side of the scribe. For any given threshold, the number of missing pulses remains fixed. If the threshold changes, for instance, to 50% of the remaining signal, the scribe will be detected as a missing pulse over a smaller radius than at a 60% threshold.

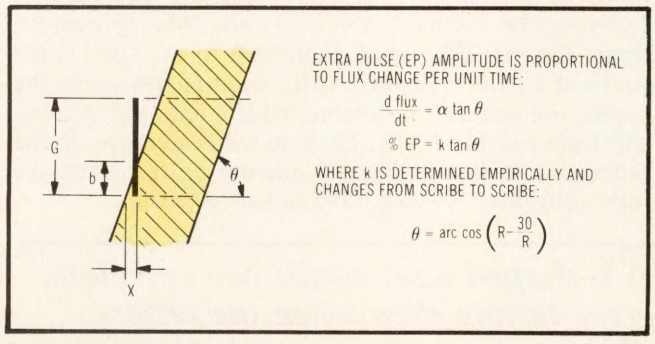
The number of extra pulses produced by a laser scribe is also unique to each detection threshold. At the center of the scribe, the head encounters a sharp discontinuity in the oxide coating. This will produce a large extra pulse, since pulse magnitude is proportional to flux change per unit of time. When the head is not at the



Scribe orientation



Missing pulse calculations



Extra pulse calculations

center of the scribe, the amplitude of the extra pulse drops off. The angle of the scribe to the read/write gap then changes, and the scribe is no longer a sharp discontinuity.

The scribe produces a unique number of extra pulses for every detection threshold. The total radius over which the tester detects an extra pulse caused by the scribe depends on the detection threshold. The lower the threshold, the larger the radial dimension over which an extra pulse is detected.

The number of extra pulses produced by a laser scribe is also unique to each detection threshold.

Physical dimensions of the scribe are critical and are dependent on the particular application. The minimum width of the scribe is constrained by the physical half wavelength of the $2f$ frequency. For example, at 4.8 MHz and 3600 r/min, the one-half wavelength on the inside diameter is about 4.25 μm. The scribe therefore must be wider than 4.25 μm to drop the entire half wavelength.

Maximum scribe width depends on the effective track width for the heads and the missing pulse detection threshold. If a 2.0-mil (50-μm) head is used and the scribe is 2.0 mils wide, the tester will detect a missing pulse across the entire scribe. This does not give the desired condition of a unique error count for each threshold. Instead, if a 2.0-mil head is used and the missing pulse threshold is 50%, the scribe width must be less than 1.0 mils (25 μm)—a 0.5-mil (13-μm) scribe would work quite well. The scribe width is important only for missing pulse considerations. Extra pulses do not depend on the width, but rather on the sharpness of the scribe edges.

The scribe radius determines the length of the scribe, and the total length of the scribe in the disc radial direction determines the number of errors that the tester will detect. In terms of error count, errors due to the scribe should greatly exceed other errors that might exist on the disc. Scribe radii of 0.3 to 0.5" (8 to 12 mm) have worked well in practice.

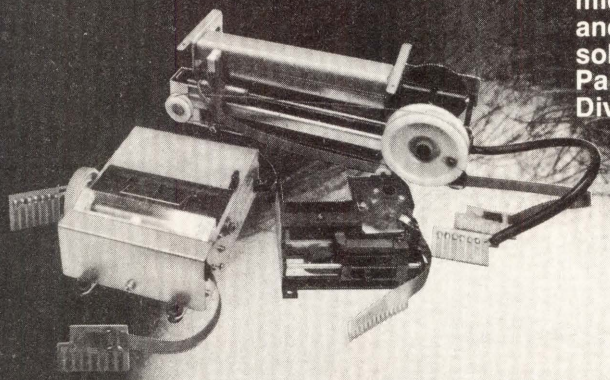
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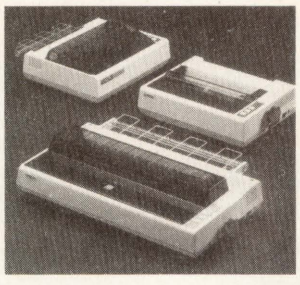
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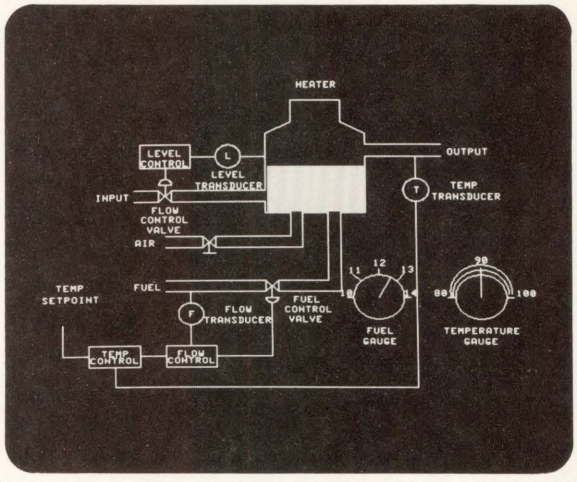
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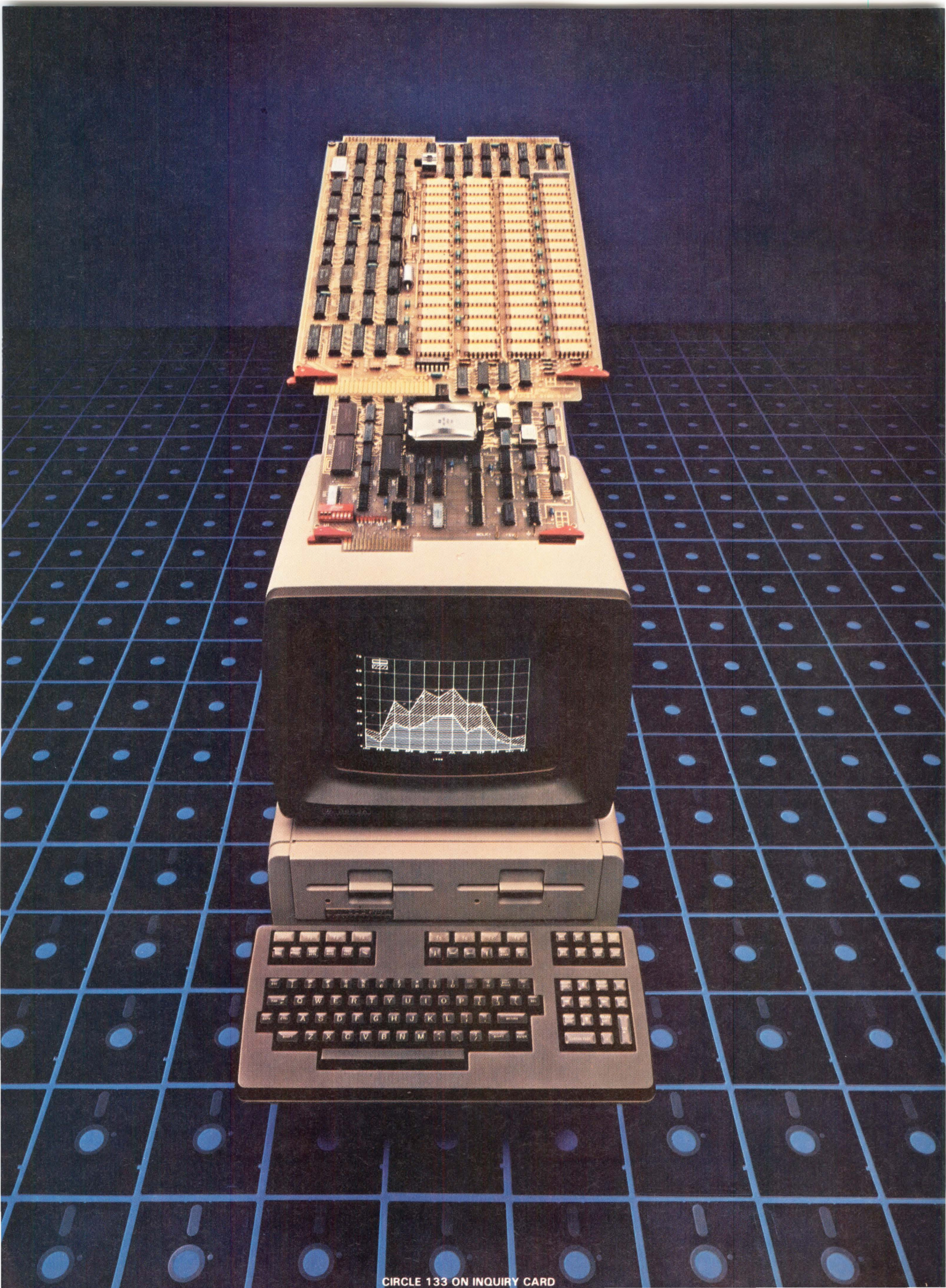
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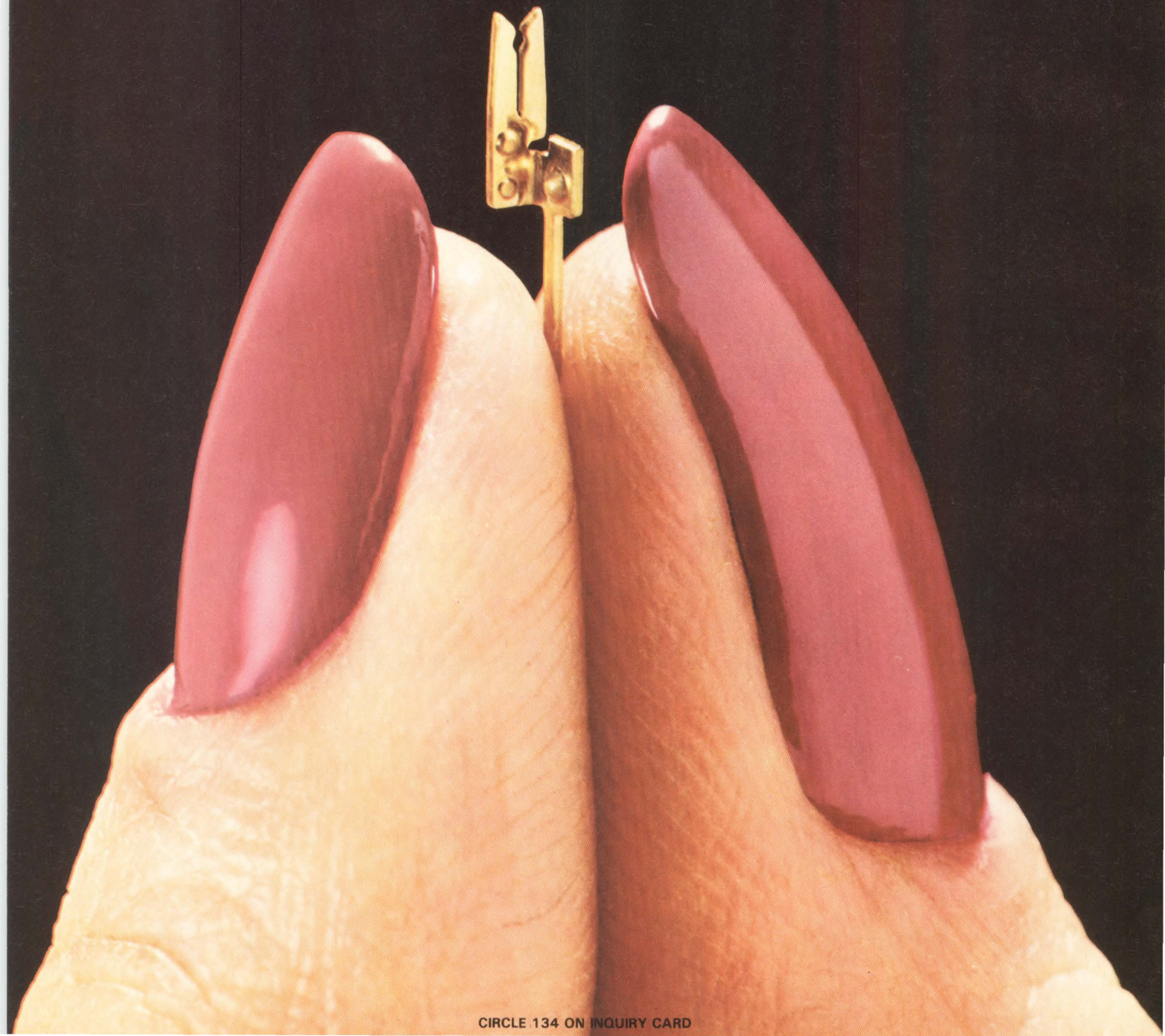
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VMOS TRANSISTORS INTERFACE ICs TO HIGH POWER LOADS

Several precautions, not obvious at first glance, must be taken when VMOS transistors are used to interface high power loads with ICs

by Bill Roehr

Vertical metal oxide semiconductor transistors are well suited to interface power loads with integrated circuit logic. Although circuit design is simple, a few rules and precautions must be observed to minimize power dissipation and have reliable operation. This article will consider the nature of the load, the general driving requirements of vertical metal oxide semiconductors, and the output characteristics of the logic element.

Load considerations

Freedom from second-breakdown limitations makes driving highly inductive or capacitive loads a natural application for a vertical metal oxide semiconductor (VMOS). Inductive loads include transformers, solenoids or relays. Generally, high current inrush loads such as incandescent lamps, pulse-forming networks, and motors also are handled easily. Some attention must be paid to the load characteristics, however. In common with bipolar semiconductor devices, VMOS transistors can be damaged if their voltage ratings are exceeded. Although their avalanche energy capability is much greater than that of bipolar transistors, a good design does not allow the VMOS to absorb inductive energy unless the part is rated for this type of service. Spikes generated from inductive loads can have tremendous energy content; usually, some means of limiting their amplitude must be provided.

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In addition, the transient power generated during turn-on and turn-off intervals must be determined to check for excessive channel temperatures. Highly inductive loads may generate significant power on turn-off, whereas capacitive-like loads cause power surges on turn-on. The power waveform should be obtained, a suitable rectangular model derived, and peak junction temperature computed.[1,2] This calculation is especially important for incandescent lamp and motor loads; their current surges last from tens to thousands of milliseconds, causing a significant temperature surge in the VMOS power driver.

Inductive loads. Usually with inductive loads the peak voltage spike should be limited to a value below the breakdown rating of the transistor. Typical circuits for three commonly employed techniques are shown in Fig 1. A freewheeling diode effectively handles spikes caused by most electromechanical inductive loads, such as solenoids or relays. Low diode impedance usually causes a long current decay time, however, which can be intolerable in some applications. Speed may be traded

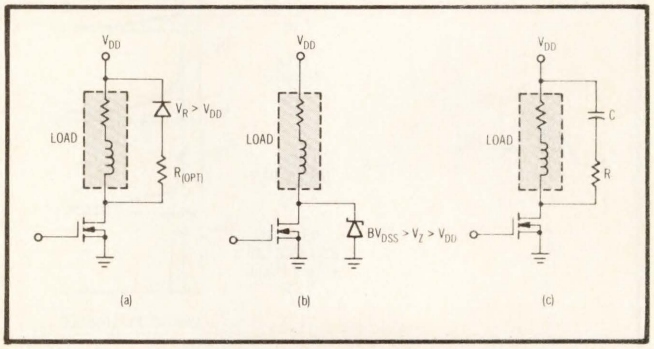


Fig 1 Methods of limiting inductive spikes. Freewheeling diode clipper (a) limits most electromechanical spikes. Zener diode clipper (b) can be safer and cheaper. In power conversion, RC snubbing (c) reduces power dissipation and limits transformer leakage and wiring inductance spikes

for overshoot voltage by using a resistance R in series with the diode.[3] The freewheeling diode can be an inexpensive rectifier, such as the IN4002. However, junction rectifiers exhibit a turn-on transient that can allow excessive overshoot if the VMOS transistor is being driven off rapidly. For high speed switching, a Schottky or low voltage ion-implant rectifier is required; the ordinary, fast recovery rectifier does not have a fast turn-on time.

Often the safest and least expensive limiting technique is to use a Zener diode. The Zener responds in picoseconds and can protect the VMOS from supply transients as well as from inductive spike; consequently, Zener limiting is particularly attractive on raw power buses. In a manner similar to that using a resistor in series with a freewheeling diode, the load current decays faster as the clipping level rises higher above the supply voltage.

The resistive-capacitive (RC) snubber is commonly used in power conversion circuits to limit spikes caused by transformer leakage inductance and wiring inductance. It also reduces power dissipation by shaping the load line to appear more resistive. Resistor R, in series with the capacitor, is required to limit the current surge on turn-on (a good idea even when VMOS is used) and to ensure that the circuit is adequately damped. Since the circuit is basically a resonant tank, it will exhibit a damped oscillation unless the circuit Q is ½ or less. Values are usually empirically determined. Peak voltage across the network will not exceed that calculated using the energy relationship

$$\tfrac{1}{2} LI^2 = \tfrac{1}{2} CV^2$$

Solving for the voltage, it is found that

$$V = I\sqrt{L/C}$$

The resonant frequency can be calculated from the usual relationship and R selected so that $Q \approx \tfrac{1}{2}$ by using

$$R = 4\pi fL$$

The equations and experience both indicate that higher values of C lower the peak voltage and resonant frequency, and consequently the resistor R also must be reduced. An optimum value exists for a given LC combination, which results in minimum overshoot. Another consideration is to minimize the power dissipation in the transistor.[4,5]

Capacitive and high inrush loads. Usually auxiliary circuitry is not required with capacitive-like loads. It is necessary, however, to keep the load line within the safe area curves of the VMOS transistor in order to avoid excessive temperature excursion during current inrush. When inrush power is excessive, increasing the gate drive will usually reduce it and may hold it within bounds. In Fig 2, the lamp circuit (at left) and waveforms will be used to discuss some design considerations.

The Fig 2 graphs labeled "Current Determined by Load" illustrate the typical transient current, voltage, and dissipation of a VMOS transistor driving an incandescent lamp load where the VMOS is not drive limited—it can supply all the current that the load demands while maintaining operation in the ohmic region. Under these conditions, the output voltage quickly swings from its off state (V_1) to its on state in a time dictated by the transient gate drive current and the VMOS capacitances, as shown in (a). The peak current shown in (b) is a function of the lamp's cold resistance and decays quasi-exponentially as the lamp filament heats and resistance increases. The transistor dissipation waveform is similar to the power waveform of (c); this can be equated to the rectangular power pulse of (d) to simplify peak and average power calculations.

The case where the power transistor is drive limited (when it cannot supply all of the peak current that the load demands) usually—but not always—results in greater transistor dissipation. The usual situation is illustrated in the transient waveforms of the Fig 2 graphs labeled "Current Limited by Gate Drive," where the peak current is much less than in the previous example, but also where transistor operation does not enter the ohmic region initially during the switching transition. The resulting power dissipation pulse is greater and may be excessive.

VMOS transistors make ideal drivers for incandescent lamps because they can handle higher current surges than a similarly rated bipolar transistor. Lamp drivers may need to handle two types of surges, cold resistance inrush and flashover. Cold resistance inrush occurs on all lamps during turn-on; the peak is between 12 and 18 times the steady state current. Furthermore, the inrush current may be from 2 to 5 times the rated current 5 ms after power application. Inrush depends somewhat upon the lamp's design and the cold temperature of the bulb, which in turn is dependent upon the lamp's operating duty cycle and ambient temperature. Since the turn-on surge is a repetitive transient, for maximum VMOS reliability the VMOS transistor must function within the safe operating area.

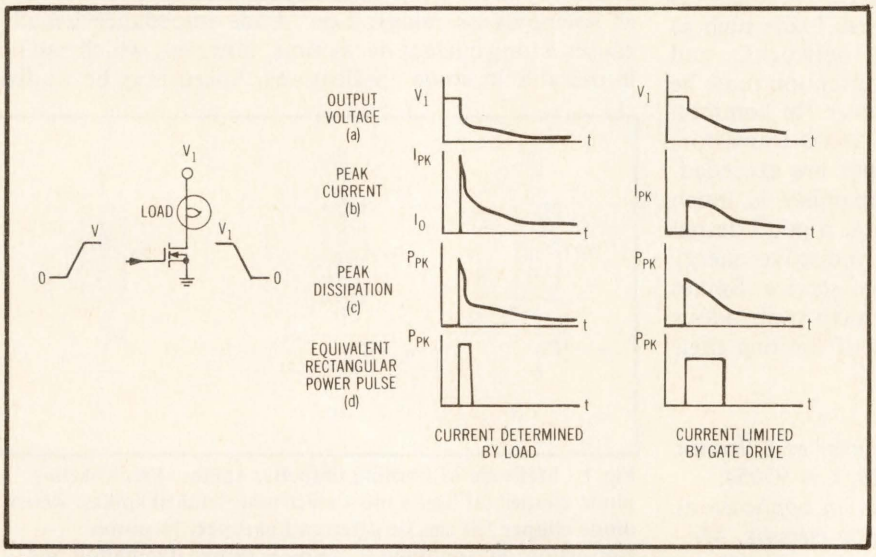


Fig 2 Transient current, voltage, and dissipation. VMOS transistor shown here drives incandescent lamp. High inrush loads develop similar waveforms

Flashover surge occurs during the failure of a gas-filled lamp. (All

lamps over 60 W designed for 120 V, or higher voltage lines, contain some gas for improved efficiency and life.) As the filament burns out an arc develops, causing an extremely high surge on the order of 80 to 200 A with a baseline of 2 to 4 ms. Coping with this surge is a problem for the circuit designer when bipolar devices, such as junction transistors or thyristors, are used. If a device rated adequately for the steady state and inrush current is used, the flashover surge will cause failure. If a device rated to handle the flashover is used, cost is usually out of bounds because the device ratings far exceed those required for normal use. Semiconductor fuses can be used, but these are expensive. With VMOS power devices, nonrepetitive operation can often exceed the safe operating area without causing a failure; the actual nonrepetitive rating is usually not published but may be obtained from the VMOS manufacturer.

General driving considerations

Regardless of the type of logic or network used to drive a VMOS transistor, consideration must be given to such VMOS properties as the input protection Zener diode; the high frequency response; and the capacitive input impedance. The input protection Zener diode integral with some devices places restrictions on the drive levels. The positive voltage on the gate with respect to the source should not exceed the maximum voltage rating of the Zener diode, nor should the Zener become forward biased by allowing the gate-to-source voltage to become negative.

The reasons for these restrictions are evident from the Fig 3 circuit. The Zener is the base-emitter junction of a bipolar transistor and exhibits a negative resistance characteristic similar to the BV_{CEO} of a transistor. Above a few hundred microamperes, the voltage may switch from, for example, 20 to 8 V. The lower voltage will limit the amount of current available from the VMOS transistor and excessive dissipation in the Zener and drive circuitry may occur.

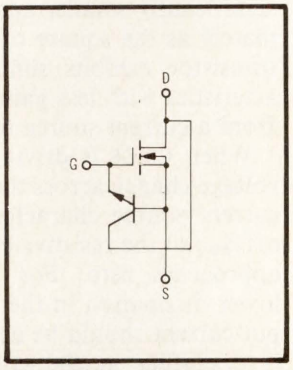


Fig 3 Parasitic npn transistor. Device is in monolithically constructed Zener protected MOSFETs. Zener diode is base-emitter junction of bipolar transistor. Transistor collector connects to drain

If the drive circuit can cause a negative gate-source voltage—a common situation with a source follower driving a capacitive load—the bipolar turns on in the forward direction, causing a flow of current from the drain terminal to the gate terminal. The device can be damaged by excessive current if the current loop impedance is very low, but usually this is not a problem unless the drain-source voltage is high enough to cause the bipolar to operate in a $BV_{CEO(SUS)}$ mode. Since the BV_{DSS} rating of the field effect transistor (FET) is essentially the BV_{CBO} rating of the bipolar, $BV_{CEO(SUS)}$ is approximately one-half of BV_{DSS}. Consequently, a second-breakdown failure of the Zener bipolar may occur when the drain-source terminal voltage exceeds one-half of BV_{DSS}. If negative gate voltages are unavoidable, a VMOS part that does not have an input Zener diode should be used.

The carrier transit time through the channel is under 1 ns for most VMOS structures, resulting in cutoff frequencies on the order of 1 GHz. Consequently, very fast switching is readily achieved, but parasitic oscillations can be troublesome if one or more of the following guidelines are not observed: keep lead and trace lengths short, particularly those connecting to the gate; place ferrite beads on the gate lead close to the gate terminal, or use an appropriately chosen resistor in the range of 10 to 1000 Ω in series with the gate; avoid a layout that may couple an output signal to the input; and surround the VMOS transistor with a ground plane and shield output from input.

Since VMOS gate input resistance is essentially infinite, many VMOS transistors can be driven from a complementary metal oxide semiconductor (CMOS) or transistor-transistor logic (TTL) output. However, the input impedance of a VMOS is capacitive and the drain current essentially follows the voltage on the gate. Although switching speed, in itself, is not important when driving a lamp or electromechanical load, the limited transient current available from the logic element may result in switching slow enough to cause significant transient power dissipation, particularly when several VMOS stages are being driven in parallel. Accordingly, a transient analysis is usually required.

A fairly simple yet accurate analysis uses a charge control approach, as described by Evans and Hoffman.[6] For any particular time interval,

$$\Delta t = \frac{(\Delta V_{GS})(C_{in})}{I_G}$$

where

ΔV_{GS} = gate-source voltage change
C_{in} = effective input capacitance
I_G = average gate current during switching

All the preceding values must be determined for a specific time interval.

The table, "Pertinent switching relationships," shows the appropriate quantities to use in the equation. For completeness, turn-on and turn-off delay relations are included, but these intervals are rarely of interest in power circuits. However, dissipation may be a problem during rise and fall times. Capacitance values used are the average values as V_G varies over the ranges shown for the time interval of interest. Appropriate V_{DS} values must also be used to determine the capacitance. Key V_{GS} points are:

$V_{G(off)}$ = off-state gate voltage prior to turn-on
$V_{G(TH)}$ = threshold gate voltage
V_G at $I_{D1(on)}$ = V_G corresponding to the peak value of drain current for capacitive or resistive loads or the value of drain current when the drain voltage enters the ohmic region for inductive loads
$V_{G(on)}$ = on-state gate voltage prior to turn-off
V_G at $I_{D2(on)}$ = V_G corresponding to the value of drain current flowing prior to turn-off

Pertinent switching relationships

Interval	Symbol	Gate voltage change	Capacitance
Turn-on delay	$t_{d(on)}$	$V_{G(TH)} - V_{G(off)}$	C_{iss}
Rise time	t_r	V_G at $I_{D1(on)} - V_{G(TH)}$	$C_{iss} + \frac{\Delta V_{DS}}{\Delta V_{GS}} C_{rss}$
Turn-off delay	$t_{d(off)}$	$V_{G(on)} - V_G$ at $I_{D2(on)}$	C_{iss}
Fall time	t_f	V_G at $I_{D2(on)} - V_{G(TH)}$	$C_{iss} + \frac{\Delta V_{DS}}{\Delta V_{GS}} C_{rss}$

Driving from CMOS logic. Widely used CMOS logic elements are ideal for direct coupling to VMOS power transistors, because CMOS can operate with supplies up to 15 V—a level that provides ample drive for VMOS. Since VMOS switching speed and transient load handling capability is related to the output impedance of the drive source, a brief examination of the CMOS circuit follows.

CMOS circuits usually have an output configuration like that of the inverter in Fig 4. The inverter consists of a p-channel MOSFET connected in series with an n-channel MOSFET (drain-to-drain) with the gates tied together and driven from a common signal. When the input signal goes positive, the p-channel FET is essentially off and conducts only I_{DSS} (pA). The n-channel unit is forward biased, but since only I_{DSS} is available from the p-channel, V_{DS} is very low. Conversely, when the input goes low (zero), the p-channel device is turned full on, the n-channel device is off, and the output will be very near the positive rail. Since the current (without a load) is extremely small, the inverter dissipates almost no power in either stable state; the only dissipated power of consequence occurs during the switching transitions as capacitances are charged. Because of the extremely high input impedance of VMOS, the CMOS gate can interface with many VMOS power transistors.

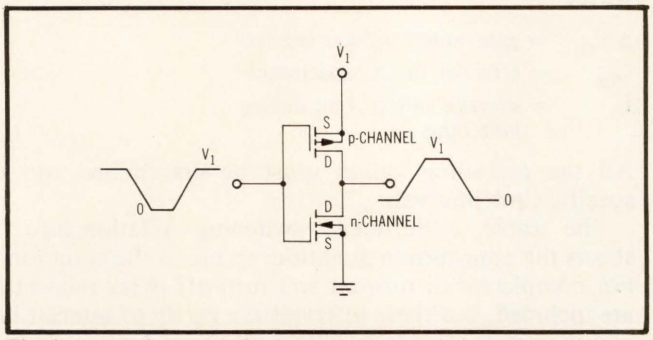


Fig 4 CMOS inverter. P-channel MOSFET is in series with n-channel MOSFET; gates are tied and driven with common signal

Direct current (dc) resistance between drain and source when the device is turned on is generally labeled ON resistance, R_{ON} or $r_{DS(on)}$. However, the CMOS gate has a limited output capability determined by the gain of the n- and p-channel devices.

A look at the characteristic curves of CMOS transistors (Fig 5) will provide insight into the dynamic driving source impedance presented to the VMOS gate. Referring to the curve of V_{GS} = 15 V (gate-to-source voltage) for the n-channel transistor, note that for a constant drive voltage V_{GS}, the transistor behaves like a current source for drain-to-source voltages greater than $[V_{GS} - V_T]$. V_T equals the threshold voltage of an MOS transistor—on the order of 1 or 2 V. For a V_{DS} below $[V_{GS} - V_T]$, the transistor behaves essentially like a resistor. Similar curves are obtained for lower values of V_{GS}, except that the magnitude of the current is significantly smaller and, in fact, I_D increases approximately as the square of increasing V_{GS}. The p-channel transistor exhibits similar, but complementary characteristics with less gain and a more gradual transition from a current source to a resistor.

When CMOS is driving a capacitive load, the initial voltage change across the load will be a ramp due to the current source characteristic, followed by a rounding off due to the resistive characteristic dominating as V_{DS} approaches zero. For fastest turn-on and therefore lower dissipation in the VMOS transistor, the peak output current should be achieved while the CMOS inverter is operating in the constant current mode. To accomplish this, the maximum current from the VMOS is that which corresponds to a V_{GS} that is a few volts below the CMOS supply voltage, V_1. From Fig 5, note that operating the CMOS driver at higher V_{CC} will have a profound effect on VMOS switching speed, because the CMOS output current increases roughly as the square of V_{GS} and the voltage where rounding occurs has been pushed to a higher level.

Therefore, the optimum interface from CMOS to VMOS is shown in Fig 6. In this configuration, the turn-on current is supplied from the p-channel FET that has the poorest characteristics of the CMOS pair, but when operating at 15 V, serious rounding of the VMOS gate waveform can usually be made to occur at a level above that required to handle the load current. The turn-off current is supplied from the n-channel FET; it maintains good drive capability down to the threshold voltage of the VMOS gate, which minimizes tailing of the VMOS drain current.

Driving from TTL logic. Lower logic levels used in TTL make it much less satisfactory than CMOS for direct coupling to VMOS; however, TTL can be directly coupled to VMOS when lower output currents are required, or some additional circuitry is added to make the match more universally applicable. Coupling problems are readily appreciated by analyzing the output circuit of TTL. Fig 7 shows the "totem pole" output circuit configurations commonly used in TTL. When the driver is off, the output is high; however, the output is slightly over two diode drops below the supply voltage for either configuration. Since the nominal supply is 5 V, the output is approximately 3.5 V, a level too low to fully utilize a VMOS transistor.

When the driver is on, the lower output transistor is also on; the output is low, on the order of a few tenths of a volt. In most cases, the low level ensures VMOS cutoff, but the high level needs to be raised.

A method of boosting the TTL output level is shown in Fig 8. The external resistor allows the full supply voltage to be applied to the VMOS gate, but in doing so, the TTL output transistor is cut off as the level increases above 3.5 V. Consequently, the high drive capability and low output impedance of TTL is not effectively utilized, as the drive to the final value of gate voltage must come solely from the pullup resistor. To maintain a reasonably fast rise time, it is necessary to limit the peak drain current to the value obtained for a particular VMOS type when the gate voltage is at 3.5 V; the additional 1.5 V is used as overdrive to place the operating point in the ohmic region.

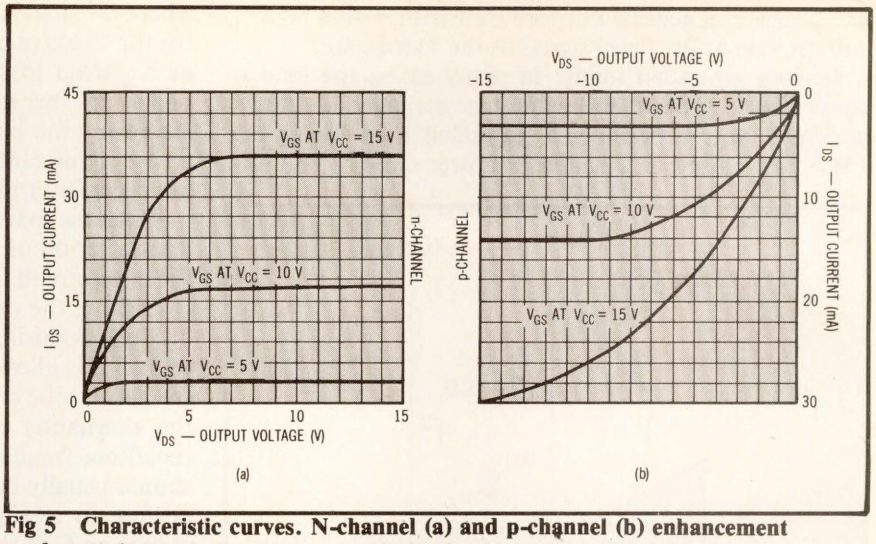


Fig 5 Characteristic curves. N-channel (a) and p-channel (b) enhancement mode transistors shown here are typically found in CMOS circuits

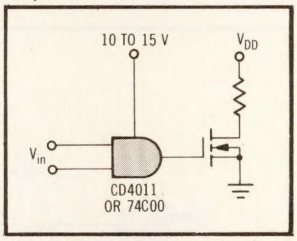


Fig 6 Driving VMOS with CMOS gate. Circuit configuration provides optimum CMOS to VMOS interface

Full utilization of VMOS transistors is achieved with open-collector TTL as shown in Fig 9. The open-collector circuits do not have the top transistors of the totem pole output and the lower transistors are designed to be used with supplies up to 15 V. The VMOS rise time is now mainly dependent upon the external resistor used. For fast rise time, the lower resistance values required may cause objectionable dissipation when the TTL output is low; the circuit in Fig 10 will provide high speed and low dissipation. It essentially restores the totem pole output to the TTL circuit by using an external high voltage transistor. Since the bipolar transistor does

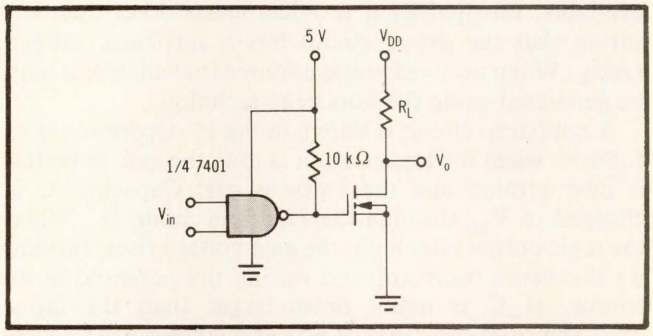


Fig 8 Method for boosting TTL output level. External resistor allows application of full supply voltage to VMOS gate. Fast rise time is maintained by limiting peak drain current

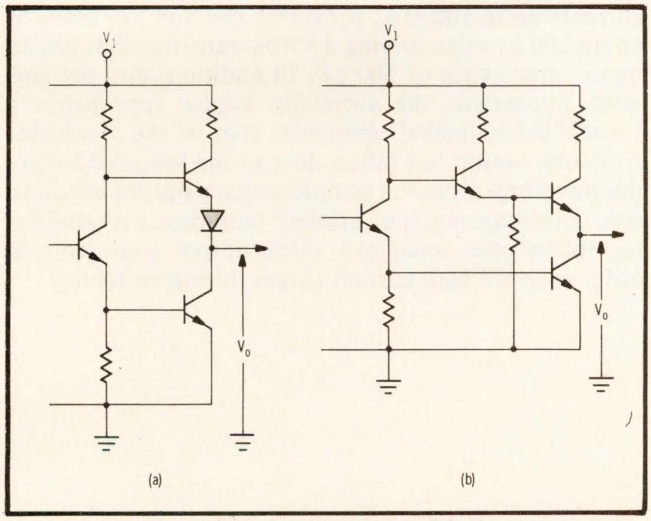


Fig 7 Basic TTL output configurations. Medium speed TTL output structure (a) is typical of 5400/7400 families. For higher speeds (b) is used

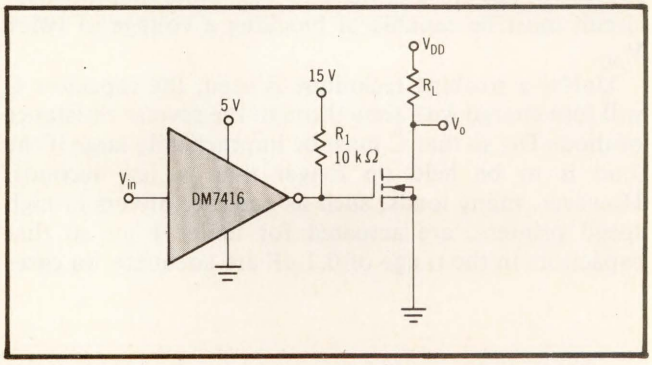


Fig 9 Open-collector TTL provides higher enhancement voltage. VMOS rise time depends chiefly on external resistor

not saturate, a general purpose transistor with a high f_T will provide a fast drive signal to the VMOS gate.

Driving grounded loads. In many cases, the load is connected to ground and cannot be arranged as shown in Figs 1 and 2. Driving a grounded load forces the VMOS to be used in a source follower circuit. The difficulty with a follower is that to keep the VMOS in the ohmic region with a large drain current flow, the gate must be about 10 V above the source potential, which is only slightly lower than the supply. Therefore, the gate drive voltage must come from a voltage source which is about 10 V above the supply voltage. If such a voltage is available, no significant problem exists other than ensuring that the driver circuit has a sufficient voltage rating. When no fixed voltage source is available, it may be generated using the bootstrap technique.

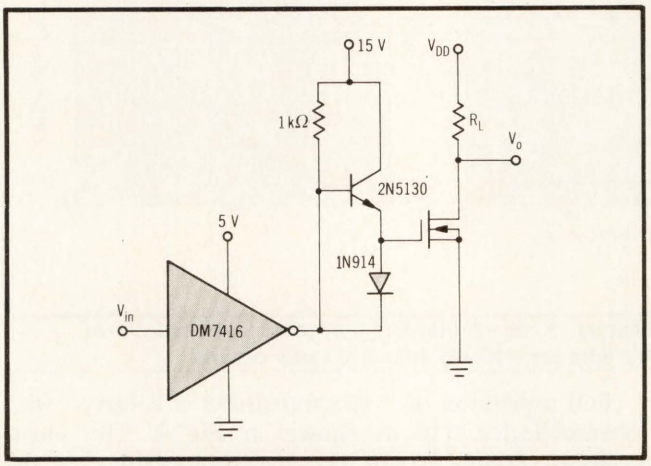


Fig 10 Totem pole driver. Using external high voltage transistor, configuration increases switching speed and reduces dissipation

A bootstrap circuit is shown in Fig 11. Operation is as follows: when the logic output is low, the gate potential is near ground and the VMOS is off. Capacitor C is charged to V_{DD} through the load and diode D_1. When the logic output goes high, the gate voltage rises, turning on the VMOS transistor and raising the potential at its source. If C is many times larger than the input capacitance of the VMOS, it acts as a voltage source having a value close to V_{DD}, which is in series with the VMOS source terminal potential. The resistors couple the capacitor voltage to the gate, thereby providing a gate-source voltage close in value to V_{DD}. Note that the logic circuit must be capable of blocking a voltage of twice V_{DD}.

Unless a strobing technique is used, the capacitor C will lose charge with time through the reverse resistance of diode D_1, so that C must be impractically large if the load is to be held on longer than a few seconds. However, many loads, such as hammer drivers in high speed printers, are actuated for under 1 ms so that capacitors in the range of 0.1 μF are adequate. In cases where the load is a solenoid, it is sometimes permissible for the VMOS to come out of the ohmic region as a result of a partial loss of gate drive after the solenoid has pulled in, because the hold-in current is very low. However, the power dissipation of the VMOS may increase significantly unless the drop in gate drive reduces drain current to a rather low value.

When the load must remain actuated at full power for a long period of time, a pulsed signal can be applied to the drive circuit instead of a dc level. When load current is to flow, the driver is off, except for occasional brief on periods during which the VMOS source voltage drops to ground, allowing C to recharge to V_{DD}. The source for this strobe signal could be a system clock signal or the alternating current (ac) line. The higher the pulse repetition frequency, the smaller C may become, but C should usually be at least ten times the C_{iss} of the VMOS devices to avoid transferring more than 10% of the charge on C to the VMOS gate during turn-on. There is a dearth of logic elements with high enough current capability and blocking voltage to permit the high speed operation possible with the circuit in Fig 11. Consequently, an interface circuit composed of discrete parts, or a special integrated circuit, often must be used.

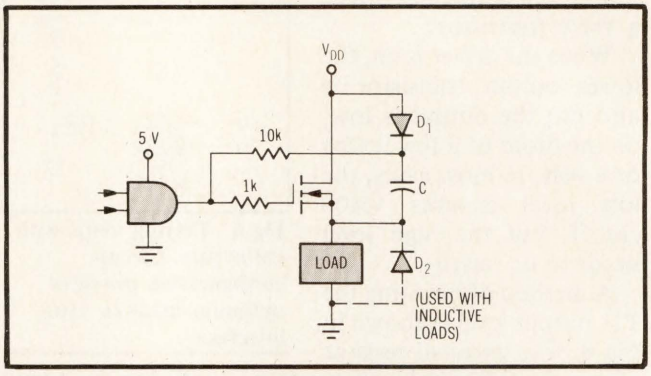


Fig 11 Driving ground connected loads by using bootstrapping. Technique is suitable for discrete devices and IC logic or interface drivers

The D169 interface element is ideal in many applications. It is a dual driver with complementary outputs. It can withstand 36 V, allowing it to be used in a bootstrap circuit operating from a 15-V supply. It can deliver peak currents up to 100 mA, providing rise and fall times of about 100 ns when driving a VMOS transistor that has an input capacitance of 500 pF. In addition, and perhaps most important, the switching action approaches a "break-before-make" sequence; that is, the waveform from one output has fallen close to the low level before the waveform from the complementary output begins to rise. This sequence is of primary importance when driving totem pole connected VMOS output transistors in order to avoid high current surges during switching.

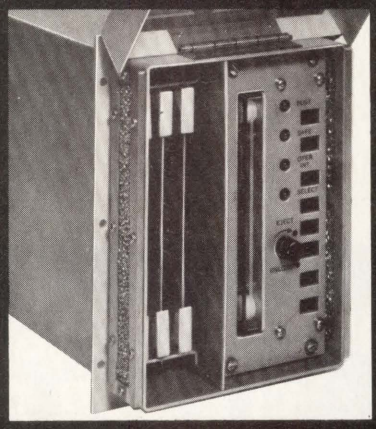
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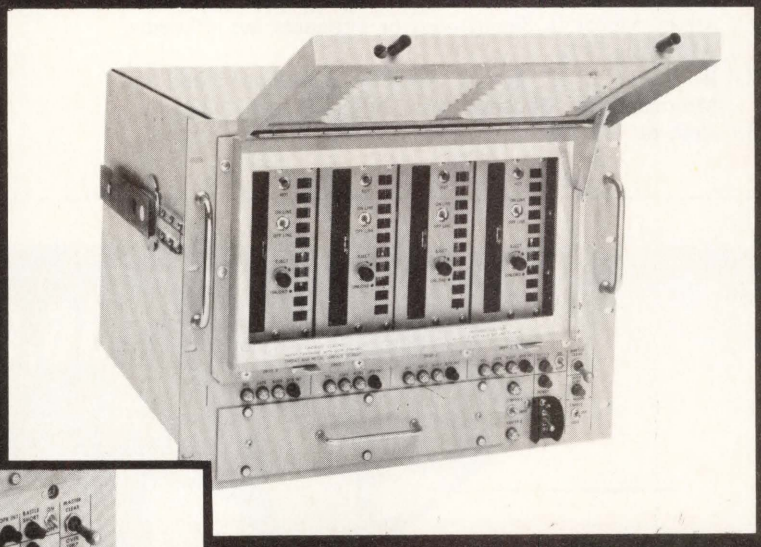
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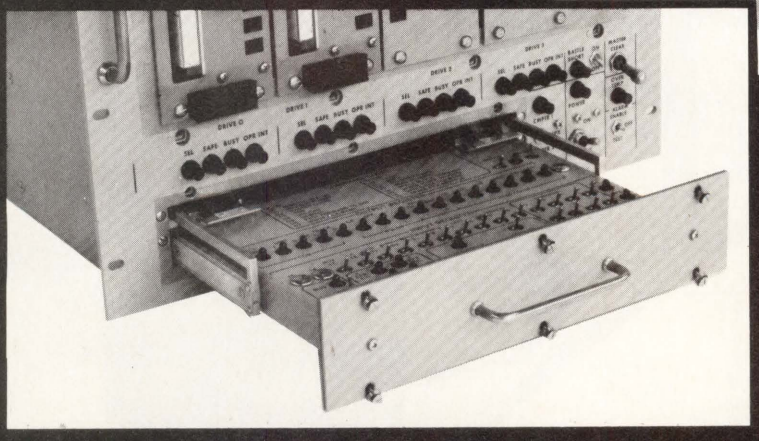
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CIRCLE 135 ON INQUIRY CARD

Summary

VMOS power FETs do easily interface power loads to integrated circuit logic. However, spikes from inductive loads usually must be limited to a level below the breakdown voltage of the VMOS transistor. Also, high inrush, capacitive-like loads usually require high gate drive to rapidly place operation in the ohmic region during inrush.

To avoid deleterious operation and ensure fast switching, consideration must be given to the VMOS input protection Zener diode—if present—and capacitive input impedance. Direct coupling to CMOS is usually satisfactory if the integrated circuit supply is 10 to 15 V. With TTL, open-collector elements are usually required to obtain sufficient gate voltage for the VMOS. Bootstrapping is an effective technique for driving grounded loads, and may be applied to discrete devices, integrated circuit logic elements, or integrated circuit interface drivers.

References

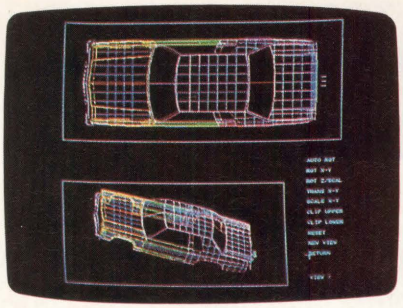
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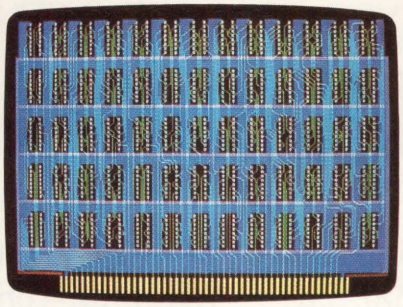
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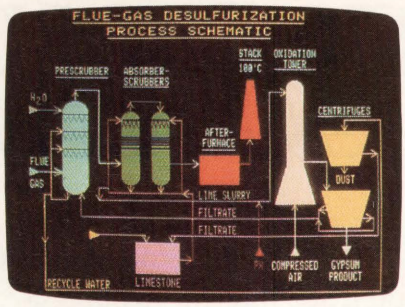
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CIRCLE 136 ON INQUIRY CARD







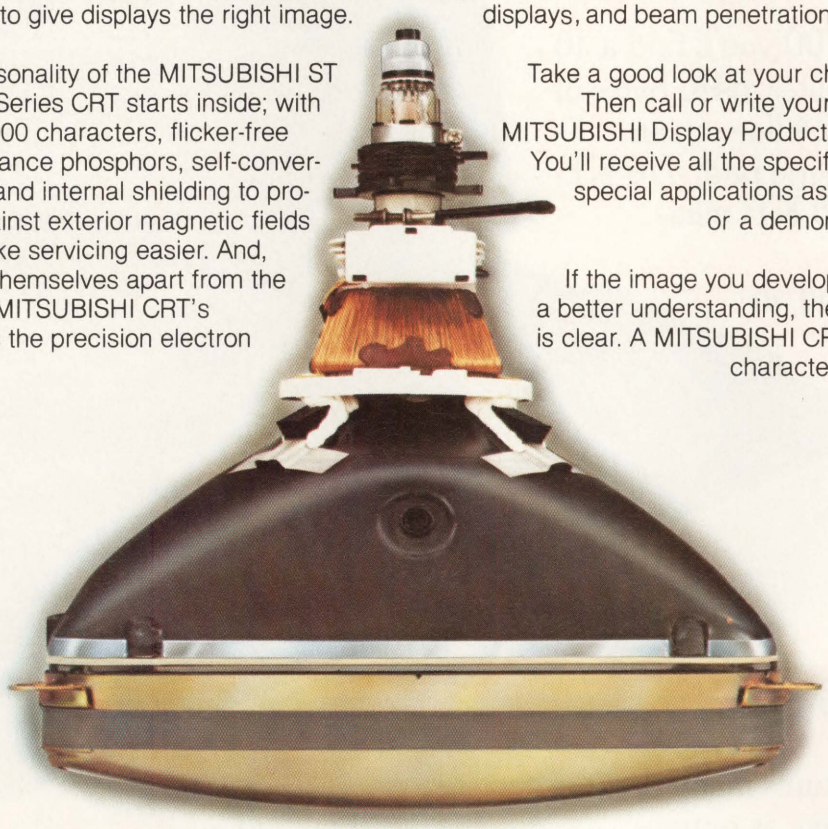
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CIRCLE 139 ON INQUIRY CARD

COMPILER OPTIMIZATION TECHNIQUES

Techniques used within the PL/M-86 compiler make the programmer's job easier while supplying highly efficient code

by Armond Inselberg and Stan Mazor

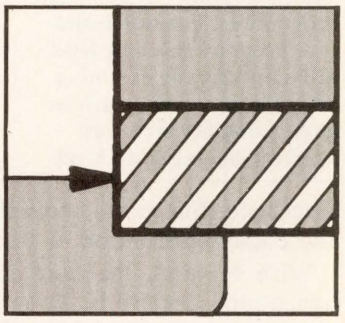
Increasing demands for software development have combined with continuing shortages of programming personnel to create a crisis situation. Shortages of skilled programmers can be partially relieved by careful choice among available programming languages and their compilers. High level languages can make programming easier. Compilers can reduce time spent coding and make up for a shortage of experience by providing the techniques needed to optimize both size and execution speed of machine level code.

What is a compiler?

Software implementation environments can be divided into two levels, as shown in Fig 1: the program machine level and the hardware machine level. Although actual code execution takes place at the hardware machine level, a software engineer cannot efficiently communicate directly with this level. Instead, a programming language, such as PL/M-86, is used as the communication link with the programming machine. The compiler is responsible for translating language input to the programming machine into the language of the hardware machine. In this regard, the maturity of the PL/M-86 compiler as a powerful tool for 8086 software development is revealed.

The compilation process

During the compilation process, the compiler closely binds the input program, determines its syntactic correctness, and generates efficient hardware machine code. Closely binding a program means to fix the types of variables, the forms of the expressions, and the program's structure. To generate efficient hardware machine code, various optimization techniques are used.



The two major steps of the compilation process are the parsing of the input source program and the generation of the output object code. (See Fig 2.) Parsing is achieved by a lexical and syntactic analysis. Lexical analysis separates individual components or tokens making up the program's symbols. These symbols include variable names, key words, and operators. Syntactic analysis checks the program for any syntax errors by determining the structure of the source program in terms of its blocks, statements, and expressions. Results of the parsing are an intermediate text string and a dictionary of variables used in the program.

Generation of the dictionary, or symbol table, is central to the compilation process as it provides a reference for the variable names and their properties. Built during examination of the data declarations, the symbol table is continually referenced during the remainder of the compilation.

The second step of the compilation first performs optimization over the intermediate text, independent of the target hardware. Final object code is then generated, with consideration for hardware machine dependent optimization.

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Armond Inselberg is a senior consultant at the Institute for Software Engineering, Suite 200, 535 Middlefield Rd, Menlo Park, CA 94025. He is involved in data processing capacity management for workload analysis and forecasting. Previously, he worked at Intel, Stanford University, and IBM. He has a PhD in computer science from Washington University and an MBA from the University of Santa Clara.

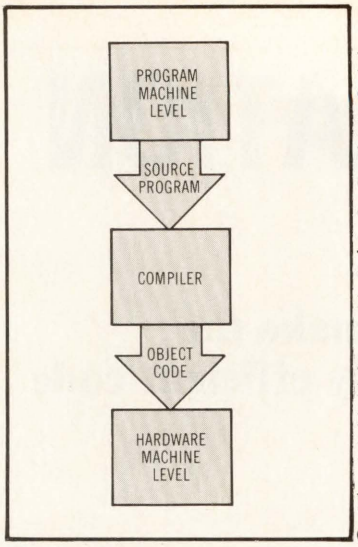


Fig 1 Software implementation environment. Programmer communicates with program machine level, while actual code execution occurs at hardware machine level. Compiler serves as interface between two levels

Optimization philosophy

Efficiency of the generated object code is a primary objective of the compiler. Providing correct code is, of course, the primary objective, but it is never stated explicitly. As with most compilers, the PL/M-86 compiler is geared toward optimizing programs written using good programming practices.

There is a tradeoff between the speed of compilation and the optimization of the resulting object code. Although optimized code is most desirable for finalized production software, the preference during development is for fast compilation. Since a conflict exists between the speed of compilation and code optimization, a compromise must be made.

With PL/M-86, the user can select the level of optimization. Level 0 is the most basic, and level 3, the most advanced. Each successive level provides all optimization techniques of the lower levels, while adding further techniques. If an optimization level is not specified at compile time, the system defaults to level 1.

Specific techniques used within the PL/M-86 compiler serve to optimize the amount of code generated, the execution time of the code, or both the amount of code and the execution time. Hardware machine independent and machine dependent optimization techniques make up a secondary classification of the techniques. Machine independent techniques optimize object code, independent of the target processor. Machine dependent optimization takes advantage of the architecture of the target processor. A third classification is based on whether the techniques optimize over a single program statement or over a range of statements. Table 1 summarizes PL/M-86 optimization techniques for these three classifications.

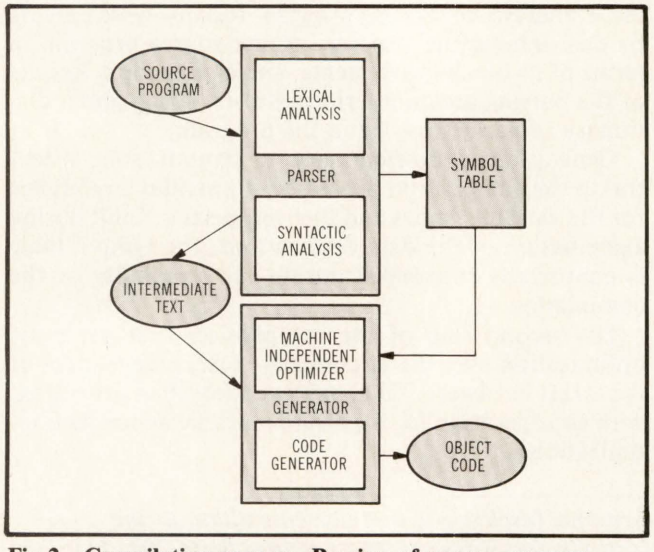


Fig 2 Compilation process. Parsing of source program produces symbol table and intermediate text string. Text string is then optimized, resulting in generation of object code

Amount of code generated

When only a limited amount of memory is available to hold the program, optimizing the amount of code is particularly relevant. Three techniques within the compiler work to reduce the amount of generated code.

Branching to duplicate code—Removing code which occurs more than once, this technique can be used when the paths through duplicate copies of code have the same termination point in the program. In this case, as shown in Fig 3, the second copy of code is replaced with a jump to the original copy.

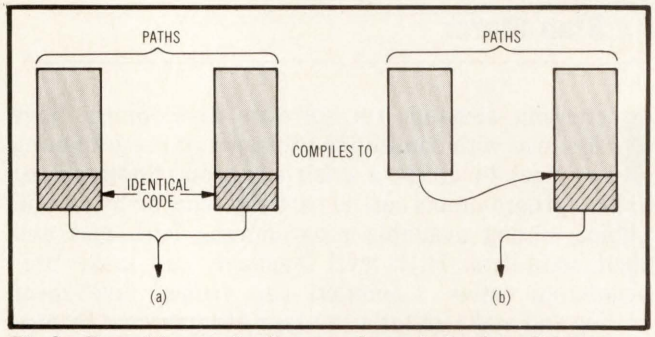


Fig 3 Branching to duplicate code optimization. Both copies of code have same termination point (a); during compilation, second copy of code is replaced by jump to first copy (b)

An example of two program paths that have portions of identical code and terminate at the same point can be found in an IF-THEN-ELSE statement.

```
IF X > Y                                    MOV   AL,Y
   THEN DO;                                 CMP   X,AL
        X=Y;          compiles to           JBE   @1
        X=X+1;                              MOV   X,AL
        END;                          @1:   INC   X
   ELSE X=X+1;
```

In the example, the common program statement X = X + 1; is compiled to INC X and is used by both paths through the compiled IF statement. If X is less than or equal to Y, the JBE (jump below or equal) instruction is executed, causing a jump to the INC instruction. If X is greater than Y, INC is reached even though the JBE is not executed.

Removal of unreachable code—This technique causes the compiler to skip those parts of the program that will never be executed. For example, unlabeled program statements that follow a GOTO statement cannot be reached, and therefore will never be executed. Thus,

```
        GOTO LABELZ;
not      IF X > Y          compiles to   JMP    LABELZ
compiled   THEN X=X+1;                  LABELZ: INC Y
        LABELZ: Y=Y+1;
```

TABLE 1

PL/M-86 Optimization Techniques

	Amount of Code		Execution Speed		Both Amount of Code and Execution Speed	
	Hardware Independent	Hardware Dependent	Hardware Independent	Hardware Dependent	Hardware Independent	Hardware Dependent
Single statement		Instruction size	Strength reduction		Folding of constants	
					Expression arrangement	
					Short circuit of Boolean expressions	
					Function evaluation	
Range of statements	Branching to duplicate code			Address pointer comparison	Elimination of common subexpressions	Peephole
	Removal of unreachable code				Elimination of superfluous branches	Indeterminant storage operations

Although this optimization technique reduces the amount of code generated, it is needed only when the programmer is careless.

Instruction size—The compiler in this case selects the shortest encoding of the instruction. Instructions involving a hardware register can be shortened by one byte if the register is the accumulator. In addition, jumps to locations within 127 bytes require shorter instructions because the increment rather than the target address is specified. For example, if a `JA` conditional jump instruction jumps to a label `@2` that is 14 bytes away, the distance of 14 bytes is stored in the instruction. Thus, the instruction uses one byte to specify an offset rather than four bytes to indicate the target address of `@2`.

```
JA @2          encoded as      7714
                                opcode   offset
```

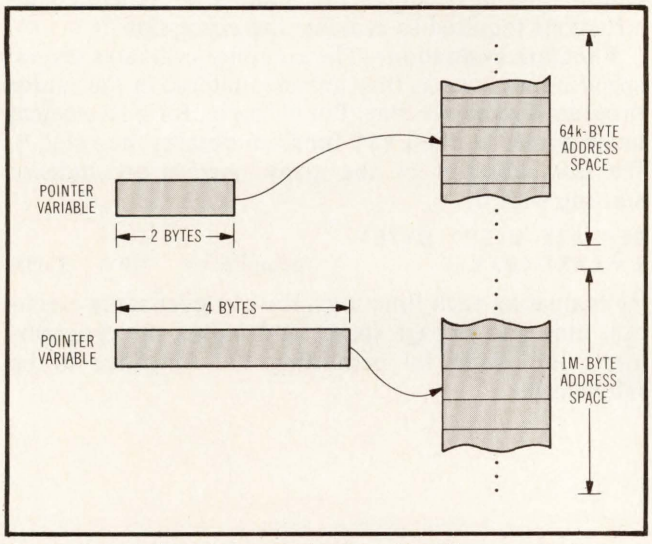


Fig 4 Instruction size optimization. If address space is restricted to 64k (top), compiler allocates 2 bytes for type pointer variable; otherwise, variables require 4 bytes (bottom)

Another aspect of this optimization technique is that the compiler will allocate two bytes to variables declared to be of type pointer, if the address spaces for code and data are restricted to 64k bytes each. Otherwise, as shown in Fig 4, variables of type pointer require four bytes. The programmer indicates the size of the address space to the compiler through a compiler control switch.

Execution speed

Optimizing the execution speed can be critical for time-dependent processing. Two optimization techniques available for improving execution speed are strength reduction and address pointer comparison.

Strength reduction—Execution is optimized by replacing certain operations with faster executing operations. For example, the compiler replaces "multiply a variable `Y` by two" with a shift left operation. The result is the same, but a shift left executes faster than a multiply.

```
X = Y*2;        compiles to     MOV  AL,Y
                                SHL  AL,1
                                MOV  X,AL
```

Address pointer comparison—This optimization technique generates code to compare two 32-bit pointer variables. Physical addresses are actually 20 bits, but are stored as a 16-bit base and a 16-bit offset field. When the base is shifted left by 4 bits and added to the offset, it yields a 20-bit address (Fig 5). Execution speed is improved because, instead of calculating the 20-bit address to compare pointers, code is generated to first compare the base parts. Only if the base parts are equal is it necessary to compare the offset parts.

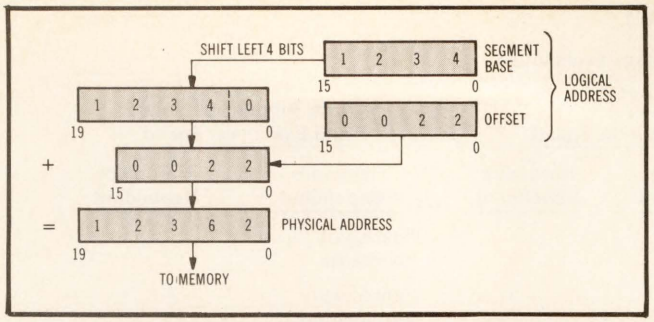


Fig 5 Address pointer comparison. 32-bit pointer variables are stored as 16-bit base and 16-bit offset. Shifting base left 4 bits and adding it to offset results in 20-bit address

For example, two variables, PTR1 and PTR2, are declared to be of type pointer. If PTR1 is greater than PTR2, then X is set equal to 0.

```
DECLARE (PTR1,PTR2) POINTER;
IF PTR1 > PTR2
 THEN X=0;          compiles to     LES   AX,PTR1
                                    PUSH  ES
                                    LES   DX,PTR2
                                    MOV   DI,ES
                                    POP   SI
                                    CMP   SI,DI
                                    JNE   $+4H
                                    CMP   AX,DX
                                    JBE   @1
                                    MOV   X,0H
                               @1:
```

In this example, the LES instruction loads the AX register with the offset of PTR1. The base is loaded into the ES register, then moved to the SI register by means of the stack. The offset of PTR2 is loaded into the DX register and the base is moved to the DI register. The two base values in the SI and DI registers are compared by the CMP instruction. If the results are not equal, the JNE instruction (jump not equal) is executed, skipping the code used to compare the offsets, and jumping to the instruction that sets X to 0.

When only a limited amount of memory is available to hold the program, optimizing the amount of code is particularly relevant.

Optimizing both amount of code and execution speed

Most optimization techniques reduce the amount of generated code and improve execution speed. Eight techniques accomplish this within the PL/M-86 compiler.

Folding of constants—This technique causes the compiler to perform arithmetic operations at compile time rather than at execution time. For example, a statement with the expression 6 + 3 + W would be coded as 9 + W. Thus,

```
V = 6+3+W;          compiles to     MOV   AL,W
                                    ADD   AL,9H
                                    MOV   V,AL
```

Expression arrangement—Code for expression evaluation is generated such that the operations are performed in that order which produces the most efficient code. If expressions I times J and K times L are to be calculated, and their results subtracted, then

```
Z = (I*J) - (K*L);    compiles to   MOV   AL,J
                                    MUL   I
                                    PUSH  AX
                                    MOV   AL,L
                                    MUL   K
                                    POP   CX
                                    SUB   CX,AX
                                    MOV   Z,CL
```

In this example, the result of I * J is pushed onto the stack, freeing the accumulator for a second multiply. After K * L is evaluated, the result of I * J is popped into the CX register. The registers are then subtracted. This process is much more efficient than having the compiler first save the two multiplication results in temporary variables, then move these results to registers, and finally subtract the registers.

Short circuit of Boolean expressions—Generated code terminates the evaluation of a Boolean expression as soon as its outcome is established. For example, consider the expression (V>X AND I>J). If V is not greater than X, the expression will be false, regardless of the results of the rest of the expression; therefore, the remainder of the expression need not be evaluated. Thus,

```
IF (V > X AND I > J)   compiles to   MOV   AL,V
   THEN B=1;                         CMP   AL,X
                                     JBE   @1
                                     MOV   AL,I
                                     CMP   AL,J
                                     JBE   @1
                                     MOV   B,1H
                                @1:
```

In this example, the generated code tests V for greater than X. If this comparison is false, the JBE (jump on below or equal) to label @1 is executed. This label is generated by the compiler to go around the IF statement without executing the remaining code of the Boolean expression. This technique not only saves execution time but reduces the number of generated instructions required to evaluate the expression.

Function evaluation—The compiler evaluates several specific functions as they are encountered in the source program at compile time. For example, for a 10-element array named W, the LAST function obtains the value 9, the last subscript of the array. Arrays are indexed starting with 0.

```
DECLARE W(10) BYTE;
I = LAST (W);              compiles to   MOV   I,9H
```

By evaluating such functions, the compiler saves execution time and storage space, and makes the programmer's job easier by permitting the functions to be referenced.

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Elimination of common subexpressions—The compiler recognizes multiple occurrences of an expression and saves the value of the expression in a register or stack so that it need not be recalculated. For example, the expression J + I or I + J may occur several times but will be evaluated only once.

```
X = J + I;          compiles to     MOV  AL,J
Y = I + J;                          ADD  AL,I
                                    MOV  X,AL
                                    MOV  Y,AL
```

By saving the result of J + I in the AL register, rather than recalculating each time it is encountered, generated object code and execution time are greatly reduced.

Optimizing the execution speed can be critical for time-dependent processing.

Elimination of superfluous branches—Optimization using this technique reduces the number of jumps that must be executed. In the first example, jumping to a LABELX that contains a jump to LABELZ transforms the first jump into a branch directly to LABELZ.

```
IF X > Y                        compiles to     MOV AL,X
   THEN GOTO LABELX;                            CMP AL,Y
                                                JA  LABELZ
          .                                       .
          .                                       .
          .                                       .
LABELX: GOTO LABELZ;                    LABELX: JMP LABELZ
          .                                       .
          .                                       .
          .                                       .
LABELZ:                                 LABELZ:
```

Another example is the selection of a single conditional jump instruction based on the result of a comparison. This optimization can occur frequently, eliminating an unconditional JMP instruction each time through the selection of the appropriate conditional jump. Consider the IF statement that executes some code only if X > Y.

```
IF X > Y                compiles to         MOV AL,X
   THEN DO;                                 CMP AL,Y
        Z=R;                                JBE @1   ]
        R=R+1;                              MOV AL,R
      END;                                  MOV Z,AL
                                            INC R
                                        @1
                                            MOV AL,X
                                            CMP AL,Y
                        compiles to         JA  $+5H ]
                        without use of      JMP @1   ]
                        optimization        MOV AL,R
                        technique           MOV Z,AL
                                            INC R
                                        @1:
```

In this example, the JA (jump above) and JMP (unconditional jump) instructions are replaced by a single JBE (jump below or equal) instruction.

Peephole—This optimization attempts to discard redundant instructions. One such action might be loading a register with a value that it contains already. For example, if Y is set equal to X + 1, the value of Y is currently in the accumulators since it was last used to calculate X + 1. If Y is again used in the next statement, there is no need to fetch the value of Y. Thus,

```
Y=X+1;          compiles to     MOV  AL,X
Z=W+Y;                          INC  AL
                                MOV  Y,AL
                                ADD  AL,W
                                MOV  Z,AL
```

Since the value of Y is currently in the accumulator as a result of the calculation of X + 1, it need not be reloaded into the accumulator for the calculation of W + Y.

Indeterminant storage operation—The compiler does not reload the starting point of a based data structure each time that it is referenced. For example, consider PART to be an array of structure elements based by the pointer variable PARTPTR.

```
DECLARE PART BASED PARTPTR (10)
 STRUCTURE (PARTNO WORD,
            AMT    BYTE,
            COST   WORD);

PART(2).PARTNO=6C4H;    compiles to     MOV  BX,PARTPTR
PART(6).AMT=79H;                        MOV  PART[BX,0AH],6C4H
                                        MOV  [BX+20H],79H
```

The first reference to the array structure places the base of the array, contained in PARTPTR, in the BX register. Further references to the array structure do not require that the BX register be reloaded.

Evaluation examples

PL/M-86 offers four levels of optimization. Optimization techniques provided at each of these levels are classified in Table 2. To indicate how much storage is actually

TABLE 2

Optimization Techniques Provided In Each Compiler Level

Optimization Technique	Optimization Level			
	0	1	2	3
Folding of constants	X	X	X	X
Expression arrangement	X	X	X	X
Short circuit of Boolean expression	X	X	X	X
Function evaluation	X	X	X	X
Strength reduction		X	X	X
Elimination of common subexpressions		X	X	X
Elimination of superfluous branches			X	X
Removal of unreachable code			X	X
Branching to duplicate code			X	X
Instruction size			X	X
Peephole			X	X
Indeterminant storage operations				X
Address pointer comparisons				X

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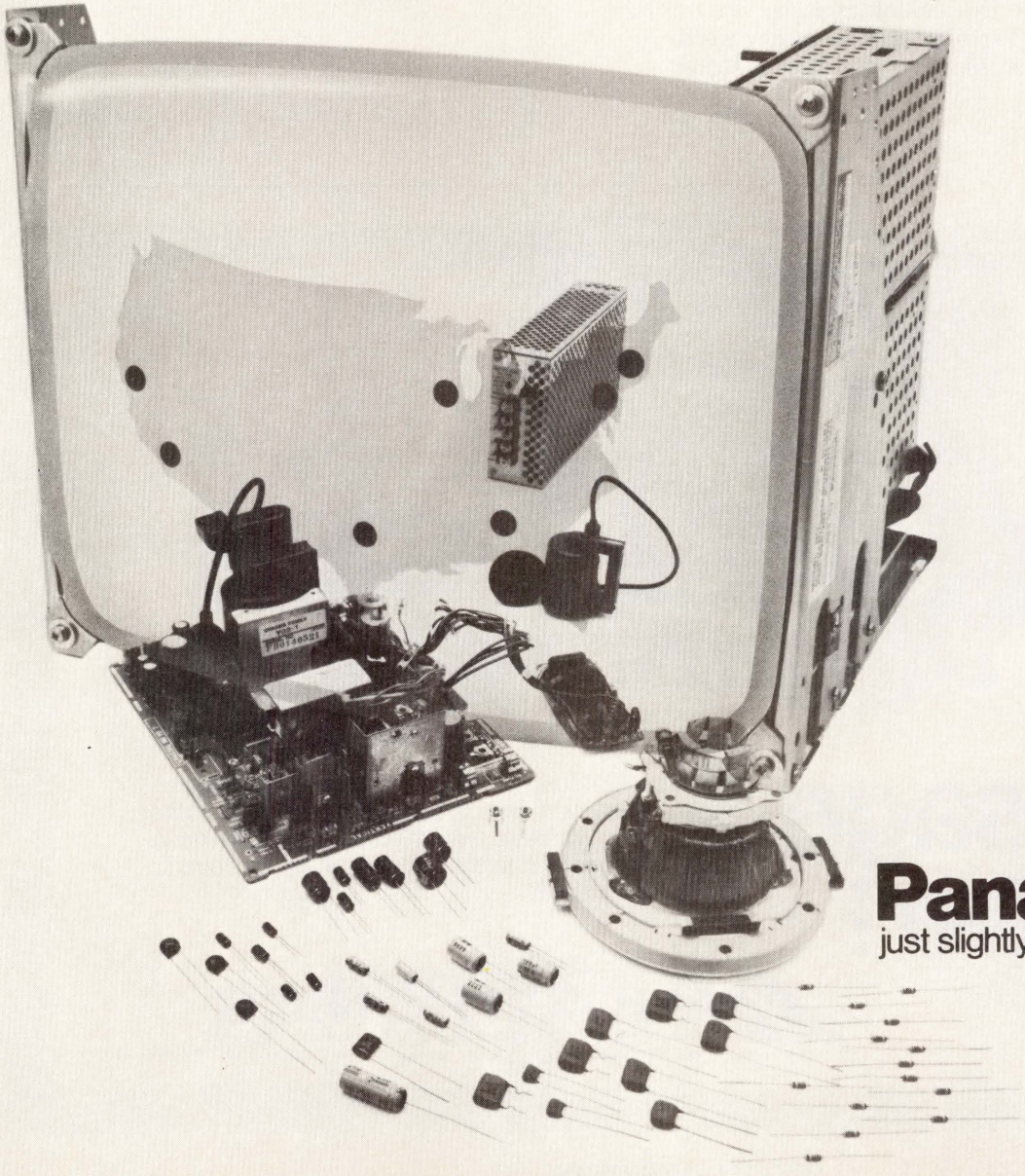
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TABLE 3

Object Code (bytes) Generated For Each Optimization Level

	Level 0	Level 1	Level 2	Level 3
Program A: Mastermind	1688	1559	1450	1450
Program B: General sort	1953	1789	1503	1503
Program C: Frequency count	849	765	694	694
Program D: Process simulation	7955	7951	7083	7083
Program E: Service queue	289	250	212	185
Average % size reduction from previous level		7.9%	12.28%	2.55%

saved by these techniques, five sample programs were compiled at each level using version 2.1 of the compiler; Table 3 provides the size in bytes of resulting compilations. The reduction in size obtained in going from one level to the next higher level is due to the additional optimization techniques used at the higher level.

Programs used in this study demonstrate the compiler's ability to optimize various types of instructions. Program A plays the game of mastermind with the operator performing a large amount of input/output with the cathode ray tube. Program B performs a sort on an array of 1000 records, making extensive use of structures and pointers. Performing a frequency word count on an arbitrary text file, Program C uses string move instructions and pointers. Program D uses simple coding with no structures or pointer addressing to perform a process simulation. Service queue simulation using linked data structures is done in Program E.

For each successive level of optimization, the individual percentages in size reduction of the programs were averaged. From Table 3, it becomes apparent that Level 3 optimization provides nearly a 25% reduction in storage requirements.

Conclusion

As the demand for microprocessor software increases, the selection of the implementation language will receive more attention. In choosing a language, users must consider not only high level constructs of the language itself, but also the capabilities of available compilers to translate the resulting programs.

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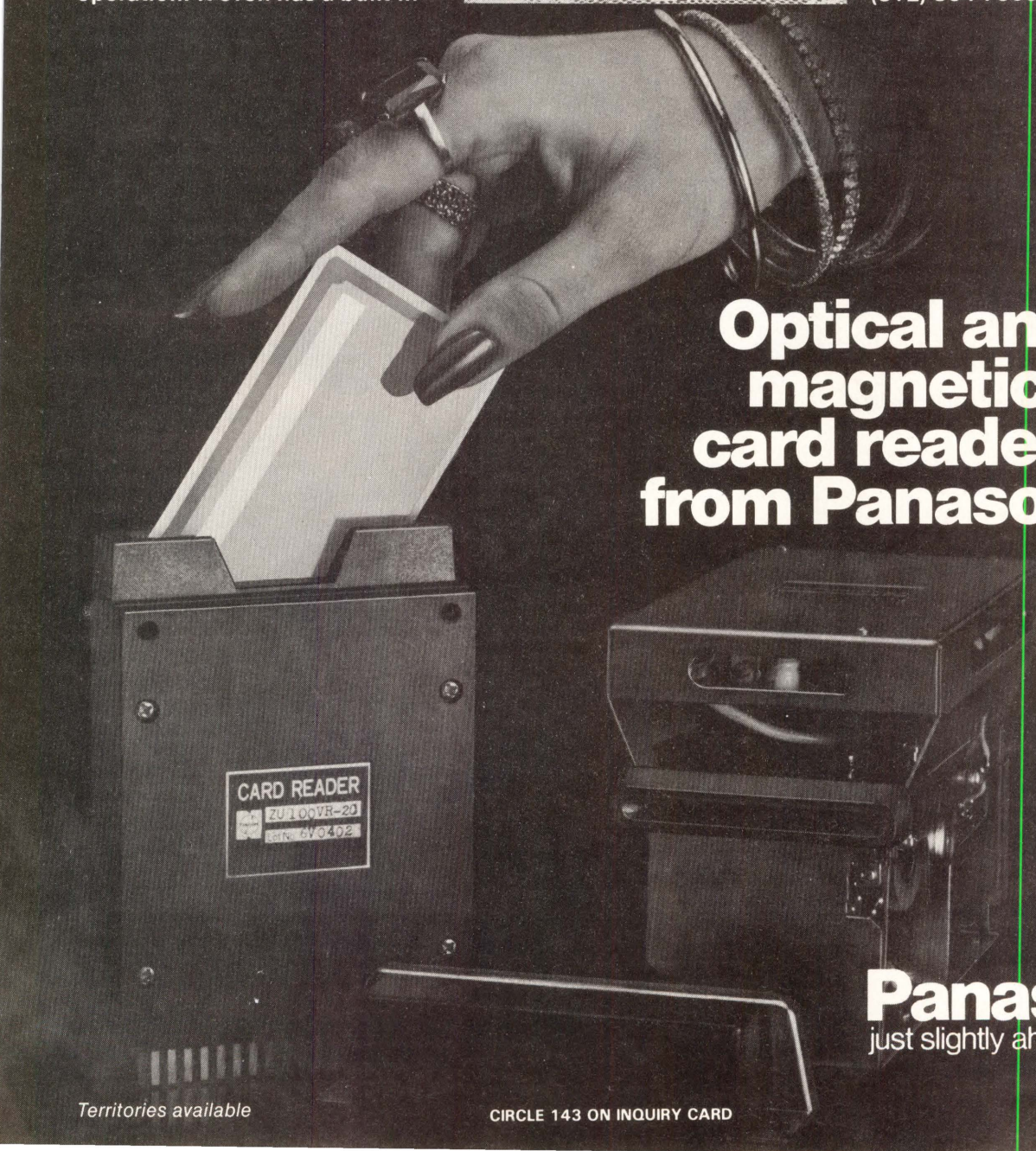
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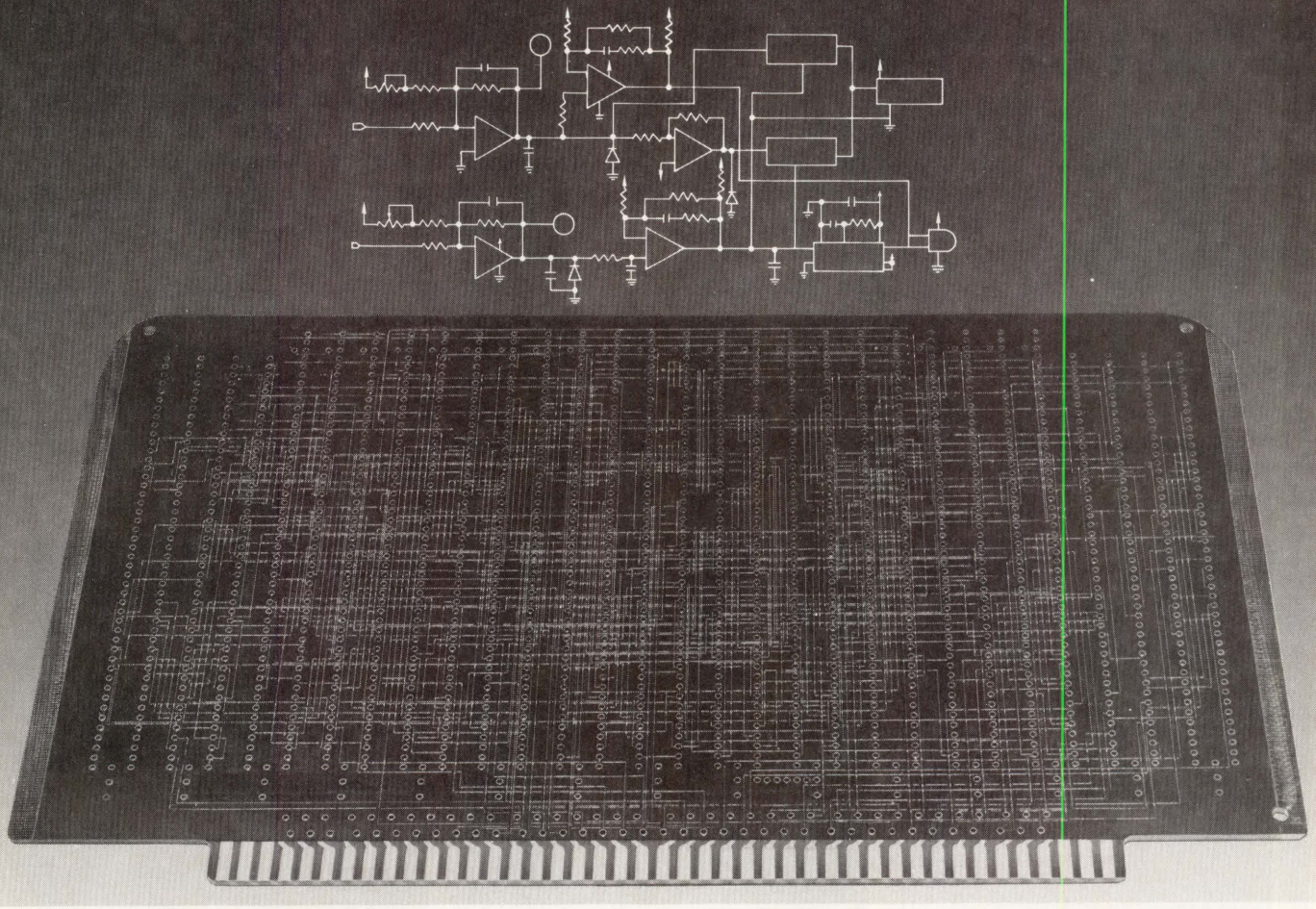
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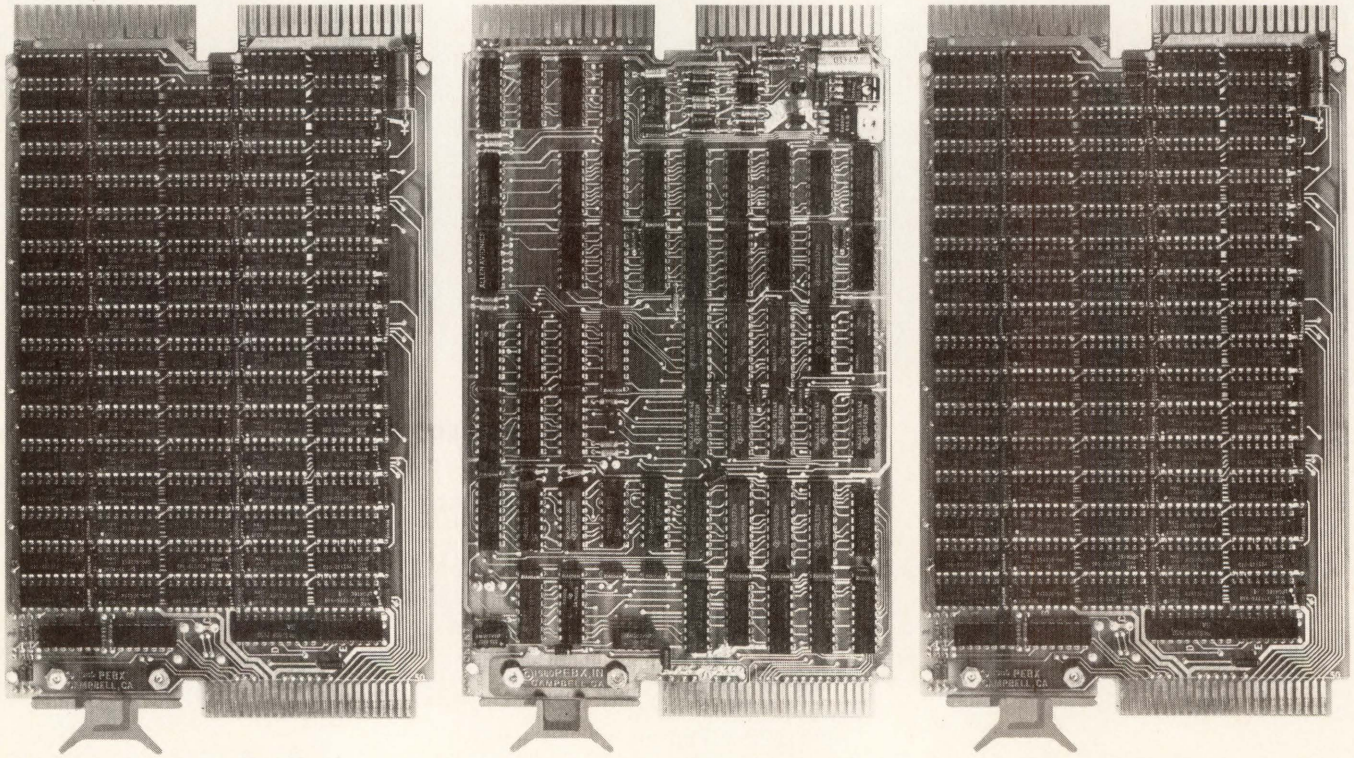
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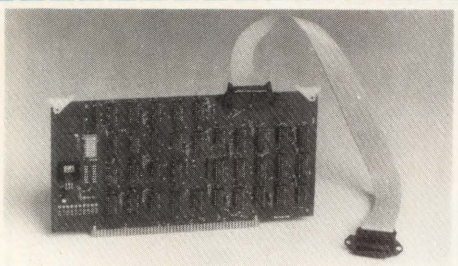
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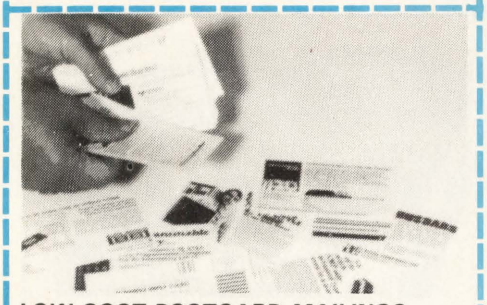
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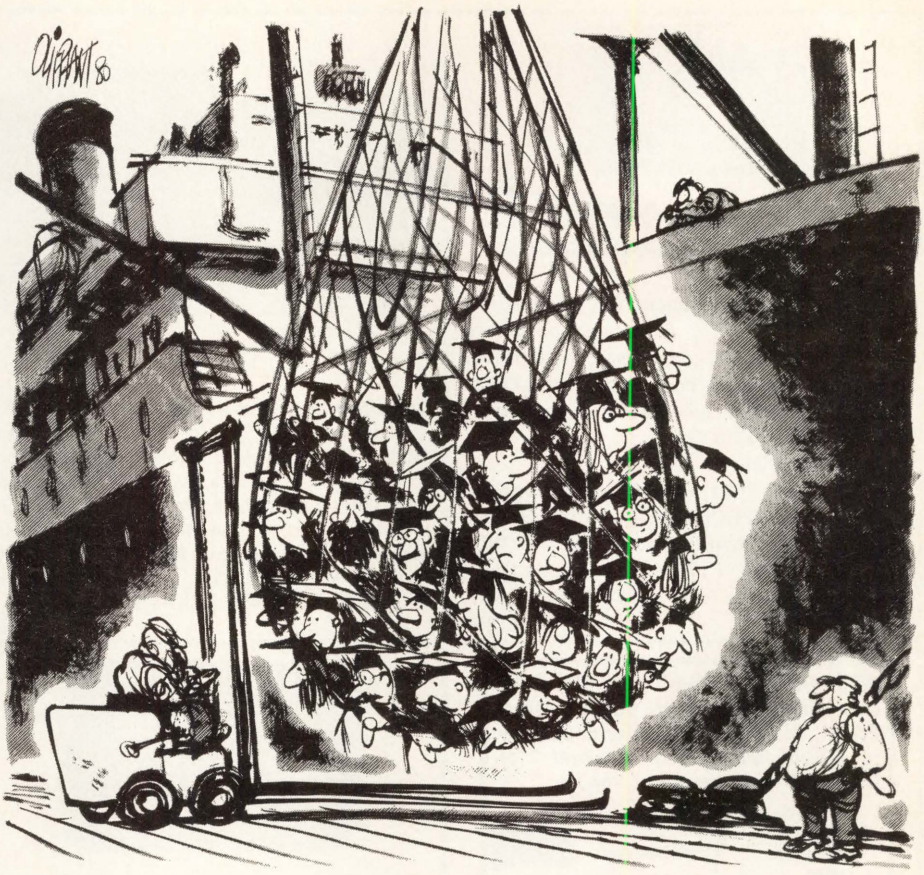


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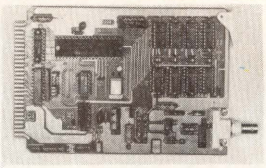
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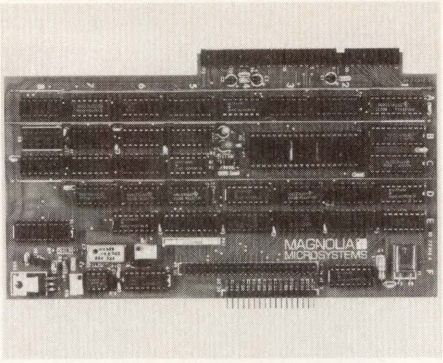
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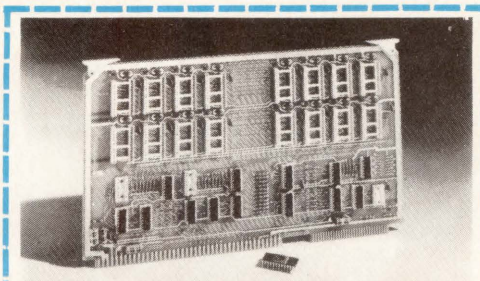
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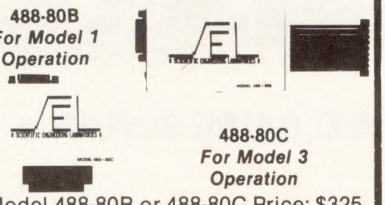
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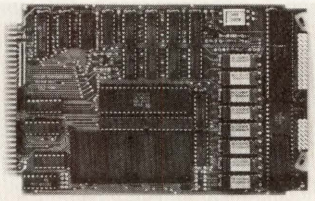
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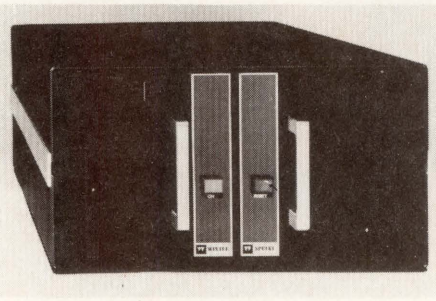
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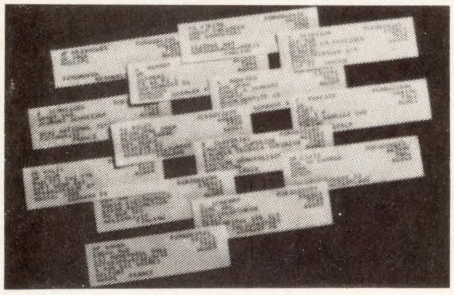


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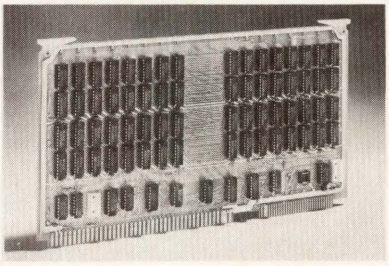
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4 AND 8k RAM BOARDS ARE MULTIBUS COMPATIBLE

Multibus: Intel trademark

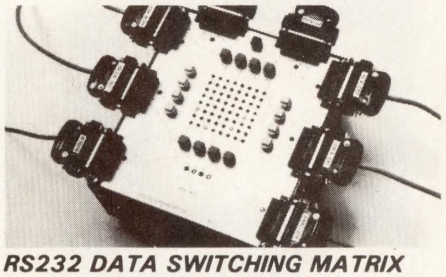
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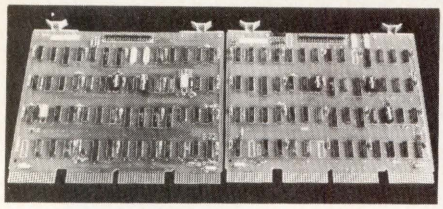


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- Implements every possible connection between Tx Data and Rcvd Data for eight I/O ports.
- Manual Control and connection monitoring via built in key array and 8 x 8 LED display.
- Non-volatile memory for 16 connection arrangements.
- 20 ma, RS232, or TTL may be mixed.
- Remote selection via parallel TTL interface.

$995 (1-4, USA only), **DIGITAL LABORATORIES**,600 Pleasant St., Watertown, MA 02172. (617)924-1680.

CIRCLE 401



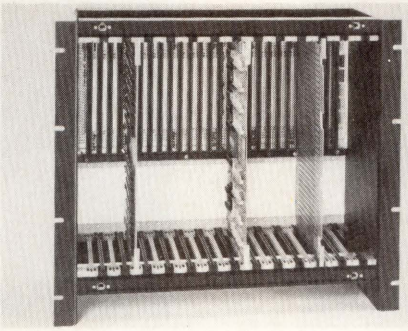
New DEC-compatible shared memory link obsoletes traditional CPU links.

The PPL-1 Peripheral Processor Link is a unique shared memory interface between any two Q-bus (LSI-11) and/or Unibus (PDP-11)-based DEC CPU's. Two quad boards and a connecting cable link the peripheral unit with the host. Up to 32KB of memory can be accessed by the peripheral processor in 4KB boundaries anywhere in the address space of the host. Address spaces are 18 bits for Unibus and 22 bits for the Q-bus. This memory sharing does not require software to support the link. 16 vectored interrupts (8 from each direction) provide necessary hardware for protocol implementation.

DEC, LSI-11, PDP-11 Q-bus and Unibus are registered trademarks of Digital Equipment Corp

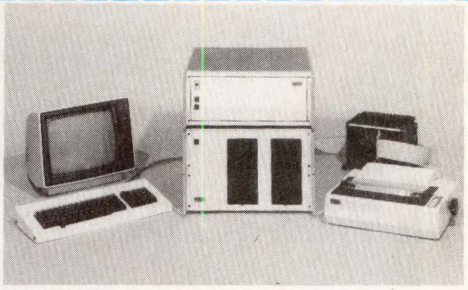
RANYAN Computer Enhancement Systems
Box 790 • Huntington Beach, CA 92648 • 714-536-0646

CIRCLE 402



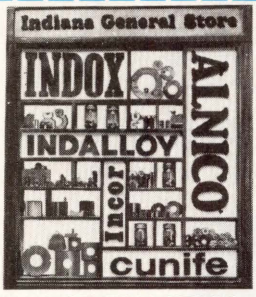
RACK MOUNT MULTIBUS™ CAGES

Now you can assemble Multibus systems for rack mounting applications with a minimum of mechanical design effort. The 15.75" high units are available with up to 26 card slots complete with backplane and power supply connections. Multibus™ Intel Corporation. **ELECTRONIC SOLUTIONS**, 5780 Chesapeake Ct, San Diego, CA 92123. Toll Free: (800)-854-7086. In Calif. (714) 292-0242. **CIRCLE 405**



STD BUS MICRO COMPUTER DEVELOPMENT SYSTEM

The BASIS/80 MDS features: MEMORY MAPPED CRT, CPM operating system, STD BUS hardware, SCREEN BASED EDITOR, BASIC, FORTRAN, PASCAL, FORTH and other languages for 8080, Z80, 8085, 8088, and other CPU's WITH IN-BUS EMULATION with direct connection to users target STD BUS prototype system for SYMBOLIC debugging, downloading, TRACING, SINGLE-STEP execution and memory display. Typical MDS $7,500. ***ANTONA CORPORATION***, 13600 VENTURA BLVD, SHERMAN OAKS, CA 91423. Tel: (213) 986-6651. **CIRCLE 408**



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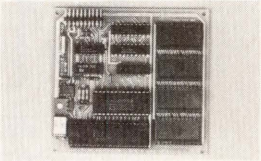
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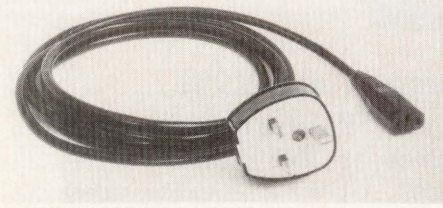
CIRCLE 406



M410 VOICE RESPONSE MODULE

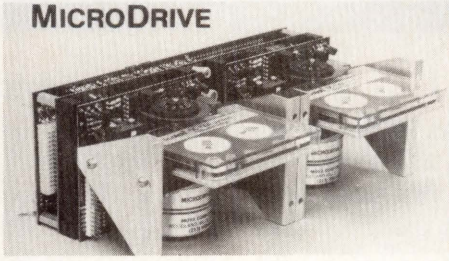
Versatile speech module provides high-quality synthesized speech with vocabularies up to 120 words selected by user from extensive standard vocabulary list. Single +5 v supply, 0.2 watt speaker output, size 4 by 3.75 inches. Easy to apply. Message selection by 8-bit parallel code. Internal FIFO buffer stores sequences up to 54 words and phrases. Special code starts and stops speech output. Single unit with basic 24-word vocabulary is $185. EPROMs coded with selected vocabularies can be added later. Custom speech coding available. Bus-level products also manufactured. **SPEECH TECHNOLOGY CORPORATION**, 631 Wilshire Blvd, Santa Monica, CA 90401. Tel: (213) 393-0101.

CIRCLE 409



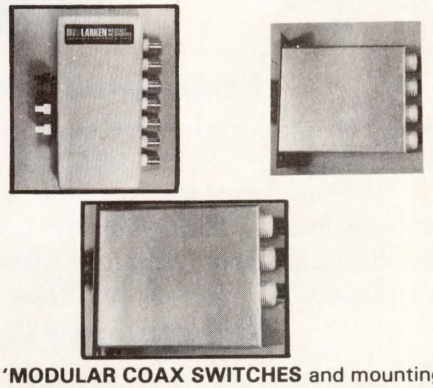
INTERNATIONAL CORDS AND CORDSETS

Standard cords for use in European countries, Australia, U.S. and Canada are available from stock or with shorter delivery times than custom cords. Cords have approvals at VDE, SEV, SEMKO, and other national test agencies as well as CSA certification and UL listings. Power supply cords can be installed permanently; cordsets with CEE-22 connector are detachable. Bulk cordage is available in sizes 3 x 0.75 mm², 3 x 1.0 mm², and 3 x 1.5 mm². **PANEL COMPONENTS CORP.**, P.O. Box 6626, Santa Rosa, CA 95406. Tel: (707) 523-0600. **CIRCLE 404**

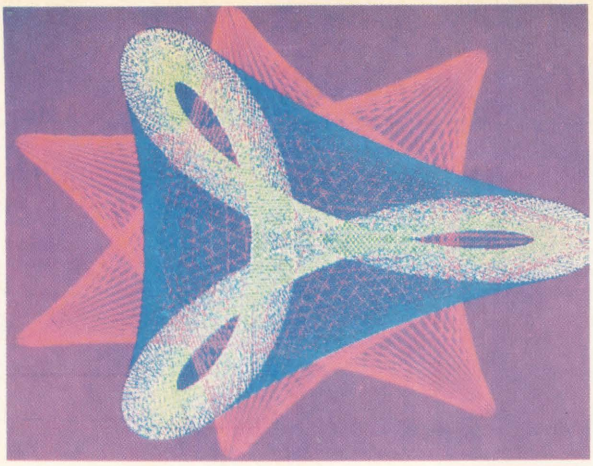


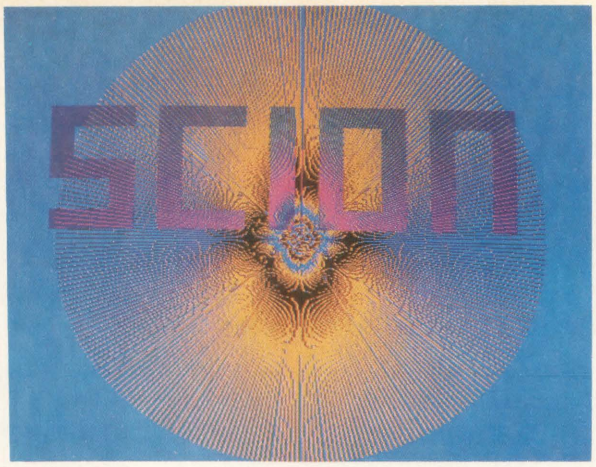
MicroDrive (TM) TAPE CARTRIDGE DRIVE SYSTEMS DESIGNED FOR OEM'S

Rugged, all metal, patented main plate assures precise head to tape interface for DC100A cartridge interchange. Compact units (2 Drives) with control and formatting circuits use only 8" by 3" of panel space. RS-232 and parallel I/O are available. Modular design allows distributed packaging in tight terminal applications. Call or write for OEM pricing and full specs. **MOYA CORPORATION** 9001 Oso Ave, Unit B, Chatsworth, CA.91311. Tel: (213)700-1200 **CIRCLE 407**

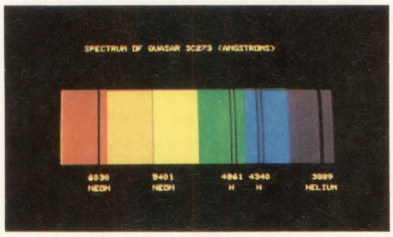


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BYTE, Product Review



"...better monochromatic ...display...."
ELECTRONIC DESIGN, 1981 Technology Forecast

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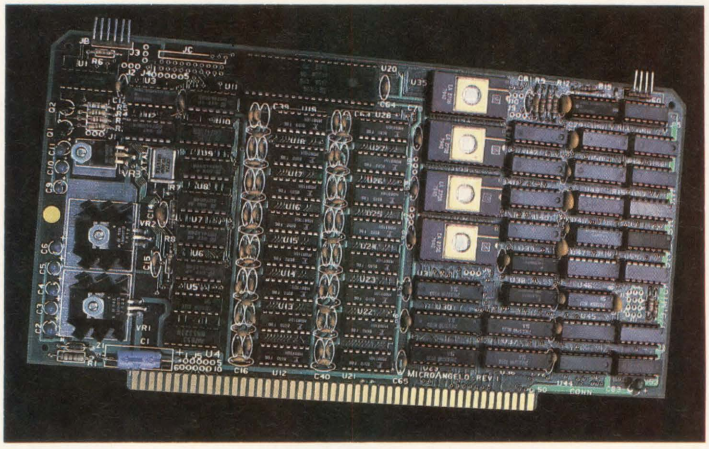
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IEEE S100 bus compatible



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4K resident Screenware™ Pak I operating system

32K RAM isolated from host address space

High speed communications over parallel bus ports

Screenware™ Pak I

A 4K byte operating system resident in PROM on MicroAngelo™. Pak I emulates an 85 character by 40 line graphics terminal and provides over 40 graphics commands. Provisions exist for user defined character sets and directly callable user extensions to Screenware™ Pak I.

Screenware™ Pak II

An optional software superset of Pak I which adds circle generation, polygon flood, programmable split screen for separate graphics and terminal I/O, relative coordinates, faster vector and character plotting, a macro facility, full UCSD Pascal compatibility, and more.

And now...COLOR!!

The new MicroAngelo™ Palette board treats from 2 to 8 MicroAngelos as "bit planes" at a full 512 x 480 resolution. Up to 256 colors may be chosen from 16.8 million through the programmable color lookup table. Overlays, bit plane precedence, fade-in, fade-out, gray levels, blinking bit plane, and a highly visual color editor are standard.

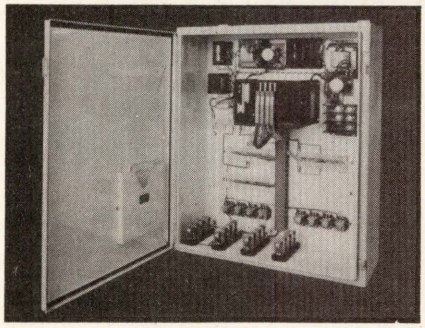
SCION

12310 Pinecrest Road • Reston, VA 22091 • (703) 476-6100 • TWX: 710-833-0684

CIRCLE 149 ON INQUIRY CARD

CONTROL & AUTOMATION

Industrial control units function remotely in distributed systems



Fully-configured, packaged industrial control units in LINK/130 line typically function as remotes in a distributed system that interfaces to analog and discrete process sensors and control points; collects, checks, and analyzes process data; telemeters process data and control information to other units; and implements process control actions. Each unit monitors and controls up to 144 data points.

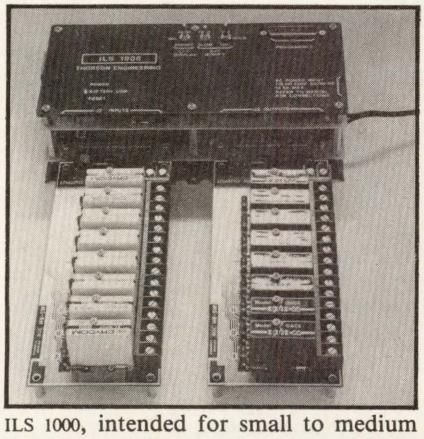
Units consist of a 16-bit microprocessor, 24k bytes of RAM, 48k bytes of P/ROM, interface, process data interface boards, card chassis, process data cables, terminal connection blocks, output relays, a NEMA-12 enclosure, and data acquisition and supervisory control software. Nine card slots are available for various analog and discrete process interface boards.

Implemented on a single PCB, the units' 8086 processor system includes a communication port for SDLC transmission in network applications. Each unit includes the company's EXEK realtime operating system and ACCESS monitoring and control applications software package that performs point scans, data processing, alarm checking, network communication, and control output functions. For many applications, no additional software is required.

Units have op temp range of 0 to 50 °C, measure 36 x 30 x 12″ (91 x 76 x 30 cm), and meet IEEE-472 std for surge withstand capability for all connectors outside the enclosure. Terminal connector blocks that accommodate industrial wire sizes, std output relays, and excitation source for contact inputs aid in installation. **Modular Integration, Inc,** PO Box 1079, Issaquah, WA 98027.

Circle 269 on Inquiry Card

Solid state programmable controller



ILS 1000, intended for small to medium size industrial logic systems, replaces complex relay logic systems. CMOS logic provides high noise immunity, while industry std solid state relays simplify interfacing and maintenance. The unit features an op temp range of −30 to 60 °C; 1024-byte program memory of battery backup RAM, EEPROM, or UV EPROM; 50 timers, counters, shift registers, or state sequencers; up to 32 inputs and 32 outputs; 192 internal control variables; std Opto 22 style I/O modules; and a dedicated display for preset and current value of timers/counters. **Thorson Engineering Co,** 6225 76th St SE, Snohomish, WA 98290.

Circle 270 on Inquiry Card

Microprocessor based direct digital control system

Model W-8010 operates as standalone control system for municipal or industrial processes and can be configured as an intelligent remote processor in a distributed processing configuration. Housed in std cardbox assembly, system includes solid state power supply module, 8085 CPU module with 6k words of EPROM, and 2.25k words of RAM. Realtime multitasking programs provide executive control over 8 simultaneously running programs. **Aquatrol Corp,** 2258 Terminal Rd, St Paul, MN 55113.

Circle 271 on Inquiry Card

2-axis computer controlled positioning system

Microdex II offers a direct interface to an IEEE-488 bus that accepts ASCII data with RS-274 format, provides manual run and step with full digital readout for both axes, and sets speed in steps/s while loading and executing both axes simultaneously. Features include auto home and home offset, absolute/incremental control, 6-digit X-Y commands with M function outputs, and keyboard local data entry. Prices start at $3476 and include drives, motors, and 19″ (48-cm) rackmount chassis. **Aerotech, Inc,** 101 Zeta Dr, Pittsburgh, PA 15238.

Circle 272 on Inquiry Card

Intelligent motion control modules

Smart Motion™ modules provide 2 to 8 axes of continuous path motion control and feature stored, nestable subroutines that permit complex motion sequences from a single command or in response to a switch closure or programmable controller output. They handle all control and monitoring functions via a full-duplex RS-232-C serial data interface in terminal compatible code, have no control panel, and require no operator interaction. Interfaces are available for both closed-loop velocity servos and open-loop stepper drives, and up to 48 opto-isolated discrete I/O points (32 inputs/16 outputs). **Controlsmith, Inc,** 17 Airport Rd, Nashua, NH 03063.

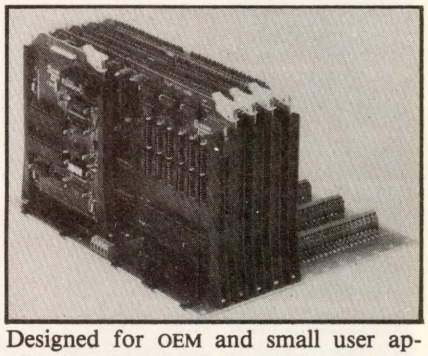
Circle 273 on Inquiry Card

Incremental shaft position encoder

Model 82 provides 2 quadrature channels for determining direction and features precision ball bearings, TTL compatible outputs, and solid state GaAs illumination sources. Zero index third channel is optionally available as well as 5-, 12-, 15-, or 24-V operation. Twenty-four std resolutions are available up to 1024 cycles; other resolutions, from 1 to 2540 cycles, are available on special order. Std round frame is also available with square flange mount. **Litton Systems, Inc, Encoder Div,** 20745 Nordhoff St, Chatsworth, CA 91311.

Circle 274 on Inquiry Card

Microcomputer system



Designed for OEM and small user applications in robotics and industrial control and automation, VIμP 7000 features wide range of optional functions including stepping motor drivers, ADCs, DACs, realtime calendar clock, and optically isolated I/O. Utilizing a 6502 microprocessor, system bus is equivalent to KIM 4 and consists of two 44-pin edge card connectors per slot. The 6.5 x 10.75″ (16.5 x 27.31-cm) board has both terminal strip and mass termination schemes. Prices start at $500. **Systems Innovations, Inc,** PO Box 2066, Lowell, MA 01851.

Circle 275 on Inquiry Card

CONTROL & AUTOMATION

Measurement and control system



TEN/50 BASICPAC™ measures physical parameters and processes and reports data online, using up to 56k bytes of user programming capability with an additional 64k bytes of RAM data capability. Operator interface makes system available with single keystroke of user programmed function keys. System includes J, K, T, R, S, E, and B thermocouple capability and features high noise immunity, bar graphs, extended message capability, onboard cartridge tape, and 4 RS-232 remote I/O ports. **Acurex Autodata,** 485 Clyde Ave, Mountain View, CA 94042.

Circle 276 on Inquiry Card

Universal distributed I/O subsystem

U12 uses up to 12 appropriate signal conditioning cards to handle process measurement or control jobs. Self-contained subsystem is plug compatible with most computers and offers either parallel or remote serial computer interfaces. Wide range of option cards permits the subsystem to interface with most sensors or actuators; custom cards are available for special requirements. Subsystem fits std NEMA cabinets and is ready to plug in and run. **Computer Products, Inc,** 1400 NW 70th St, Ft Lauderdale, FL 33307. Circle 277 on Inquiry Card

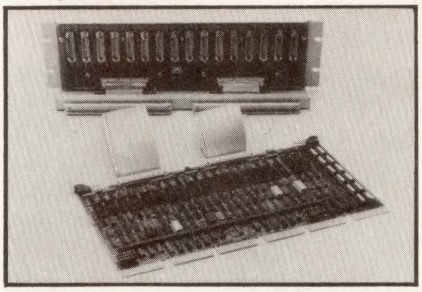
Realtime monitoring and control system

FORTRAN based RCS-7 uses interactive color graphics that can be configured by nonprogrammers. Initial CRT screen images, called RCS-7 formats, lead user through process of building new formats and defining database inputs. New formats then function as interlocking parts to evolving monitoring/control strategy. When finished, formats convey real process data to an operator via data base and receive control requests via lightpen, touch screen, or keyboard. **SGM Inc,** 8830 Interchange Dr, Houston, TX 77054.

Circle 278 on Inquiry Card

DATA COMMUNICATIONS

Single-board communications multiplexer



Model CS21/H contains all the active circuitry required to connect 16 asynchronous communications lines to PDP-11 and VAX computers. Connected by two 50-conductor flat cables to the passive 5.25″ (13.34-cm) high CP21 distribution panel, the unit is functionally compatible with DEC DH11 and transparent to std PDP-11 diagnostic and operating system software. With the company's VMS/UH software package, version CS21/HV is compatible with VMS (versions 2.0 and above) and can be used on all current VAX-11 models. **Emulex Corp,** 2001 E Deere Ave, Santa Ana, CA 92705. Circle 279 on Inquiry Card

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	DESCRIPTION	PURCHASE PRICE	PER MONTH 12 MOS.	PER MONTH 24 MOS.	PER MONTH 36 MOS.
DEC	LA36 DECwriter II	$1,095	$105	$ 58	$ 40
	LA34 DECwriter IV	995	95	53	36
	LA34 DECwriter IV Forms Ctrl.	1,095	105	58	40
	LA120 DECwriter III KSR	2,295	220	122	83
	LA120 DECwriter III RO	2,095	200	112	75
	VT100 CRT DECscope	1,695	162	90	61
	VT101 CRT DECscope	1,195	115	67	43
	VT125 CRT Graphics	3,295	315	185	119
	VT131 CRT DECscope	1,745	167	98	63
	VT132 CRT DECscope	1,995	190	106	72
TEXAS INSTRUMENTS	TI745 Portable Terminal	1,595	153	85	58
	TI765 Bubble Memory Terminal	2,595	249	138	93
	TI Insight 10 Terminal	695	67	37	25
	TI785 Portable KSR, 120 CPS	2,395	230	128	86
	TI787 Portable KSR, 120 CPS	2,845	273	152	102
	TI810 RO Printer	1,695	162	90	61
	TI820 KSR Printer	2,195	211	117	80
LEAR SIEGLER	ADM3A CRT Terminal	595	57	34	22
	ADM5 CRT Terminal	645	62	36	24
	ADM32 CRT Terminal	1,165	112	65	42
	ADM42 CRT Terminal	1,995	190	106	72
DATAMEDIA	DT80/1 CRT Terminal	1,695	162	90	61
	DT80/3 CRT Terminal	1,295	125	70	48
	DT80/5L APL 15" CRT	2,295	220	122	83
TELEVIDEO	920 CRT Terminal	895	86	48	32
	950 CRT Terminal	1,075	103	57	39
NEC SPINWRITER	Letter Quality, 7715 RO	2,895	278	154	104
	Letter Quality, 7725 KSR	3,295	316	175	119
GENERAL ELECTRIC	2030 KSR Printer 30 CPS	1,195	115	67	43
	2120 KSR Printer 120 CPS	2,195	211	117	80
HAZELTINE	Executive 80/20	1,345	127	75	49
	Executive 80/30	1,695	162	90	61
EPSON	MX-80 F/T Printer	650	62	37	24
	MX-100 Printer	895	86	48	32

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Built-in intelligence does all the housekeeping, sorting, and searching, to make even the most tedious jobs easy.

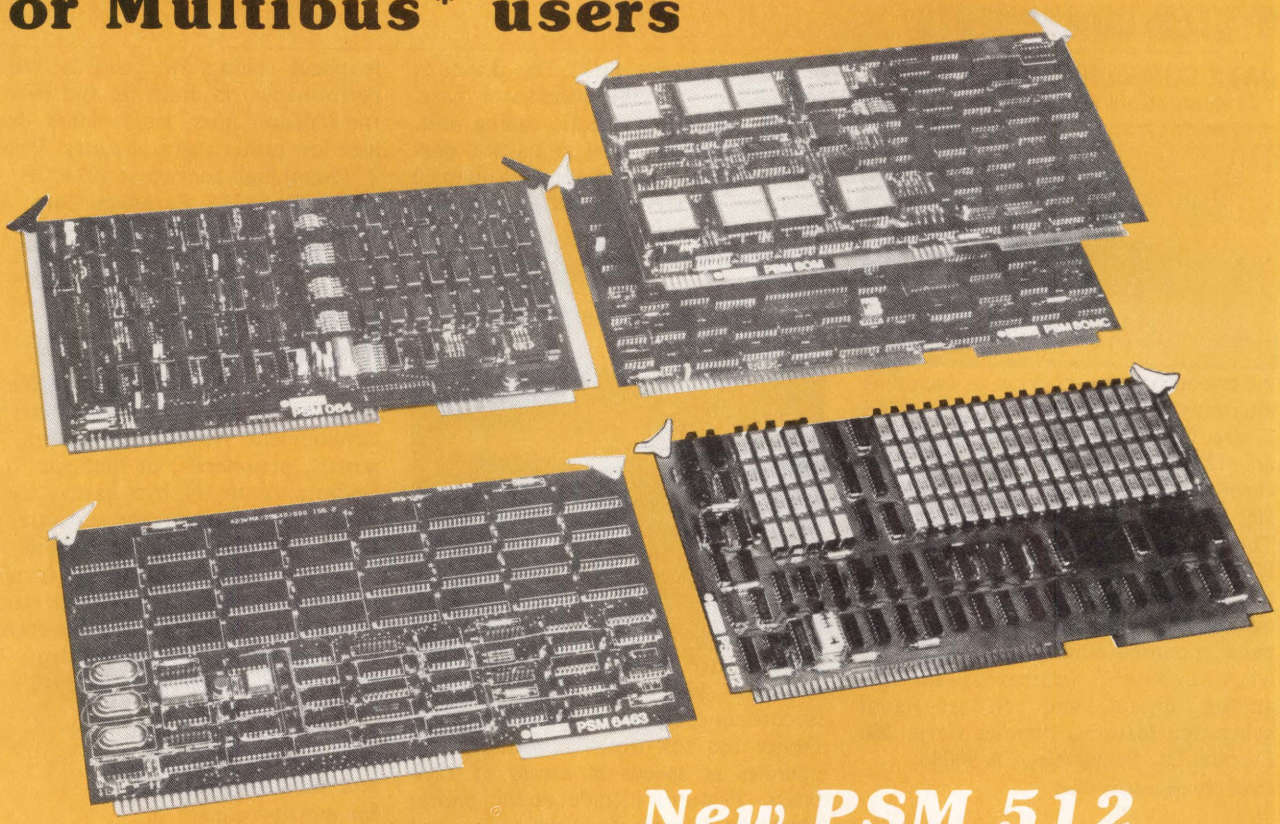
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For Multibus* users



New PSM 512

2 slots = 1 Mbyte

Plessey has successfully marketed Multibus-compatible OEM add-on storage for a good while. Now comes PSM 512, the ideal Multibus RAM card to handle the memory demands of the new breed of 16-bit micros now hitting the market. Offering a 24-bit address range, byte and word operations, 350ns access time and full bus compatibility, it packs a full megabyte into just two card slots.

The 512 is just perfect for 8612 users and systems needing very high density storage in a broad spectrum of applications, such as data capture, and multi-user systems of all kinds.

Its EDC system gives a mean time-to-data-error in excess of 15 years, using high quality, industry-standard 64k MOS dynamic RAMs. On-board control takes care of all refresh, timing and error handling. All this adds up to a memory that we're pleased to give a 12 month warranty on.

As well as its superlative performance and quality you'll be pleasantly surprised at the price.

	Technology	Capacity (bytes)	Error Handling	Address Bus Width (bits)	Data Bus Width (bits)
PSM 512	**64k DRAM**	**512k**	**Correction / Detection**	**20 /24**	**8-16**
PSM 064	16k DRAM	64k	–	20	8
PSM 6463	CMOS + battery	64K	–	20	8-16
PBS 80	Magnetic Bubbles	256k to 8M	Detection	20	8

PLESSEY
MICROSYSTEMS

Plessey Microsystems, 451 Hungerford Drive, Rockville, Maryland 20850.
Telephone: (301)279-2892 TWX: 710-828-9815
and at 1641 Kaiser Ave., Irvine, California 92714.
Telephone: (714) 540-9931 TWX: 910 595 1930

Plessey Microsystems Limited, Water Lane, Towcester, Northants NN12 7JN.
Telephone: Towcester (0327)50312 Telex: 31628

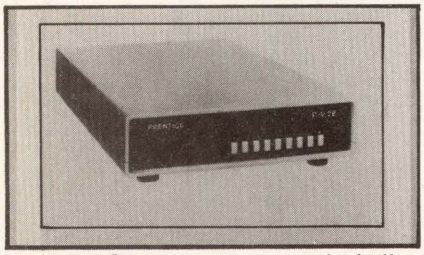
Paris: 7764106 **Noordwijk:** (01719) 19207
Munich: (089)2362226 **Rome:** (06) 350189

*Multibus is an Intel trademark

CIRCLE 151 ON INQUIRY CARD

DATA COMMUNICATIONS

V.22 compatible modem



P-V.22 conforms to CCITT V.22, including alternatives A, B, and C, and offers 2-wire, full-duplex capability. Data rates are 1200 and 600 bits/s in the synchronous mode, and 1200, 600, and 0 to 300 bits/s in the asynchronous mode. The 600-bit/s rate is available as a fallback capability to enable accurate transmission even with deteriorated transmission line characteristics. Front panel mounted diagnostic controls and AT-A-GLANCE™ indicators include analog, digital, and self-test signal generation features. **Prentice Corp**, 266 Caspian Dr, Sunnyvale, CA 94086.

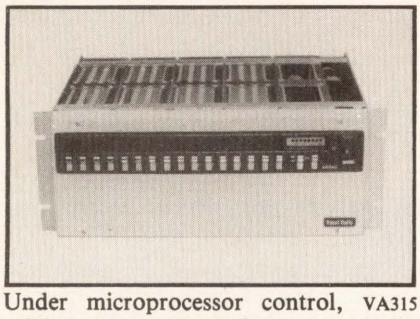
Circle 280 on Inquiry Card

Automatic answer direct connect modem

Bell 103 compatible AUTO-CAT communicates at 300 baud over dial-up telephone lines using std modular jack. It has automatic and manual answer and manual originate data modes and operates in either full or half duplex. Device features both local and remote loopback test functions. Computer-modem interface is EIA RS-232. Pressure sensitive switches on end of modem's case select answer or originate functions, and LEDs indicate operational status. Price is $249. **Novation Inc**, 18664 Oxnard St, Tarzana, CA 91356.

Circle 281 on Inquiry Card

Direct connect computer site modem



Under microprocessor control, VA315 originates/answers calls automatically or manually, and handles applications for full-duplex, 0- to 300-bit/s data transmission over the dial-up network. It replaces Bell 103A, 103E, 103J, 113A, 113B, 113C, and 113D type modems and connects to the switched network through programmable RJ41S or RJ458 data jacks or an RJ11C voice jack. The device is compatible with the company's VA811 single/multiline automatic calling unit, allowing a single RS-366 or RS-232-C port to provide automatic dialing for up to 60 modems. **Racal-Vadic**, 222 Caspian Dr, Sunnyvale, CA 94086.

Circle 282 on Inquiry Card

Interactive data communications monitor/analyzer



EPIVIEW 2000® monitors, stimulates, and emulates synchronous, asynchronous, isochronous, and bit oriented protocols. Device has 16k bytes of memory and operates at speeds in excess of 120k bits/s. Features include online parity; block-check character verification and generation for CRC-16, LRC-8, and CRC-DLC (CCITT); interface control; 4 character traps on both sides of line; and Auto-Program feature that allows operator to set up all menu items by depressing one button. **Epicom, Inc**, 592 N Douglas Ave, Altamonte Springs, FL 32701.

Circle 283 on Inquiry Card

4800-bit/s multidrop modem

Microprocessor controlled DL 4800 synchronous modem, intended for multidrop polled and point to point applications, operates full duplex over 4-wire and half duplex over 2-wire type 3002 unconditioned lines. RTS/CTS turnaround time is 50 ms. Error rate of automatic equalization is typically less than 1 bit in 10^6. End to end compatible with Bell 208, the device features extensive self-testing capabilities and is suited for rackmount and tabletop installations. **Infotron Systems Corp**, Cherry Hill Industrial Ctr, Cherry Hill, NJ 08003.

Circle 284 on Inquiry Card

9600-bit/s modem

T-96, intended for use in full-duplex, point to point applications, features training time of 253 ms, fallback operating rates of 7200 and 4800 bits/s, CCITT V.29 compatibility, and diagnostic facilities including operator initiated local and remote digital and analog loopback testing. Designed for reliable performance on domestic and overseas transmission lines, single-board design uses low power CMOS circuitry. Price in 2″ (5-cm) high package is $2740; PC version costs $2715. **Paradyne Corp**, 8550 Ulmerton Rd, Largo, FL 33541.

Circle 285 on Inquiry Card

RS-232-C communications interface option

Option provides RS-232-C connection between an M910A P/ROM programmer and development systems, computers, terminals, peripherals, or modems. It includes a 4k- to 16k-byte battery backed RAM buffer, P/ROM based software, and RS-232-C adapter. Features include key-selectable communications formats, remote control of duplicate operations, and switch-selectable baud rate from 50 to 9600 baud. **Pro-Log Corp**, 2411 Garden Rd, Monterey, CA 93940.

Circle 286 on Inquiry Card

DATA CONVERSION

ADC subsystem offered for multiprocessor or standalone applications

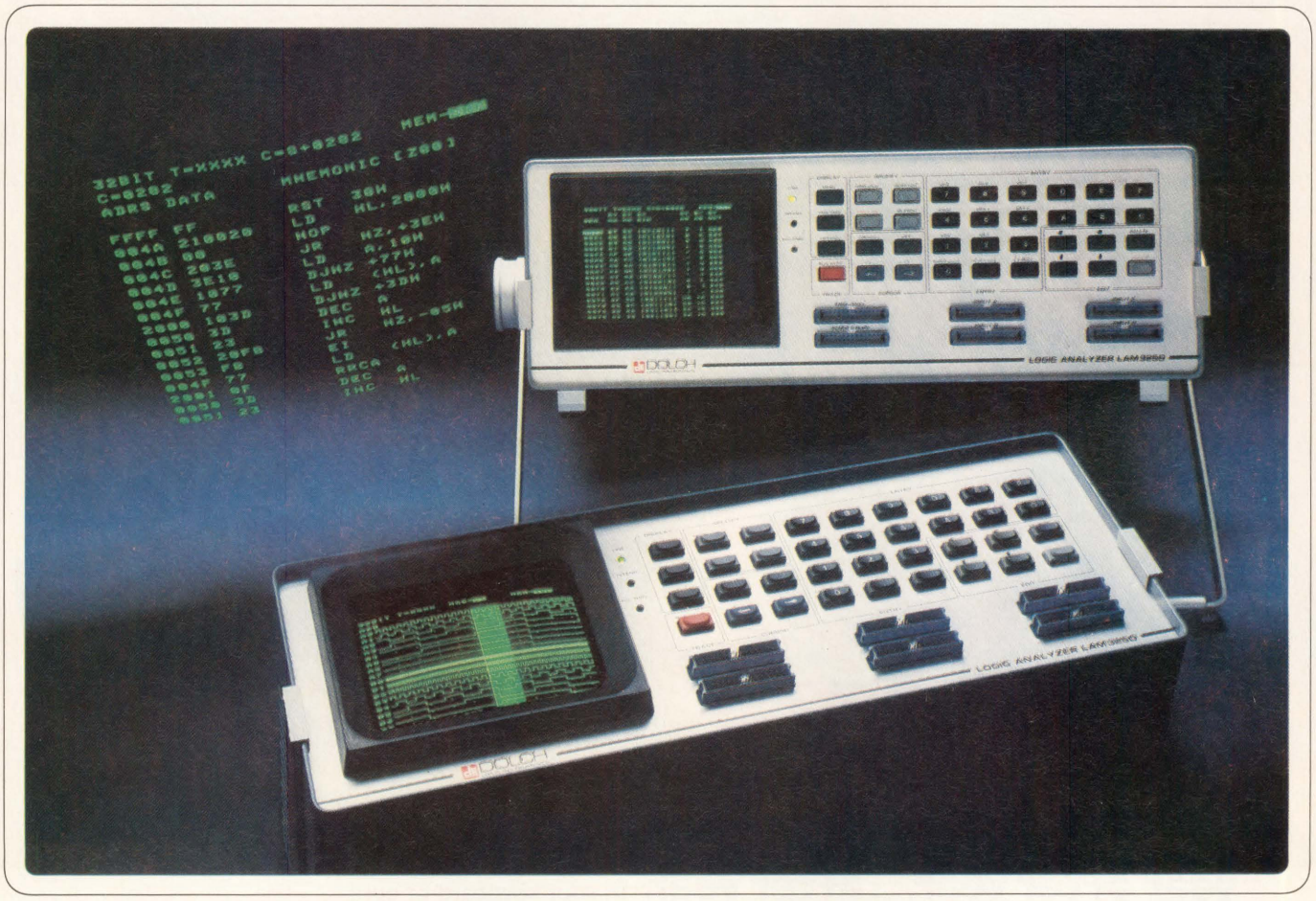
EXORciser/EXORterm™ bus compatible AIM-6809 analog input module and companion ATP-08 externally mounted analog terminal panel combine to form an intelligent, 14-bit, dual-slope integrating, high/low level A-D subsystem for standalone or multiprocessor applications. The analog input module contains a programmable gain instrumentation amplifier that provides 11 program selectable gain levels between 1 and 1024; a dual-slope integrating, 12-bit binary plus sign and overvoltage, byte organized ADC; and a 6809 microprocessor that selects amplifier gain and stores converted data in shared memory or outputs it through an RS-232-C communications port. Module also provides 1k byte of static RAM, 2 sockets for mounting 1k/2k-byte RAM or 2k/4k/8k-byte EPROM devices, 4 differential or 8 single-ended input channels, and an input range of 10 mV to 8.192 V. In std configuration, the module is capable of 7.5 conversions/s. Two op temp ranges are available: 0 to 70 and −40 to 75 °C.

Up to 4 analog termination panels connect to an analog input module, expanding the A-D subsystem's input capability to 32 differential input channels or 64 single-ended input channels. The panels provide 300-V overvoltage protection, current guarding for analog input channels, a cold reference junction, and an RTD precision source of 2.048 V. **Phoenix Digital Corp**, 2315 N 35th Ave, Phoenix, AZ 85009.

Circle 287 on Inquiry Card

Dolch.

advanced logic analysis



32 to 64 Channels plus Mnemonics.

Trace it all—fast—and disassemble your code into Mnemonics. When you have a sophisticated job to do, don't get bogged down in machine code. The Dolch LAM 3250 logic analyzer gives you the channels you need to trace data, address, port and control lines. And Dolch makes sure you'll be able to handle future needs with channel expansion to 48 or even 64 channels.

Hook up fast, too. Dolch personality probes clip right over your CPU chips so you don't waste valuable time connecting dozens of individual hooks on IC pins. And the probe takes care of clock, timing and signal interfacing so you don't have to worry about signal conditions.

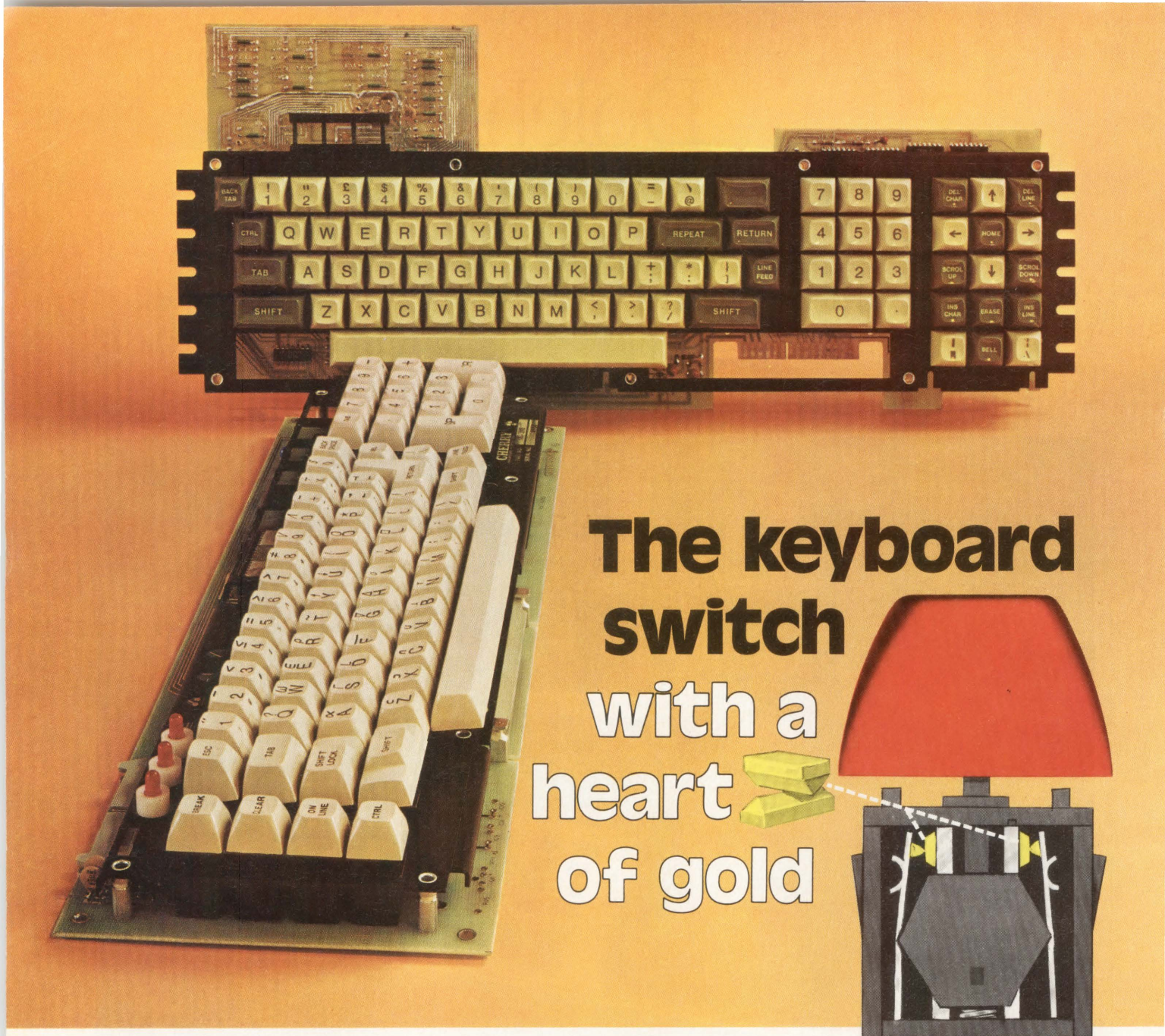
Store your setups. The Dolch LAM 3250 lets you hold setups in a nonvolatile memory. Six files of menu and display configurations can be stored for up to three months without power. You don't have to reprogram every time you power up.

Don't settle for less than Dolch. The LAM 3250 is truly a universal logic analyzer with recording speeds of up to 50 MHz, sophisticated sequential triggering, multilevel clocking, and 1 K-deep source and reference memories.

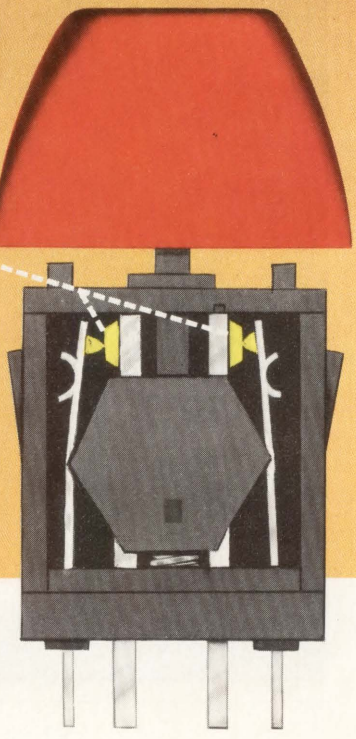
See a demonstration. You'll appreciate the difference in Dolch. For details on the LAM 3250, or any of our other trouble-shooting tools, write: Dolch Logic Instruments, Inc., 230 Devcon Drive, San Jose, CA 95112. Or call toll free: (800) 538-7506; in California call (408) 998-5730.

dli DOLCH
LOGIC INSTRUMENTS

CIRCLE 152 ON INQUIRY CARD



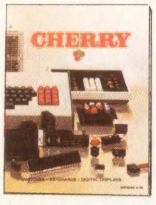
The keyboard switch with a heart of gold



...keeps your product WORKING year after year...after year.

In your keyboard or ours, Cherry key switches just don't fail. The knife-edge contact area is so small (9 millionths of a square inch)... the contact pressure so great (about 5,000 psi) ... the gold alloy so pure and film-free ... that you are assured of positive contact every time. For 50 million operations and beyond. (Which is probably beyond the life expectancy of your product!)

Cherry "heart of gold" keyboard switches are available individually or with two-shot molded keycaps. Hopefully, you want keycaps. Because, *we have keycaps* ... in more legends, sizes, type faces than you're likely to find anywhere else. Sculptured keycaps? We've got 'em. Gloss or matte finish? We've got *both.* Colors? Lighted? Specials? Sure! Some "off the shelf"... all at prices that make it obvious why the *Cherry* way is the *economical* way to put a heart of gold in any keyboard.



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CIRCLE 153 ON INQUIRY CARD

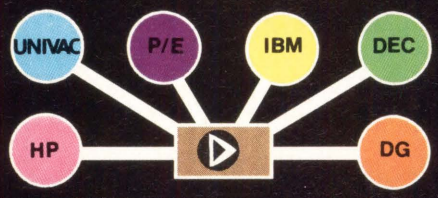


2 Years and $1 Million Better

Not just another 45 ips tape transport, the all new DATUM D451F is the result of an investment of over $1 million and two years of intensive research and development.

Completely redesigned, the D451F features enhanced microprocessor control and an embedded, dual-density formatter on just two circuit boards. Electronic components are functionally grouped and clearly marked for easy identification. And, serviceability is enhanced by one of the industry's most comprehensive on-board diagnostic program sets.

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Only DATUM manufactures both the tape transport and the controller. And only DATUM offers you a full line of controllers designed to interface with most popular CPU's (Data General, Digital Equipment, IBM, Hewlett Packard, Interdata, Univac).

After 2 years and $1 million, DATUM offers you the D451F . . . the latest state-of-the-art 45 ips tape transport. To get all the facts, call or write:

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DATA CONVERSION

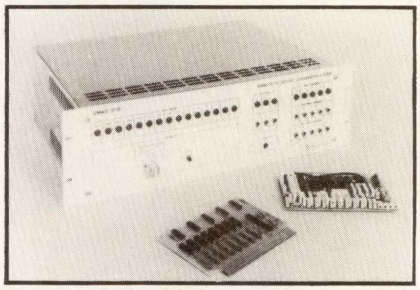
Monolithic 16-bit DAC requires only 12-bit accurate resistor matching

Utilizing a segmented design that yields a full 16-bit monolithic DAC, but requires only 12-bit accurate resistor matching, the AD7546 features guaranteed monotonicity over temperature and max linearity error of ±0.012% of full-scale range. Included in the single chip are 16-segment resistors, a 12-bit voltage switching DAC, a 16-bit wide data latch, a deglitch switch, and switch decoding logic and drivers. Device features full microprocessor compatibility, CMOS and TTL compatible latched inputs, low power consumption (50 mW typ), and a constant output impedance voltage output.

Four versions are available: KN and JN grades, packaged in 40-pin plastic DIPs, are specified over 0 to 70 °C, while AD and BD grades are specified over −25 to 85 °C and are packaged in ceramic. Relative accuracy for KN and BD grades is ±0.012% max, and differential nonlinearity is ±0.0015% max. JN and AD grades are specified for relative accuracy of ±0.05% max, and differential nonlinearity of ±0.006% max. Settling time is 5 μs typ, to within ±0.003% of final value, and 10 μs typ, to within ±0.00076% of final value. The DAC requires 15- and −5-V power supplies at a ±5% tolerance for specified performance and is priced from $29.75 in quantities of 100. **Analog Devices, Inc,** Rte 1 Industrial Pk, PO Box 280, Norwood, MA 02062.

Circle 288 on Inquiry Card

A-D conversion system



GM29SE, designed for use in automatic test and data acquisition systems, features 32 differential analog input channels (expandable to 128 channels), programmable gain input, and 15-bit resolution at 70k samples/s. Linearity is ±0.02% of full scale on all gain settings, crosstalk is less than 0.01% of full scale from dc to 60 Hz, stability is ±0.01% of full scale (30 days at same temp), and common mode rejection is 80 dB from dc to 1 kHz. Analog input on any channel can be ±0.625, ±1.25, ±2.5, ±5, or ±10 V. **Preston Scientific, Inc,** 805 E Cerritos Ave, Anaheim, CA 92805.

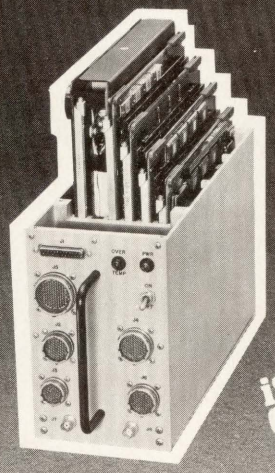
Circle 236 on Inquiry Card

Industrial Multibus D-A board

Memory mapped ST-728 is compatible with both 8- and 16-bit Multibus systems and features 4 or 8 D-A channels, 12-bit resolution, and 5 individually selectable output ranges (±5 Vdc, ±10 Vdc, 0 to 5 Vdc, 0 to 10 Vdc, and 4- to 20-mA current loop) for each channel. The board draws power from the Multibus 5-V line, weighs approx 11.2 oz (0.3 kg), and operates over a temp range of 0 to 55 °C with relative humidity from 10 to 90% (noncondensing). **Datel-Intersil,** 11 Cabot Blvd, Mansfield, MA 02048.

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Ruggedized Microcomputer



iSBC 80 Compatible

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SECS 80 is a ruggedized version of Intel's iSBC* single-board computer. Even uses the same development system software.

Meets MIL-E-5400, 4158, 16400, making it perfect for military, avionics, and tough industrial environments.

SECS 80 comes with a multitude of support modules: RAM, ROM, EPROM, digital tape recorder and controller, 1553 interface, A-D converter, digital I/O, high-speed arithmetic unit, and more.

You can buy a complete system or configure your own with individual modules. Either way, this versatile microcomputer system will save you valuable time and development costs.

Phone or write for complete details today.

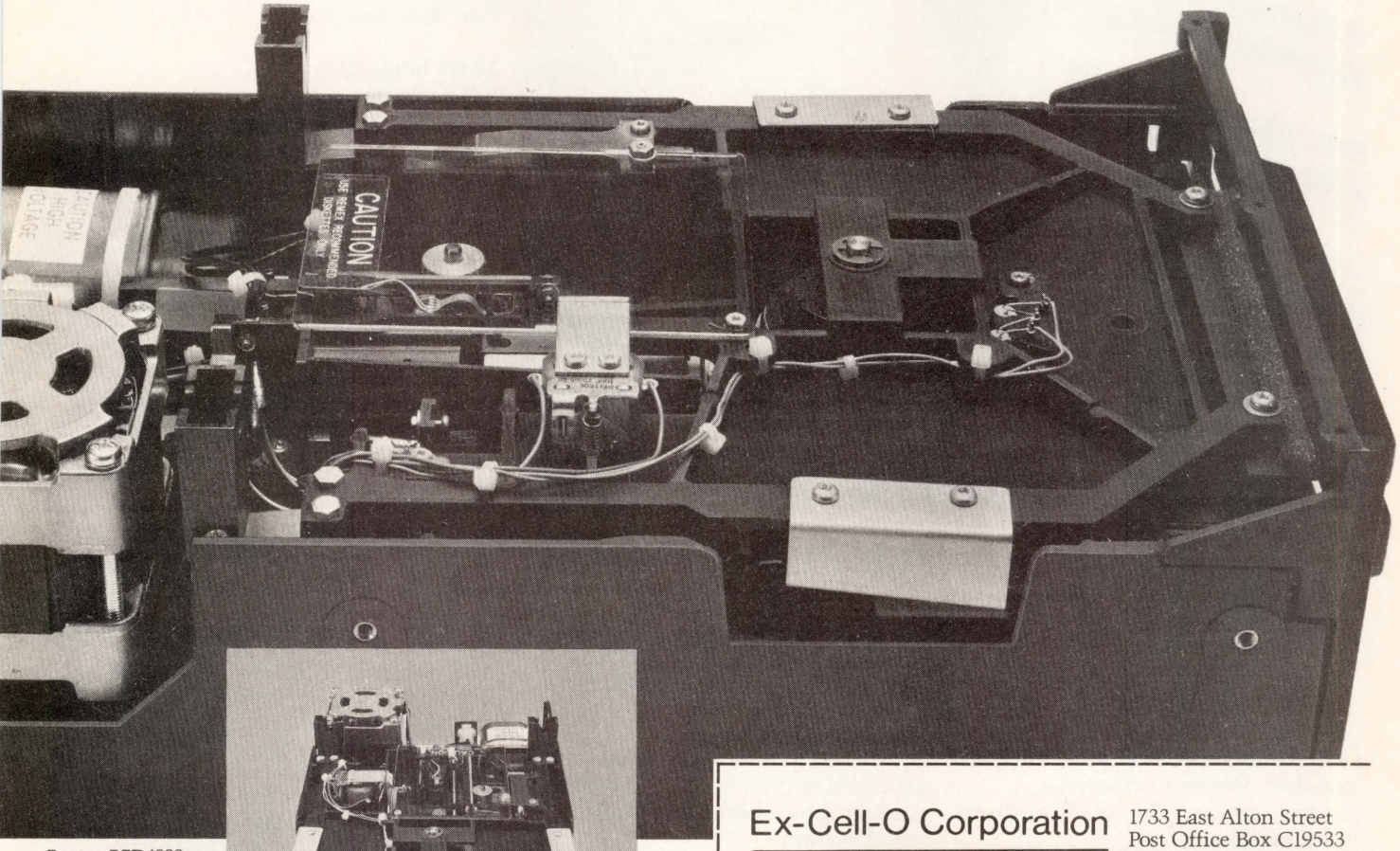
*Trademark of Intel Corporation

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Severe Environment Systems Company
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Telephone: (213) 998-9090 • Telex: 69-1404

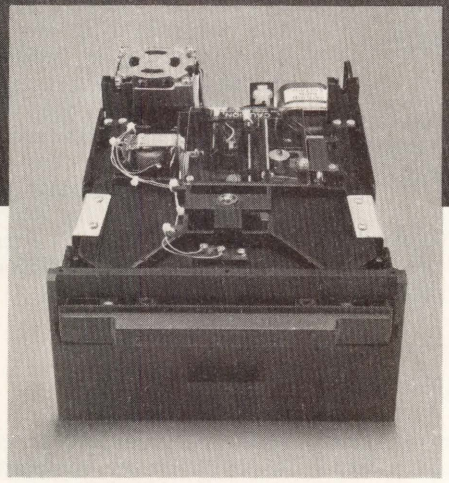
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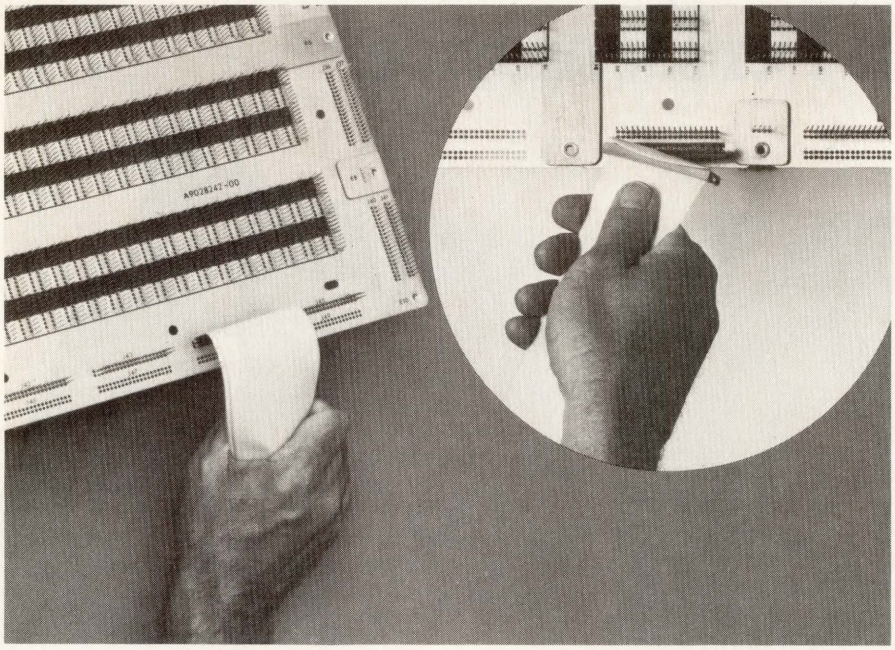
DATA CONVERSION

16-bit DAC achieves near-zero drift over time and temperature

A high resolution, true 16-bit DAC, DAC74 incorporates transparent microprocessor calibration circuits to achieve near-zero drift over time and temperature. Converter features self-calibration and maintains 16-bit accuracy by removing linearity, gain, and offset errors caused by temperature variations, aging, and varying load conditions. Device maintains ±1 LSB total error, ±0.00075% max nonlinearity, ±0.00075% max gain error, and ±80-μV max offset, all over a 15 to 45 °C temperature sweep, for 1 year before manual readjustment is necessary.

Automatic calibration cycle is initiated with a single TTL pulse; a "calibrated" signal indicates completion of the 2.5-s calibration cycle. Converter offers uni- or bipolar voltage output and is double buffered for interface to an 8- or 16-bit bus. Its noise shielding metal package measures 5 x 7 x 0.6" (13 x 18 x 1.5 cm); 34-pin digital and 40-pin analog user connectors provide interconnection. Primary applications include high resolution, high accuracy test equipment; analytical instruments; remote installations where frequent access to equipment is undesirable or impossible; and applications where temperature drifts cannot be tolerated. Unit price is $1495. **Burr-Brown, Data Conversion Products,** PO Box 11400, Tucson, AZ 85734.

Circle 290 on Inquiry Card



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Our strain relief isn't just snapped together. We've perfected a unique, rugged, *molded-on* strain relief system.

That's why designers specify Chabin Transmission Line Assemblies (TLAs) to get their high-speed signals from board to board or subsystem to subsystem.

After the connector is attached to the cable, the entire assembly is injection molded to provide an integral strain relief.

The result? Ultra-reliable transmission line assemblies . . .

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- Even if they're roughly treated.

For high-speed data transfer assemblies that work all the time, specify the dependable strain relief system.

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At Chabin, we're large in capability yet small enough to be responsive.

12-bit integrating A-D converter

System oriented 7109 interfaces directly to a microprocessor by means of byte organized TTL 3-state outputs. It is directly accessible via 2 byte enable inputs and the chip select input for simple parallel bus interface. Features include monotonic performance with no missing codes and an auto-zero circuit that maintains the zero code without requiring zero adjustment. Input stage features 1-pA typ input bias current and 15-μV pk to pk typ input noise. **Teledyne Semiconductor,** 1300 Terra Bella Ave, Mountain View, CA 94043.

Circle 291 on Inquiry Card

Digital signal processors

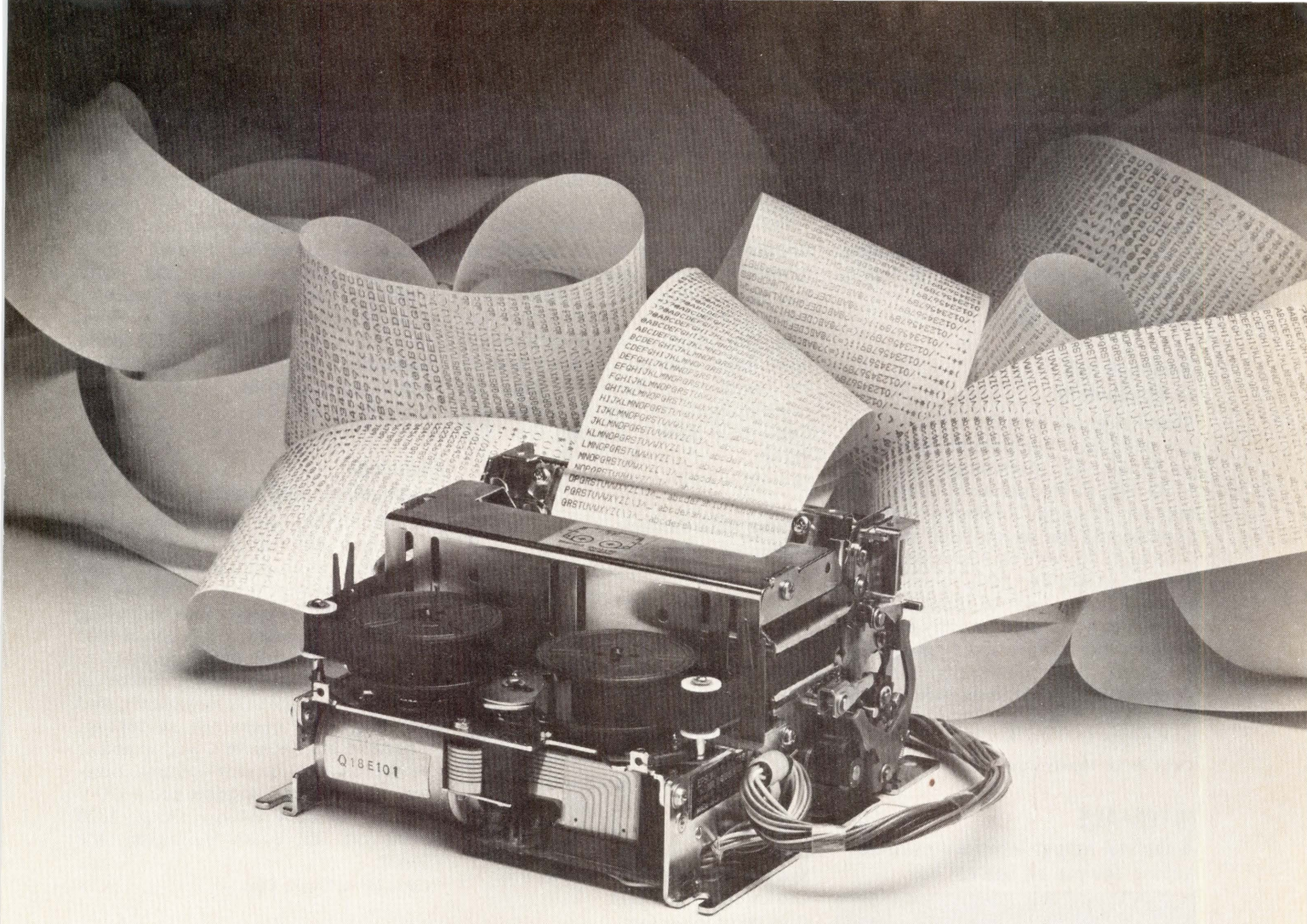
S2811 high speed arithmetic processor features a parallel bus architecture that links the 12 x 12 multiplier and 16-bit add/subtract unit with instruction and data memories to achieve a 300-ns instruction cycle time. Independent serial and parallel I/O ports increase programmer flexibility. Unit operates standalone or with any 8- or 16-bit microprocessor. S2814A fast Fourier transformer uses a decimation in frequency technique to calculate 32-point fast and inverse fast Fourier transforms in 1.3 ms. **American Microsystems, Inc,** 3800 Homestead Rd, Santa Clara, CA 95051.

Circle 292 on Inquiry Card

14-bit S-D and R-D tracking converter

HSDC-8915 Monobrid™ series, housed in 36-pin double DIP, combines monolithic and hybrid technologies and features 10-rotation/s min tracking at 400 Hz and 3-state latched outputs. Internal logic is CMOS and all logic inputs and outputs are buffered to external logic level. Series is available in 8 input models, 2 accuracy grades, and 2 temp

CIRCLE 157 ON INQUIRY CARD



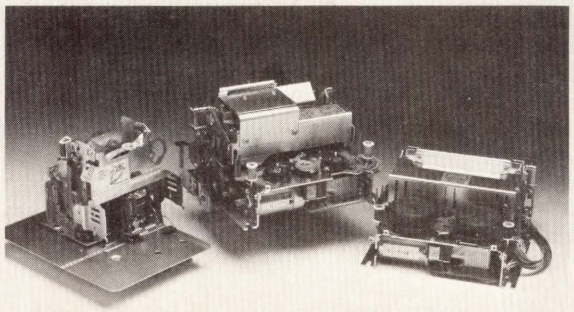
OUTRUNS THE COMPETITION.

The print head on a C. Itoh 500 series dot matrix printer prints out over 100,000,000 characters in its lifetime. That's a lot of cash register receipts. A lot of journal entries. It's one reason why C. Itoh printers are among the most reliable in the industry. And the most popular.

Of course, every series 500 printer is also long on features. Each is bi-directional. Each prints a fast 152 CPS. But best of all, there's one just right for your application. Our Model 512, for example, is the perfect journal printer with 40-column printout for a variety of applications. The Model 522, on the other hand, gives you two-stage 18-column journal/18-column receipt printing complete with logo stamp and automatic paper cutter for cash register applications. For efficient flat bed ticket or slip printing, the Model 542 40-column unit is the one to buy.

C. Itoh Series 200 printers are equally impressive. Compact and rugged, each requires just 24VDC and prints 5x7, 7x7 or 9x7 matrices at 2.4 LPS from a reliable 7-wire print head. They're the OEM's choice for cash registers, home computers, data loggers, electronic calculators and general peripherals. Choose the Model 210 roll-fed printer with 26-35 column capacity. Or the sprocket-fed Model 210S with 22-30 columns. You get 2-color printing either way. For dual-roll applications, the Model 220 records receipt and journal entries and features auto-stamp and independent high-speed line feed. And for multi-ply slip document applications, there's the Model 240 featuring an adjustable document stop gate.

So if you're looking for a little printer with a lasting impression, contact C. Itoh Electronics, Inc., 5301 Beethoven St., Los Angeles, CA 90066; Tel. (213) 306-6700. New York office: 666 Third Ave., New York, NY 10017; Tel. (212) 682-0420.



C. ITOH ELECTRONICS, INC.

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CIRCLE 158 ON INQUIRY CARD

DATA CONVERSION

ranges. Accuracy is ±4 min ±0.09 LSB and ±2.6 min. Op temp ranges are −55 to 125 and 0 to 70 °C. Device requires 15-vdc power supply in addition to external logic power supply. ILC **Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716.

Circle 293 on Inquiry Card

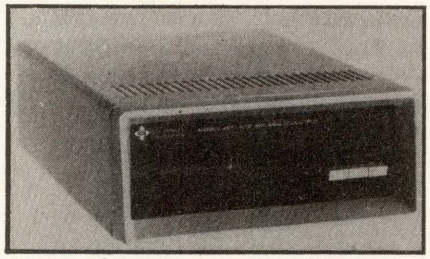
Miniature 5-V dc-dc converter

Model MSR2805S provides 3.5 W of output power at 5 Vdc from an input of 16 to 32 Vdc, with overvoltage protection to 40 Vdc. It features short circuit protection through foldback current limiting and has an op temp range of −55 to 85 °C, with derated operation to 1 W at 110 °C. Unit has a volume of 0.4 in^3 (6.6 cm^3) and is supplied in a hermetically sealed metal package designed for military and aerospace applications. MIL-STD-883B environmental screening is optional. **Integrated Circuits Inc,** 13256 Northrup Way, Bellevue, WA 98005.

Circle 294 on Inquiry Card

INTERFACE

4-channel output interface controls analog devices on IEEE-488 bus



A general purpose coupler with IEEE-488 bus controlled dc analog outputs, model 4871 provides IEEE-488 bus control of analog devices. This analog output interface operates as listener or talker, with most of its functions user programmable in software. Four analog output channels have 3 separate, user-selectable output signal ranges per channel: 0 to 10 V, −10 to 10 V, and −4 to −20 mA. Analog output channels are isolated from the bus as well as from the device's internal logic, providing a low noise environment for system applications.

Features include self-test upon turn-on and 3 modes of automatic calibration: Internal Auto-Cal, External Auto-Cal, and Software Auto-Cal. Internal Auto-Cal is performed automatically at turn-on and provides zero- and full-scale calibration of the dc output of each analog channel. External Auto-Cal functions in a similar manner, except that desired value is read at the output of externally connected device that generates it. Software Auto-Cal places offset and scale factor values into an equation to exactly determine required output parameter.

The unit also connects most digital instruments to the bus via 24 parallel TTL compatible input lines (with handshaking) that accept up to 24 binary bits (6 digits of BCD data). Two auxiliary outputs are available as well. Four auxiliary relays provide on/off and power control for auxiliary devices and functions powered from the bus. ICS **Electronics Corp,** 1620 Zanker Rd, San Jose, CA 95112.

Circle 295 on Inquiry Card

Severe environment analog I/O subsystem

SECS 80/732, a severe environment version of Intel's iSBC 732™, provides a 32-channel 12-bit ADC, two 12-bit D-A output channels, and a sample and hold programmable gain amplifier on a 6 x 9″ (15- x 23-cm) air transport rack circuit card. The module will operate under a 10-G vibration level (per MIL-E-5400) and a 15-G (11-ms) shock. Operating temp is −55 to 85 °C and operating humidity is 0% to 95% with condensation. All components meet MIL-STD 833 level B for high reliability. EMM **Severe Environment Systems Company,** 20630 Plummer St, Chatsworth, CA 91311.

Circle 296 on Inquiry Card

Inverting buffers have complementary enables for multiplexed bus driving

High speed, 8-bit wide octal interface buffers SN54/74LS210, −/74S210, and −/74LS310 are inverting versions of the industry std noninverting SN54/74LS241, −/74S241, and −/74LS341 octal buffers, respectively. Devices feature 3-state outputs, complementary enables for fast, multiplexed bus driving, and either PNP (−/74LS210 and −/74S210) or Schmitt trigger (−/74LS310) inputs. Schmitt trigger inputs provide greater hysteresis for full 200-mV guaranteed (400-mV typ) noise immunity on either side of switching threshold; "deadband" in which noise is ignored has width of 400 mV guaranteed (800 mV typ). Buffers are housed in 20-pin, 300-mil (0.76-cm) wide SKINNYDIP™ packages.

Each device is internally organized with 2 groups of 4 buffer elements; 1 enable input controls the buffer elements within each group. Enable 1 (E1) is "assertive low," while Enable 2 (E2) is "assertive high." A TTL low voltage on E1 causes the buffer elements of group 1 to be enabled, and a TTL high on E1 causes them to go into a high impedance state. Since E2 is assertive high, it operates according to the reverse scheme. Architecture provides optimum system speed when bus is driven from 2 alternate sources within the same module or local circuit group. Typically, E1 and E2 are tied together and driven by the same control signal. **Monolithic Memories, Inc,** 1165 E Arques Ave, Sunnyvale, CA 94086.

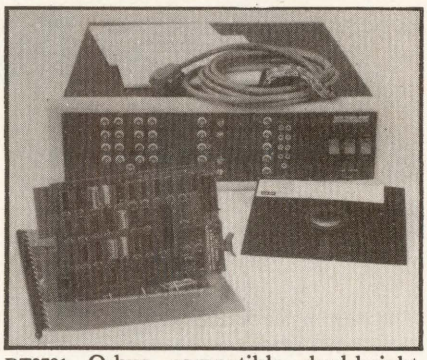
Circle 297 on Inquiry Card

Wireless computer/ac line interface

TeleBrain™ RS-232-C communicates programmed, automated switching decisions throughout an entire facility using software and existing ac wiring. It transmits switching decisions emanating from a host computer to any one of 1600 Teleswitch™ independent control points. The control point device receives the discrete command, identifies it, and performs the necessary switching. Telebrain interfaces with any computer having an RS-232-C serial output, plugging into the host computer and a 110-V outlet. **National Energy Corp,** 1820 Shelburne Rd, South Burlington, VT 05401.

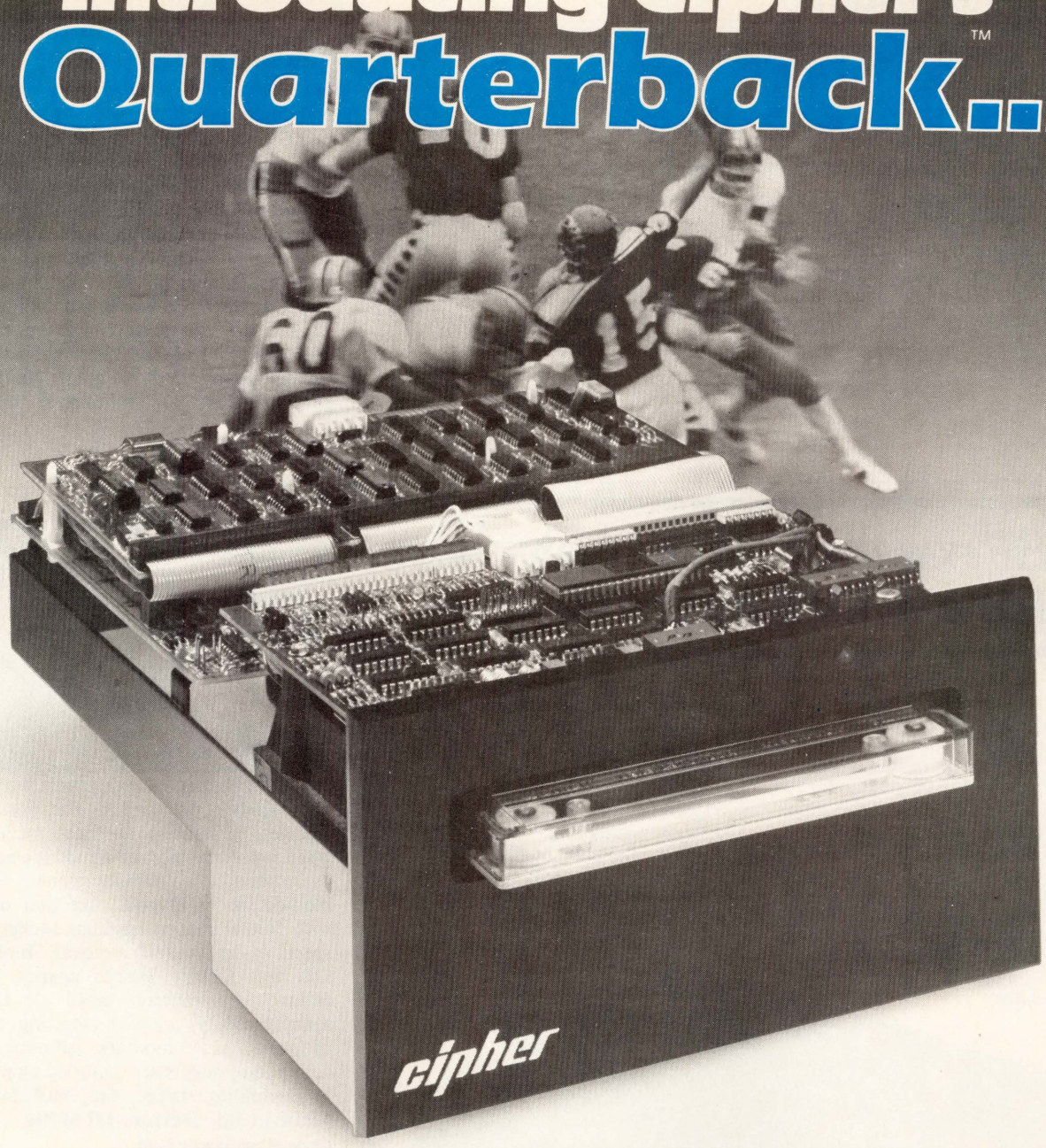
Circle 298 on Inquiry Card

IEEE-488/Q-bus interface



DT2791 Q-bus compatible dual-height board provides complete hardware and software support for interfacing up to 14 peripheral devices on the IEEE-488-1978 GPIB to the LSI-11 series Q-bus within LAB-DATAX. It provides talker, listener, and controller capabilities on the GPIB and can be used in either single- or multiple-controller environments. Board is furnished with 8″ (20-cm) flexible diskette containing device support and control subroutines and utility program. Power required is 5 V at 1 A. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752. Circle 299 on Inquiry Card

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Our new 1/4-inch cartridge streaming drive has the intelligence and the physical ability to give you all-pro performance. It's the ideal device to backup lower capacity Winchester disks.

Just look at these stats:

- ☐ It has a microprocessor-controlled intelligent formatter that does complete error corrections and retries, totally transparent to your system, to give you the highest data reliability.
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- ☐ It has a storage capacity of 20 megabytes, and that's formatted data.
- ☐ It gives you a choice of 30 or 90 ips models, which translates directly to a transfer rate of either 30 or 90 kilobytes per second—you can transfer 20 megabytes in just over four minutes.
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CIRCLE 160 ON INQUIRY CARD

INTERFACE

Intelligent multiple-axis stepper motor controller

First in PICMAC® family is the DEC LSI-11/2, –/23 Q-bus compatible controller. Dual-wide card contains 2 independent 4-phase stored program controllers that operate in immediate command execution, program entry, and stored program execution modes. In most applications, controller functions without processor intervention, except for program loading. When stored program is done, or motion is complete, controller notifies processor via interrupts. **Robotic Synergy,** 1336 S 1100 East, Suite 210, Salt Lake City, UT 84105.

Circle 300 on Inquiry Card

BASF has the 8" Winchester drive with the difference you can see.

Notice that our linear voice coil actuator and many of our electronics are positioned *outside* the basic package. It makes a big difference in reducing circuit-damaging heat, and cuts your risk of magnetic field-induced data loss. Our linear actuator is a far more accurate and higher performance design than the competition's rotary or stepper motor systems, and more appropriate to tomorrow's high track densities.

- Field-proven for more than two years.
- Available for immediate delivery.
- 8, 24, and 40 megabyte unformatted capacity.
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- Incorporates BASF-manufactured disks...never a shortage.

Write for complete details, or call, in the East, (617) 271-4168; in the West, (714) 752-6126.



It looks different because it is different.

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ATTN: Marketing Services, Computer Hardware Products.
Please send me complete details on the BASF 6170 Series 8" Winchester Drives:

Name_____ Title_____
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CD-11

BASF

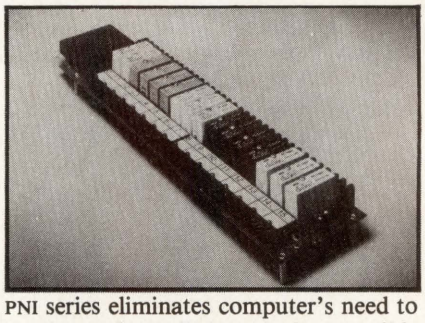
See us at COMDEX, Booth 178/80

Peripheral processor interface

PPL-1 permits interconnection of 2 LSI-11 computers or an LSI-11 and a PDP-11 computer in a host-satellite configuration; up to 32k bytes of main memory can be shared between the 2 processors. Sixteen vectored interrupts implement a communications protocol between the 2 computers. Memory window size is switch-selectable (in 4k increments) up to 32k bytes. Processor link is composed of 2 quad size PCBs connected by a 50-conductor ribbon cable. The 2 boards can be up to 30′ (9 m) apart. **Ranyan, Inc,** PO Box 790, Huntington Beach, CA 92648.

Circle 301 on Inquiry Card

I/O module boards



PNI series eliminates computer's need to continuously poll inputs for possible changes, generating an interrupt only when input changes; interrupt is cleared by computer handshake signal. Fuse module has rigid gold pins that mate with funnel shaped entrance sockets to speed insertion and removal. Built-in LED test feature guards against LED failure. Pushbutton tests all LEDs simultaneously, without affecting state of individual I/O modules. All LEDs and active components are mounted on plug-in assemblies. **duTec, Inc,** 4801 James McDivitt Rd, Jackson, MI 49204.

Circle 302 on Inquiry Card

4-port parallel I/O interface

Model 2720 allows S-100 system users to exchange bidirectional parallel data at high speeds with 3 peripherals and to transmit parallel data to a fourth peripheral. Data are transferred at TTL levels on separate 8-bit input and output data pathways. A full 4-line/port handshaking scheme ensures thorough communication protocol of both transmitter and receiver. The 4 parallel ports can be jumper assigned to any block of 4 I/O addresses where the base is a multiple of 4. Sense polarity of each handshaking line is jumper selectable. **California Computer Systems, Inc,** 250 Caribbean Dr, Sunnyvale, CA 94086.

Circle 303 on Inquiry Card

CIRCLE 161 ON INQUIRY CARD

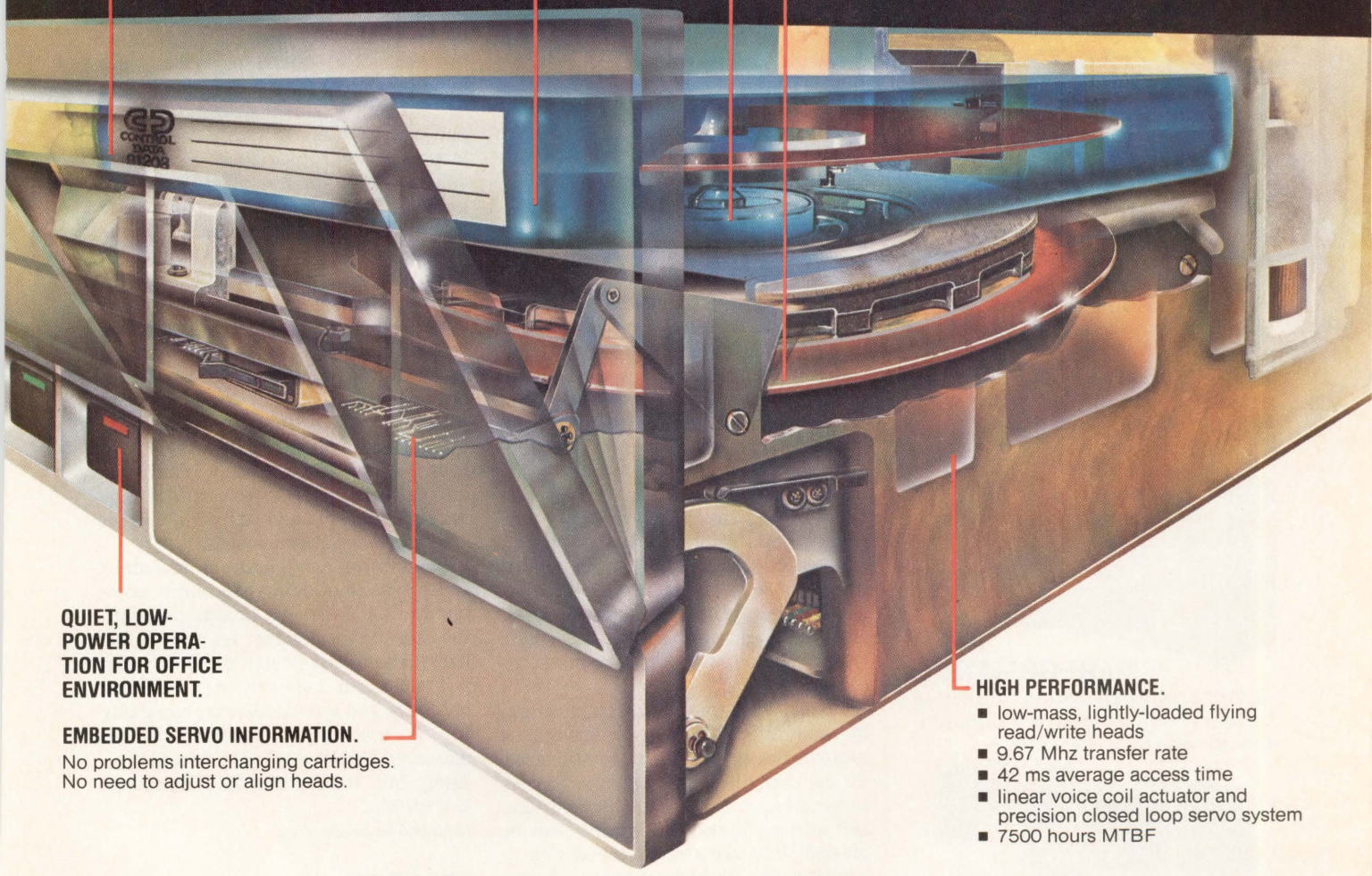
The LARK™

SOLVES BACK-UP AND OFF-LINE STORAGE PROBLEMS. Besides 8 Mbytes of *fixed* storage, Lark gives you 8 Mbytes of *removable* storage—per cartridge. Simplifies back-up and gives users both flexibility and growth capacity.

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COMPACT SIZE AND PACKAGING FLEXIBILITY. You can design smaller, more efficient systems. The Lark is the width of a floppy disk drive. In fact, you can mount two units horizontally or three vertically in a standard 19-inch rack.

EXCEPTIONAL RELIABILITY. Since the Lark is totally sealed during operation, no external air is forced across either the fixed module or cartridge disk surfaces.

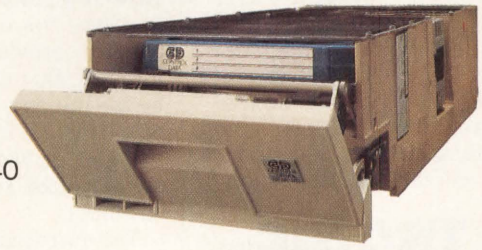


QUIET, LOW-POWER OPERATION FOR OFFICE ENVIRONMENT.

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No problems interchanging cartridges. No need to adjust or align heads.

HIGH PERFORMANCE.
- low-mass, lightly-loaded flying read/write heads
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- 42 ms average access time
- linear voice coil actuator and precision closed loop servo system
- 7500 hours MTBF

Now—an 8 inch drive with REMOVABLE MEDIA



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Control Data Corporation
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CONTROL DATA

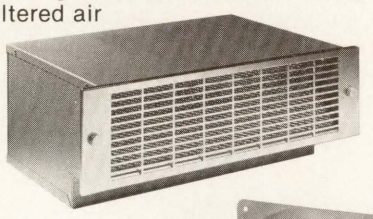
Addressing society's major unmet needs as profitable business opportunities

CIRCLE 162 ON INQUIRY CARD

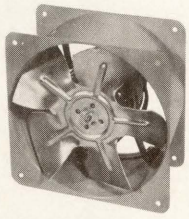
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INTERFACE

Floppy disc controller/formatters

FDC 179X family consists of 6 N-channel IBM 3740 compatible MOS/LSI devices, each packaged in a ceramic or plastic 40-pin DIP. FDC 1791 is IBM 3740 compatible in single-density mode and system 34 compatible in double-density mode; FDC 1793 is identical except that its data bus lines use positive rather than negative logic. FDC 1792 and 1794 are single-density versions of FDC 1791 and 1793, while FDC 1795 and 1797 are double-sided, double-density versions of FDC 1791 and 1793. **Standard Microsystems,** 35 Marcus Blvd, Hauppauge, NY 11787.

Circle 304 on Inquiry Card

MICROPROCESSSORS/ MICROCOMPUTERS

Piggyback design aids prototyping of single-chip microcomputers

NS87P50 piggybacked EPROM single-chip microcomputer eases prototyping in designs based on industry std 8048, 8049, and 8050 CPUs. Device contains system timing, control logic RAM, EPROM, and program module, plus 27 I/O lines to implement prototype program development and emulation. Fabricated using the company's proprietary XMOS process and housed in a 40-pin DIP, the microcomputer includes a plug-in adapter that accepts a 24-pin EPROM (2758A, 2716, or 2732) that replaces the normally onchip ROM of the INS8048 series, and a program module (IPM) that selects either INS8048, 8049, or 8050 mode of operation.

In the unit's piggyback architecture, the address and data buses have been brought out to include external EPROM. To the CPU, the external EPROM appears to be directly coupled to internal data and address buses. Std EPROMs can be plugged into the top of the device to emulate the 1k-byte INS8048, 2k-byte INS8049, or 4k-byte INS8050.

Mounted on top of the microcomputer, the program memory consists of 1024, 2048, or 4096 8-bit bytes of P/ROM (MM2758A, 2716, or 2732). A 12-bit program counter provides P/ROM addressing. Resident RAM data memory is arranged by the IPM and configures the 256 bytes of RAM into a format appropriate to the 8048, 8049, or 8050. The unit's 27 I/O lines are organized as three 8-bit ports plus 3 test inputs.

The microcomputer aids development when used in conjunction with the company's Starplex development system. In quantities of 100 or more, it is priced at $87. **National Semiconductor,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

Circle 305 on Inquiry Card

Multi-user computer system features enhanced version of UNIX operating system

A multi-user computer system designed for commercial applications in general business environments, System 8000 provides minicomputer level performance using the Z8000™ 16-bit microprocessor and ZEUS,™ an enhanced version of the UNIX™ operating system. Enhancements include a visual editor utility suited for word processing and other text-oriented applications, plus a higher degree of access control than that found in UNIX. The operating system also handles random records in large files (up to 1G byte), retains regular parameters, and enables users to create customized loops and control variables. Since these enhancements do not affect the UNIX kernel, UNIX programs developed on other systems can be transported to the System 8000. The system offers high level languages including COBOL, Pascal, C, and the company's PLZ.

Based on the 6-MHz segmented Z8001A processor, CPU card features 3 onboard Z8010A memory management units supporting segmented or nonsegmented processes. System supports up to 1.5M bytes of error correcting memory. Up to four 24M-byte, 8″ (20-cm) Winchester disc drives and 17M-byte cartridge tape backup units are handled by 2 intelligent Z80B based controller boards.

Std system configurations include 8 serial synchronous/asynchronous communication ports. All boards plug into the 10-slot backplane of the Z-Bus backplane interconnect (ZBI™). System is available in 2 models, each offering hardware and system software capability for 8 users. Its modular cabinet measures 33 x 19 x 24″ (84 x 48 x 61 cm). **Zilog, Inc,** 10340 Bubb Rd, Cupertino, CA 95014.

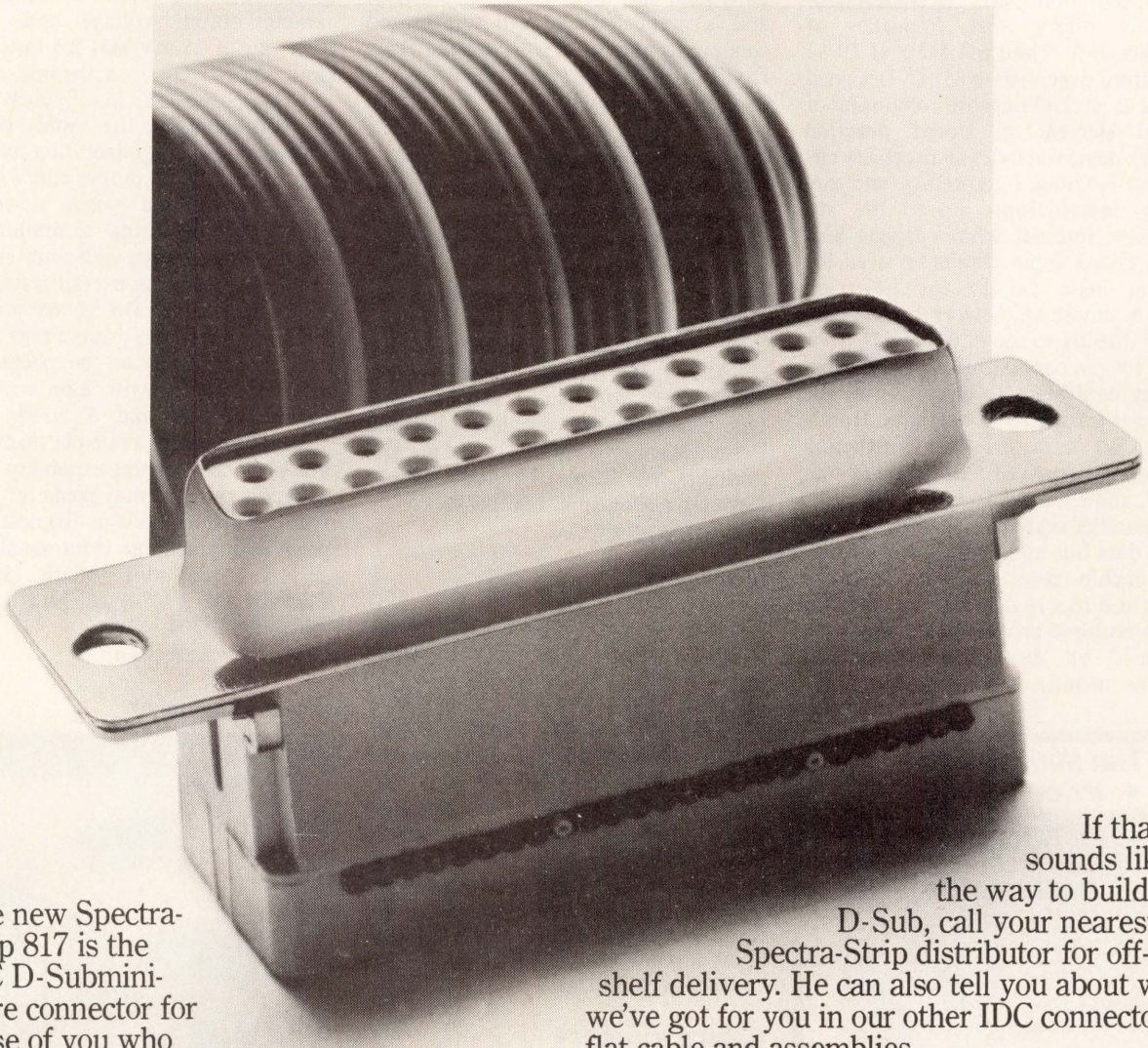
Circle 306 on Inquiry Card

Z80A STD BUS single-board computer

ST4102 uses fuse-link P/ROMs and features a byte-wide 8k-byte memory in EPROM. Three channels of user definable counter/timer functions are provided by a Z80A-CTC; one channel is software programmable as the time base for the RS-232-C port. An AM9519 universal interrupt controller offers management and priority resolution for up to 8 maskable interrupt inputs. Parallel I/O is provided by an I8255A peripheral interface that supplies 24 bits of multiple mode input or output. **Applied Micro Technology, Inc,** PO Box 3042, Tucson, AZ 85702.

Circle 307 on Inquiry Card

D-Suberior



The new Spectra-Strip 817 is the IDC D-Subminiature connector for those of you who have become disenchanted with D-Sub's.

With our D-Sub, you can now mass terminate your flat cables without separating each and every strand. Without stocking up on weird-pitched cable. Without a mechanical kluge tacked onto the back of the connector to go from .054-pitch pins to .050-pitch cable.

It terminates our Twist 'N' Flat,® 3C® Color Coded and that great old standby Spectra-Zip® cables with no fuss, no hassle.

And the Spectra-Strip 817 D-Sub connector comes with a metal shell so that it's *fully* intermateable and intermountable with any of the other real D-Sub's.

If that sounds like the way to build a D-Sub, call your nearest Spectra-Strip distributor for off-the-shelf delivery. He can also tell you about what we've got for you in our other IDC connectors, flat cable and assemblies.

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When you're down to the wire.

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CIRCLE 164 ON INQUIRY CARD

MICROPROCESSORS/ MICROCOMPUTERS

8-bit CMOS microprocessor operates at 3.2 MHz

High speed, 8-bit CMOS CDP1802A microprocessor offers clock frequency of 3.2 MHz at 5 V and 6.4 MHz at 10 V, guaranteed over −40 to 85 °C. Designed for use as general purpose computing or control element in stored program systems, device includes all necessary circuits for fetching, interpreting, and executing instructions stored in std memories. Internal Schmitt trigger buffer on $\overline{\text{CLEAR}}$ input eliminates need for external logic devices for power-on reset. A simple RC network can be connected directly to the $\overline{\text{CLEAR}}$ pin.

Pin for pin compatible with and functionally equivalent to the CDP1802, the processor is capable of operation from 4 to 10.5 V. It features min instruction fetch-execute time of 5 or 7.5 μs at V_{DD} = 5 V, and 2.5 or 3.75 μs at V_{DD} = 10 V; 8-bit parallel organization with bidirectional data bus and multiplexed address bus; onchip DMA; program interrupt mode; and 16 x 16 matrix of registers for use as multiple program counters, data pointers, or data registers. Other features include a single-phase clock, flexible programmed I/O mode, 4 flag inputs directly tested by branch instructions, programmable single-bit output port, and high noise immunity. Processor handles any combination of standard RAM and ROM up to 65,536 bytes and is supplied in 40-lead side brazed ceramic or plastic DIPs. **RCA/Solid State Div,** Rte 202, Somerville, NJ 08876.

Circle 308 on Inquiry Card

MC68000 multibus CPU board

Featuring 256k bytes of onboard RAM that allows its MC68000 CPU to execute code at full speed (8-MHz clock with no wait states), board is compatible with proposed IEEE-P796 at D16M20I16V02L compliance level. Edge connectors for logic analyzer are provided to ease debugging. Bus timeout protection, simple memory protection, and interrupt type selection are provided as well. Peripheral boards for this board are also available. **TSD Display Products, Inc,** 35 Orville Dr, Bohemia, NY 11716.

Circle 309 on Inquiry Card

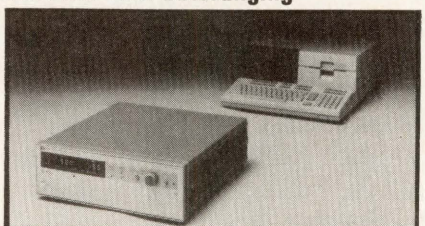
Multibus processor system

8085A based, 5-MHz MC 85 features onboard EPROM (up to 16k x 8), 4k x 8 RAM (CMOS battery backup is available), 48 programmable I/O ports, a keyboard port, an RS-232 port, and a complete monitor on ROM. A dual-ported 2k x 8 memory mapped display controller section features programmable font and either an 80- x 24- or 64- x 16-char matrix. Subsystem also includes 12 levels of vectored interrupts, parallel bus arbitration, and 3 programmable 16-bit counters. **Comark Corp,** 257 Crescent St, Waltham, MA 02154.

Circle 310 on Inquiry Card

POWER SOURCES & PROTECTION

Dc power supply offers bidirectional interface and autoranging

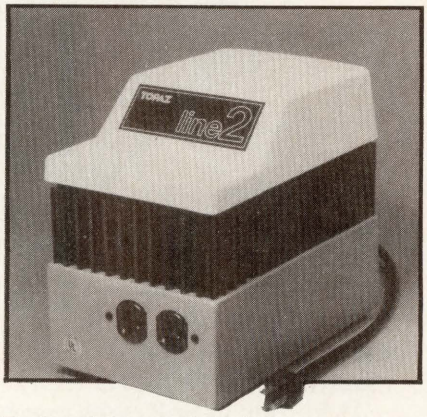


An HP-IB (IEEE-488) dc power supply, the HP 6034A system combines an internal microprocessor based HP-IB programmer with FET switching technology to provide laboratory grade performance specifications and autoranging in a compact, lightweight package. Its microprocessor based HP-IB interface provides bidirectional capabilities and programming format. Firmware allows output voltage and current to be programmed directly in volts and amperes, with 12-bit resolution. The supply provides max output power availability over a wide, continuous range of voltage and current combinations without having to program the output range. It also provides remote output voltage and current metering of 15-mV and 2.5-mA resolution, respectively, over the bus.

Using power FETs in a flyback switching configuration, the supply provides 200-W autoranging operating locus and approximately the output characteristics of 3 conventional system power supplies. This switching technology also provides the system with high electrical efficiency, reducing overall system cooling requirements. For system load protection, supply has overvoltage protection circuit that can be programmed directly in volts, with 8-bit resolution. Service request and 8 power supply status parameters available through the bus provide interrupt capability for improved system management. Other features include built-in diagnostics program and removable front panel for access to calibration board. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304.

Circle 311 on Inquiry Card

Power conditioner



Designed for small business computers, 500-VA Line 2 combines noise suppressing Ultra-Isolator and ac line regulator into single unit. Dual capability enables device to eliminate power related memory loss, program error, system malfunction, and downtime. Device plugs into 120-V outlet, eliminating need for dedicated power line. Unit features low output impedance, 1-cycle response time, and 94% efficiency. **Topaz, Inc, Electronics Div,** 9192 Topaz Way, San Diego, CA 92123.

Circle 312 on Inquiry Card

• The Mini at the
• Price of a Micro



Ardent 10 OEM's, Distributors, Systems Houses-get the performance and flexibility of a MINI, at the economy of a MICRO.

In its basic configuration the Ardent 10 contains 65KB's of a 16 bit computer, disc controller and printer controller, all integrated into a high performance, multivideo level CRT.

The system is capable of handling up to 40MB's of disc storage and printers up to 300 LPM.

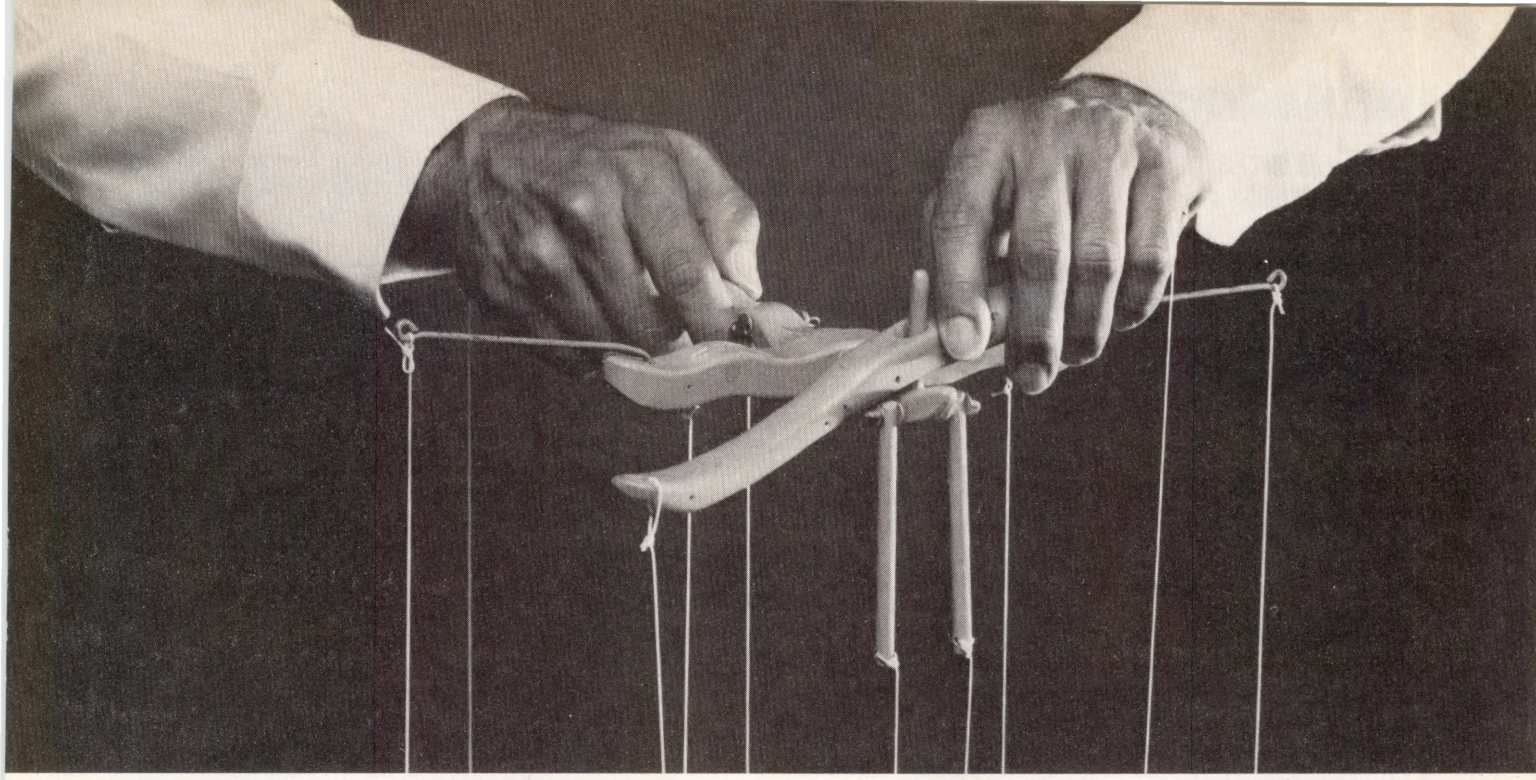
The Ardent commitment is to the OEM, Distributor and Systems Houses. We can work with operating systems supporting BASIC, COBOL or FORTRAN languages.

We have a powerful upgrade package allowing easy, economical growth from a low disc capacity, single user system, up through a hi-storage capacity multiuser system.

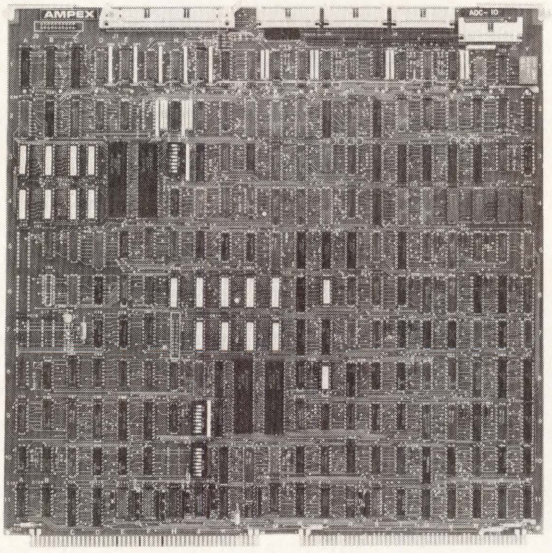
Our discount structure is aggressive, but more importantly, we can help you make money. We're not promising, we're DELIVERING.

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Ampex has a simple solution to your need for either separate disk or multifunction disk/tape controllers. We give you full emulation on a single embedded board.

Result: greater flexibility, lower costs, more control. That's because our new Constellation Series DEC and DG controllers are part of the Ampex "Subsystem" concept. It provides single-source buying for controllers, disk and tape units, so you're assured full compatibility and efficient performance.

DG EMULATION. The ADC-10 and ADC-20 are designed for Data General Nova* and Eclipse* systems. The ADC-10 attaches SMD or CMD disk drives with full emulation. The ADC-20 supports both streaming and start/stop tape drives, as well as attaching SMD disk drives. Dual microprocessor design provides high performance control of all interfaces.

DEC EMULATION. The ADC-11 and ADC-21 are both single-board DEC PDP-11 controllers with the ADC-11 attaching SMD drives with full emulation. The ADC-21 supports both streaming and start/stop tape drives, and also attaches SMD disk drives. Specify our Constellation Series. Control your costs as well as your design.

For more information contact Gary Owen, Ampex Memory Products Division, 200 N. Nash St., El Segundo, CA 90245. (213) 640-0150.

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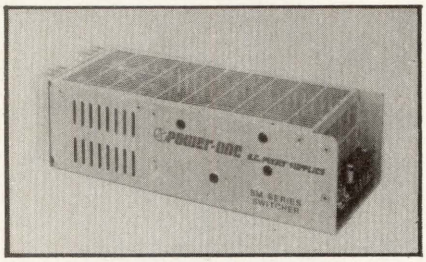
The Designer's Choice.

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CIRCLE 166 ON INQUIRY CARD

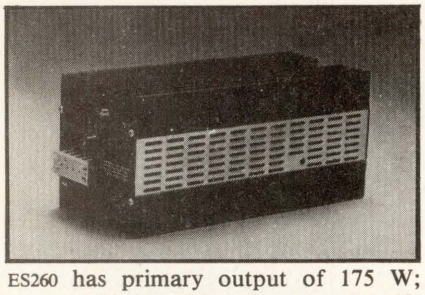
POWER SOURCES & PROTECTION

High frequency switching power supplies



Convection-cooled 400-W SM series provides voltage/current ratings of 5 V at 80 A, 12 V at 33.4 A, 15 V at 26.7 A, 24 V at 16.7 A, and 28 V at 14.3 A. Brownout protection and 20-ms (min) holdup time are std, providing immunity to ac line transients and disturbances. Each model features dual input capabilities of 90 to 130 and 180 to 260 Vac, plus internal rfi/emi filtering. Supplies measure 15 x 4.88 x 3.5″ (38 x 12.40 x 8.9 cm) and weigh 10.5 lb (4.7 kg). **Power-One Inc,** Power One Dr, Camarillo, CA 93010.
Circle 313 on Inquiry Card

4-output switching regulator



ES260 has primary output of 175 W; second, third, and fourth outputs are 48, 24, and 5 W, respectively. Measuring 5.75 x 4.87 x 13.5″ (14.61 x 12.37 x 34.3 cm), the unit is fully rated at 60 °C. Input is selectable at 90 to 130 Vac or 180 to 250 Vac, 47 to 450 Hz. Ripple and noise equal 1% pk-pk or 5 mV, whichever is higher. Overvoltage and reverse voltage protection, and power fail and remote shutdown are std. **Elpac Power Systems, Div of Elpac Electronics, Inc,** 3131 S Standard Ave, Santa Ana, CA 92705.
Circle 314 on Inquiry Card

3-phase, 30-kVA uninterruptible power system

UPS provides clean power that eliminates power outages and disturbances. Features include a static bypass switch with 4-ms fault transfer time; 60-Hz, 120/208-Vac, 3-phase input and output; and 2.5% harmonic sine wave distortion. Output frequency is controlled to ±0.5 Hz and voltage to ±2% of required critical load. The dc bus is floated at 137 Vdc and uses a battery voltage of 120 Vdc. **Clary Corp,** 320 W Clary Ave, San Gabriel, CA 91776.
Circle 237 on Inquiry Card

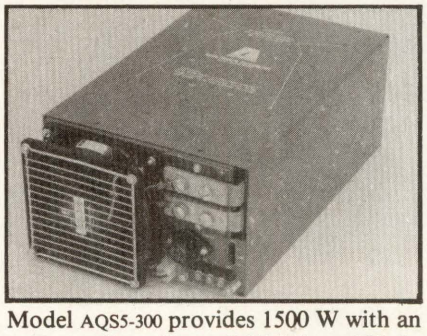
Ac power line conditioners

Six models in DLC series provide clean ac power for computer systems that require a combination of 120 and 240 Vac. The units protect computer system from damage and malfunction due to noise spikes, power surges, voltage sags, and brownouts, and are available in sizes from 3.0 to 20.0 kVA. With input varying by as much as 10 and −20% from nominal, the output will remain constant at the nominal 120 or 240 Vac. Prices start at $1495. **Gould, Inc, Deltec Operation,** 2727 Kurtz St, San Diego, CA 92110.
Circle 315 on Inquiry Card

Voltage surge and transient suppressor

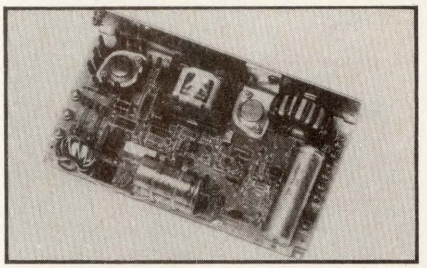
Suppressor plugs into ac line power receptacle on same 15-A breaker circuit as electronic equipment being protected. Solid state semiconductors clip all overvoltage surges beyond 132 Vac, and passive filter network snubs high frequency transients that occur anywhere over full input voltage waveform. A 2-A internal fuse provides safety overload protection. Line power problems that distort ac voltage cause indicator light to shift from amber to a predominantly red or green color, signifying poor quality electrical service. **Cuesta Systems, Inc,** 3440 Roberto Ct, San Luis Obispo, CA 93401.
Circle 316 on Inquiry Card

High power switching power supply



Model AQS5-300 provides 1500 W with an output adjustable to 5.25 Vdc at 300 A. Ac input requirement is a nominal 208/230 Vac, 47 to 63 Hz. The supply maintains full rated power and output voltage regulation to within ±0.2% over an input range of 166 to 264 Vac. Load regulation is ±0.4% for 100% load changes. Output filtering attenuates ripple and noise to 50 mV pk-pk max measured in a dc to 50-MHz bandwidth. Features include built-in adjustable overvoltage and overload protection, and input turn on surge limiting. **Acme Electric Corp,** Cuba, NY 14727.
Circle 317 on Inquiry Card

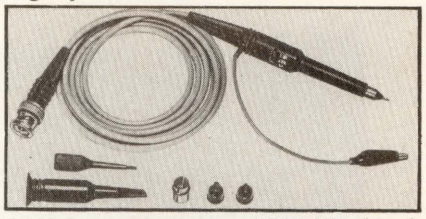
5-V, 10-A switching power supply



Model USB 5-10 open frame supply incorporates Univerter feed-forward, pulse width modulated inverter design that uses only 1 switch transistor. Supply is suited for user selectable line range of 90 to 135 or 180 to 270 Vac and line frequency of 47 to 440 Hz. Efficiency is more than 72% at full load, 115 or 230 Vac and 25 °C. Unit features compensation for up to 0.5-V line drop, output overvoltage protection crowbar fixed at 6.25 ±0.75 V, and output current limitation to 150% or less. **Adtech Power, Inc,** 1621 S Sinclair, Anaheim, CA 92806. Circle 318 on Inquiry Card

TEST & MEASUREMENT

Logic probe



Model 88100 features a 100-MHz bandwidth with a 3-position switch for 1x, 10x, and reference ground. Features include a removable ground lead, compensation adjustment for all scopes, retractable sprung hook, and other accessories. Probe is priced at $39.95. **Probe Master,** 4898 Ronson Ct, Suite B, San Diego, CA 92111.
Circle 319 on Inquiry Card

Floppy disc drive tester/exerciser

Self-contained model 723 FDD features fully automatic test capabilities or manual control of all drive functions for 5.25 and 8″ (13.34- and 20-cm) floppy drives and includes an integral power supply that provides 24, 12, 5, and −5/7.5 V for the drive. Control is provided by a Z80 microprocessor. Six display digits supply information such as test results, track numbers, and error counts, and 22 individual LEDs provide single-bit displays of drive and tester status. **Brikon Inc,** 22981 Alcalde, Laguna Hills, CA 92635.
Circle 320 on Inquiry Card

BOSCHERT. STAYING POWER IN EUROPE.



BOSCHERT NOW OFFERS THE FIRST U.S. SWITCHING POWER SUPPLY TO WIN VDE 0730 CERTIFICATION.

Regulations of the Verband Deutscher Elektronika (VDE) set tough new operating standards for electronic equipment sold in West Germany and most of the rest of Europe. Now Boschert can help you gain VDE approval for your OEM systems in European markets, with the first 200-watt switching power supply to comply fully with VDE 0730 safety specifications and meet VDE 0871 noise requirements.

We're introducing the XL 200-3501—good news for any manufacturer of microcomputer-based systems. This super-efficient switching power supply delivers up to 200 watts of power in a compact, lightweight, field-proven design. Its two jumper-selectable input ranges (95-130V and 190-265V AC), four outputs and cost-effective design make it ideal for word processors, intelligent displays, and the full range of small business computers.

Best of all, our XL 200-3501 is here today!

So remember, if you're marketing systems in Europe today, two things are certain: VDE 0730 is here to stay—and so is Boschert, first with total support for all your power supply needs. From 25 to 1500 watts, from prototype to full production, Boschert leads the way.

For more information on the XL 200-3501 or any of our open frame switchers or submodules, write Boschert Inc., 384 Santa Trinita Ave., Sunnyvale, CA 94086. Or call (408) 732-2440.

Boschert
SWITCHING POWER

CIRCLE 167 ON INQUIRY CARD

MEMORY SYSTEMS

5.25″ Winchester drives offer up to 12.8M-byte storage capacity

Models 1006 and 1012 MiniScribe I Winchester disc drives provide 6.4M and 12.8M bytes of unformatted and 5M and 10M bytes of formatted storage capacity, respectively. Drives are Seagate ST506 interface compatible and feature 5M-bit/s data transfer rate, 8.33-ms average latency, 179-ms average seek time (125-ms software scheduled), 15-ms settling time, and MTBF of 8000 h (continuous operation).

Recording density is 3.46×10^6 bits/in^2 (5.32×10^5/cm^2), claimed to be the highest available for 5.25″ (13.34-cm) Winchester drives using conventional ferrite heads and oxide drives. A rack and pinion motion translator provides for the increased number of recording tracks while retaining the full step holding torque and positioning repeatability characteristics of the stepper motor actuator, ensuring reliable performance at high densities. Positioning repeatability characteristics over the op temp range (4 to 46 °C) are enhanced by a temperature compensation technique. Within the sealed enclosure, a 0.3 μm filter coupled with a breather filter provides a clean operating environment for heads and discs. Reliable operation in electrically noisy environments is achieved with a read channel that uses an IC amplifier in close proximity to the read/write heads. Drives measure 3.25 x 5.75 x 8″ (8.26 x 14.61 x 20 cm) and weigh 5.5 lb (2.5 kg). High volume OEM prices are $745 (model 1006) and $845 (model 1012). **MiniScribe Corp,** 410 S Sunset, Longmont, CO 80501.

Circle 321 on Inquiry Card

Unit provides Winchester mass storage for Intel development systems

Winchester mass storage technology for Intel's Intellec development systems is provided by the MicroSupport™ 3100 mass storage unit; the unit is a special configuration of series 3000 OEM modules compatible at the controller level with Intel standard controllers (iSBC-201, –202, and –206) and disc subsystems (MDS-710, –720, and –740). No software overlays are required, ensuring continuing compatibility with Intellec system improvements or modifications.

The compact, portable system contains a bit-slice controller, 14″ (36-cm) Winchester drive, power supply, cables, and Multibus host adapter board that plugs into Intellec 800, Series II, or Series III systems and provides access to 20M bytes of formatted memory. Recommended system configuration contains an 8″ (20-cm) floppy disc drive that is operator assignable to either single- or double-density modes where media are compatible with Intel diskettes. High level controller can be factory configured to support up to 4 Winchester and 2 floppy drives and provide error checking and error correcting algorithms for reliable operation. **Advant Corp,** 696 Trimble Rd, San Jose, CA 95131.

Circle 322 on Inquiry Card

Disc backup transport

Serpentine operating model 401, specifically designed for Winchester backup, stores up to 17M bytes on a DC-300XL tape cartridge using 6400-bit/in (2520/cm) recording density and 30″ (76-cm)/s tape speed. Transport uses special read after write recording heads that provide bidirectional tape operation to avoid time consuming rewind time. Controller interfaces make transport fully software compatible with DEC's PDP-11 and LSI-11 and Data General's NOVA computers. **Qantex Div, North Atlantic Industries,** 60 Plant Ave, Hauppauge, NY 11788.

Circle 323 on Inquiry Card

5M-byte 5.25″ hard disc system

LS525 incorporates Seagate ST506 5.25″ (13.34-cm) Winchester disc drive, Logical System LDOS disc operating system, Microcomputer Power linear power supply, and the LSI 500 series controller into a rigid disc mass data storage system. Separate offboard host adapter allows unit to be cross-connected to most CPU and bus types. Up to 3 additional Winchester disc drives can be added to the system, with no software modifications required. Compact unit measures 13.5 x 12.0 x 5.25″ (34.3 x 30.5 x 13.34 cm). **Laredo Systems, Inc,** 669 Giraudo Dr, San Jose, CA 95111.

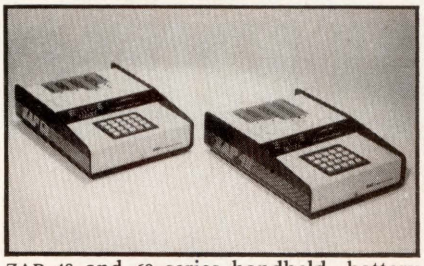
Circle 324 on Inquiry Card

Magnetic tape subsystem

IBM format compatible subsystem, designed for use with all mini- and microcomputers and operating systems, is controlled by host computer through transfer of ASCII codes over RS-232 serial or current loop interface. Subsystem uses dual-density, 9-track, 12.5″ (32-cm)/s tape drive for either 800-char/in (315/cm) NRZI or 1600-char/in (630/cm) P/E, providing more than 40M bytes of storage on a 10.5″ (27-cm) reel. Baud rates are switch-selectable from 110 to 19.2k. **Ibex Computer Corp,** 18730 Oxnard St, Tarzana, CA 91356.

Circle 325 on Inquiry Card

Microprocessor/EPROM/EEPROM programmers



ZAP 48 and 68 series handheld, battery operated units use an 8k x 8 data RAM to program and simulate single voltage EPROMs, EEPROMs, and microprocessors with onboard EPROM. Units have an RS-232 interface, keyboard and terminal editor, and self-prompting display. Functions include move, peek, poke, clear data RAM to state, checksum, list, serial load, serial dump, system test, simulate mode select, verify blank, load P/ROM to data RAM, verify program, program, select P/ROM type, and select baud rate/parity. **Sunrise Electronics,** 524 S Vermont Ave, Glendora, CA 91740.

Circle 326 on Inquiry Card

Multibus dynamic RAM boards feature onboard parity

Boards in Multibus™ dynamic RAM series range in size from 16k to 512k bytes and are compatible with the company's 8- and/or 16-bit single-board computers and existing Multibus RAM boards. Series includes the company's first high density 128k-, 256k-, and 512k-byte boards for Multibus systems.

Based on 16k- and 64k-byte RAM chips, all the boards, with the exception of the 16k-byte version, offer onboard parity. The 32k- through 512k-byte boards generate byte oriented parity during all write operations and perform parity checking during all read operations. When a parity error is detected, boards generate an interrupt on the Multibus interface. Information on the row and bank of the RAM array containing the error is stored in a parity flag register that is accessible as a Multibus I/O port. Onboard LED provides visual indication that a parity error has occurred.

The board's 5-V only design simplifies power supply and battery backup requirements and reduces total power consumption by up to 15%. Prices start at $705 (for the 16k-byte iSBC™ 016A board). **Intel Corp,** 5200 NE Elam Young Pkwy, Hillsboro, OR 97123.

Circle 327 on Inquiry Card

PACIFIC'S DONE-IT AGAIN!

CREATED THE "NEVER OBSOLETE" AC POWER SOURCE

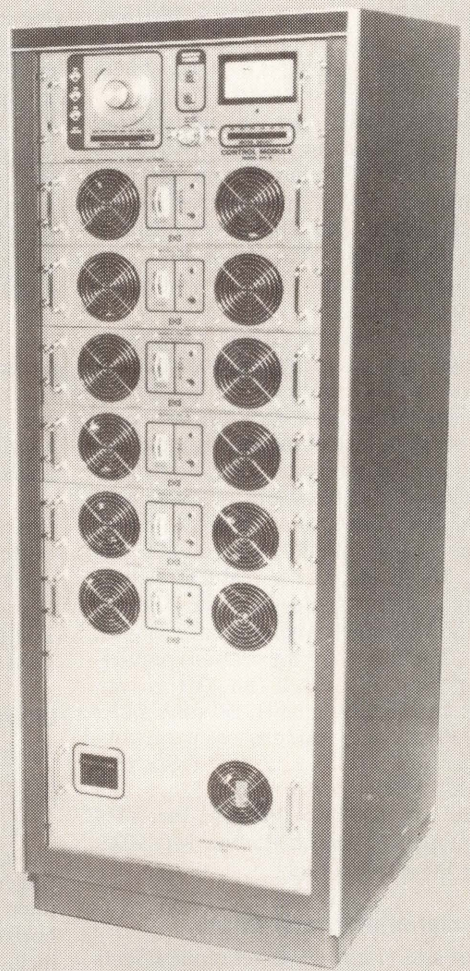
400 Hz Power

Via Pacific "TRUE PARALLELING" capability these variable frequency Solid State AC Power Sources may be USER expanded or reduced in capacity at will.

Each of these three models may be used independently or combined to form high capacity systems. This gives you the ability to have up to a six cabinet 72 KVA 400Hz system one minute, and 6 each 12 KVA 50Hz systems the next.

This type of versatility is what makes these units the "Never OBSOLETE" AC Power Sources.

MODEL 330J-B-7152 (4 KVA 3ϕ 42" High)
MODEL 360J-B-7152 (8 KVA 3ϕ 61" High)
MODEL 390J-B-7152 (12 KVA 3ϕ 78" High)



MODEL 360J-B-7152

CHECK THESE FEATURES

- 70% EFFICIENT and yet utilizes linear amplifiers to form a flawless output wave form.
- SELF-HEALING output stage with self diagnostic circuitry provides fail-safe operation.
- LOW AUDIBLE NOISE allows unit to be located directly in the work area.
- CASTER MOUNTED for easy movement.
- VARIABLE FREQUENCY provides power at any of the popular power frequencies.
- EXTERNAL INPUTS may be driven from transient generator or by remote signal generator.
- 2 YEAR WARRANTY.

50 Hz Power

ASK ABOUT OUR LEASE PLAN

60 Hz Power

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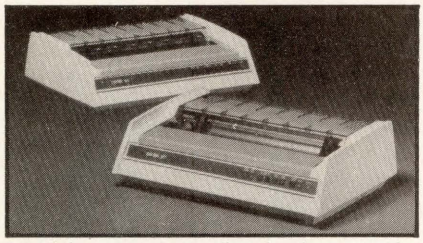
Call direct at (714) 898-2691 or toll free (800) 854-2433 outside CA.

5312 SYSTEMS DRIVE, HUNTINGTON BEACH, CA 92649

CIRCLE 180 ON INQUIRY CARD

PERIPHERALS

Compact, quiet matrix printers feature fast bidirectional printing



Models 910 and 920, first in the 900 series matrix printer line, feature 9 x 9 format, graphics density of 144 x 144 dots/in (57 x 57/cm), 96 ASCII character set with optional fonts, underlining, super/subscript, descenders, double-width characters, and downloadable character set. Line length is 136 col at 10 chars/in (4/cm). Character sizes are 10, 12, 13.3, and 16.7 chars/in (3.9, 4.7, 5.2, and 6.6/cm). Line spacing is 6, 8, 12, and 16 lines/in (2.3, 3.1, 4.7, and 6.3/cm).

Models differ only in bidirectional print speed and throughput. Model 910 prints up to 170 chars/s and has max throughput of 140 lines/min; model 920 prints up to 340 chars/s, with max throughput of 270 lines/min. In graphics, 910 prints 2000 dots/s and 920 prints 4000 dots/s.

Printers handle data processing listings, special forms, and correspondence quality printing. Std equipment includes 1800-char buffers for fully concurrent data receipt during printing; option slots to address future needs and special OEM applications; parallel and serial interfaces; and universal power supply input of 110/115/120/220/240 Vac, 50/60 Hz. Other features include lighted status indicators, easy-change ribbon cartridges, audible alarm signals, no adjustment or lubrication requirements, automatic self-test at turn on, built in diagnostic aids, 60-dBA quiet operation, and modular construction. Dimensions are 23 x 17 x 7″ (58 x 43 x 18 cm). Model 910 is priced at $1695, and model 920, at $2345. **Printek, Inc,** 1517 Townline Rd, Benton Harbor, MI 49022.

Circle 328 on Inquiry Card

Thermal printer mechanisms

PL12M and PL20M are direct replacements for Texas Instruments' EPN 9112 and 9120 thermal printer mechanisms. Electrical requirements are identical, and mechanical parts are an exact match for the TI assemblies. Units are available with ac or dc power supplies and with optional enclosures. **Telpar, Inc,** 4132 Billy Mitchell Rd, Addison, TX 75001.

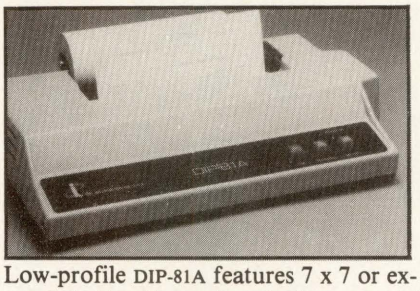
Circle 329 on Inquiry Card

15″ green and amber CRTs

Large screen CRTs have display area 30% larger than std 12″ (30-cm) units, providing significant readability advantage. Designed with 18.6-kHz horizontal video scan rate, terminals offer char resolution nominally 18% higher than conventional terminals. CRTs are available as model 10 (single-page editor), model 11 (APL/ASCII), model 12 (2-page editor), model 14 (extended memory, interactive), and model 100 (132-col with nonvolatile programmable functions). Std 12″ (30-cm) green and amber CRTs are optional on all models. **Teleray Div of Research Inc,** PO Box 24064, Minneapolis, MN 55424.

Circle 330 on Inquiry Card

Dot matrix impact printer



Low-profile DIP-81A features 7 x 7 or expanded 14 x 7 matrix printing, upper/lowercase char set, 100-char/s bidirectional printout, and "finger clean" ribbon cartridge loading. With full 96-char ASCII set, unit prints at 40 or 80 chars/line on 8.5″ (21.6-cm) wide sheet, roll, or fanfold paper. Centronics compatible parallel interface and 10-line buffer are std. Serial RS-232 or 20-mA current loop interface and 2k buffer are optional. **DIP, Inc,** 745 Atlantic Ave, Boston, MA 02111.

Circle 331 on Inquiry Card

Interactive display system

All-In-One IBM 3278 compatible display features high resolution CRT; cabinet that weighs 31 lb (14 kg) and measures 17 x 14 x 16″ (43 x 36 x 40 cm), with detached keyboard; and nonglare, fingerprint resistant screen that can be tilted 25° vertically and rotated 180° horizontally. Std screen sizes supported include 24-line x 80-col, 32-line x 80-col, 43-line x 80-col, and 27-line x 132-col. Special screen sizes that extend display's 132-col viewing capacity include 43-line x 132-col and 66-line x 132-col (full printer page). **Lee Data Corp,** 10206 Crosstown Cir, Minneapolis, MN 55344.

Circle 332 on Inquiry Card

Single-card high density display system

VG 100, designed for S-100 bus systems, has std frequency of 16 MHz (3 to 18 MHz available), 12k bytes of onboard static RAM, 4k bytes of data RAM, 4k bytes of attribute RAM, and 4k bytes of dot RAM. Display chars/line (up to 108) are software selectable. Max number of pixels per raster scan is 768. One to 30 lines can be displayed, under software control. Character field is 8 x 16 and is user definable in a 9 x 16 character space or 144-pixel field. **Echo Communications Corp,** 1708 Stierlin Rd, Mountain View, CA 94043.

Circle 333 on Inquiry Card

SOFTWARE

Machine independent Ada compiler

ADA/M conforms to Attributed Parse Tree (APT) called Diana. Target Machine Description Language (TMDL) provides machine independence so that single compiler source ensures configuration control over multiple implementations on various CPUs. Compiler is targeted to meet MIL-STD-1815 and to be certified by Ada Compiler Validation Facility. **Digital Electronic Systems Inc,** PO Box 5252, Torrance, CA 90510.

Circle 334 on Inquiry Card

Operating system

Switcher Operating System (SOS) provides multiterminal and multiprinter support for Northstar Horizon microcomputer system. It can support different operating systems individually or concurrently. Operating software utilities provided by Northstar DOS or CP/M are supported. System operates using Horizon microcomputer and either Franklin Electric (3 serial ports) or Konan Octoplus (8 serial ports) serial I/O boards. **Valley Forge Software Group,** 406 W DeKalb Pike, King of Prussia, PA 19406.

Circle 335 on Inquiry Card

Modular simulation software

SLAM II™, AID™, and SDL™ are complementary modules designed for use in simulation projects. SLAM II simulation language supports 3 modeling viewpoints in a single integrated framework, while AID is an interactive graphics approach for fitting probability distributions to observed data. SDL is a database management system for use with simulation projects. **Pritsker & Associates, Inc,** PO Box 2413, West Lafayette, IN 47906.

Circle 336 on Inquiry Card

SPEED READER.

125 MHZ A/D'S & D/A'S
SUB-NANOSECOND LOGIC
1/2 NS ECL GATE ARRAYS
APPLICATION NOTES & DATA

A quick read of this new $3.00 paperback is an easy way to get up to speed on ultra-fast data conversion and logic IC's for your computers, speech transmission systems, transient recorders, and radar and video processing electronics.

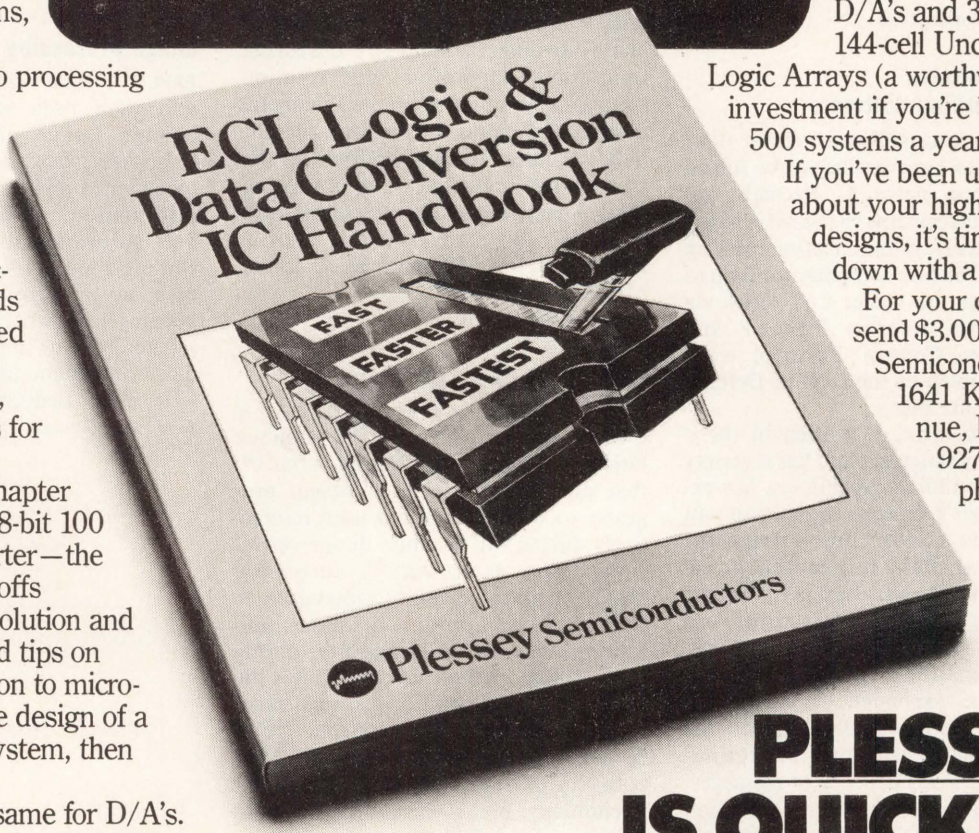
A compendium of application notes, the Plessey reader covers not just design, but practical tips and methods for building advanced real-world systems. And state-of-the-art, subnanosecond IC's for building them.

It opens with a chapter on how to build an 8-bit 100 MHz A to D converter—the methods, the trade-offs between speed, resolution and accuracy, details and tips on comparators. Goes on to micro-strip techniques, the design of a typical ECL A/D system, then covers testing.

Next it does the same for D/A's. And ends on a high note, with detailed specifications on Plessey ECL III products, including standard logic gates, a comparator with a ½-ns set-up time, 125 MHz A/D's, 8-bit D/A's and 36- and 144-cell Uncommitted Logic Arrays (a worthwhile investment if you're building 500 systems a year or more).

If you've been up in the air about your high speed designs, it's time to settle down with a good book.

For your copy, just send $3.00 to Plessey Semiconductors, 1641 Kaiser Avenue, Irvine, CA 92714. Telephone (714) 540-9979.



PLESSEY IS QUICKER.

CIRCLE 169 ON INQUIRY CARD

SOFTWARE

CP/M compatible operating system

Designed for the company's M/NET multiprocessor microcomputers, DBOS features embedded database management system, passwords, file protection, and fast data handling in a multi-user environment. Database management system allows each user to work with entire data bank. Up to 255 hierarchical passwords can be assigned to various users to restrict data access and file add or delete privileges. Compatibility with CP/M provides machine transportability, allowing CP/M based applications programs to run on the company's M/NET systems. **Micromation Inc,** 1620 Montgomery St, San Francisco, CA 94111.

Circle 337 on Inquiry Card

Display management system

System cuts time needed to create color graphic screen displays and does not require knowledge of a programming language. User paints a picture using cursor control keys, color pad, and special function keys. When screen is complete, it is saved on disc and can be recalled at will. Up to 18 displays can be saved in single disc file. Average displays are created in less than 30 min and require from 20 to 1700 bytes of memory. **Intelligent Systems Corp,** Intecolor Dr, 225 Technology Pk/Atlanta, Norcross, GA 30092.

Circle 338 on Inquiry Card

Enhancements to UNIX networking software

UNET networking software allows UNIX based small to large systems to be joined in a common network. Recently announced enhancements to the networking software extend communication rates up to 100k bits for DEC computers and up to 200k bits for the Cyber CDC series via HYPERchannel. Internet Protocol and Transmission Control Protocol standards as adopted by the Dept of Defense in Jan 1980 are met.

UNET, like UNIX, is written in the C programming language and has a variety of network building capabilities. For example, a user's remote connection can appear to be a direct one through the software's capability to establish virtual terminals. Another feature is automatic route through, using store and forward procedures to provide services transparently. Remote file transfer is offered, enabling the exchange of ASCII and binary files between computers in the network. Mail transfer provides for immediate or queued delivery of messages. Process to process communication routines permit full-duplex communication between application programs on various remote computers. A datagram service is available for implementing user-defined protocols. **3COM Corp,** 1390 Shorebird Way, Mountain View, CA 94043.

Circle 339 on Inquiry Card

Realtime executive

Designed for iAPX-86/88 processor systems, REX-80/86 provides core functions including intertask synchronization, asynchronous event coordination, interrupt handling, and memory management. Additional facilities such as time based synchronization can be added from the system macro library. Programs can be developed in high level languages such as PL/M or C. Compatible with most major development systems, including Intel MDS, GenRad 2300, Tektronix 8002, and DEC PDP-11 (with cross assemblers), the system requires less than 4k bytes of ROM and 512 bytes of RAM, a realtime clock, and a priority interrupt controller. **Systems & Software, Inc,** 2801 Finley Rd, Suite 101, Downers Grove, IL 60515.

Circle 340 on Inquiry Card

Modular CAD/CAM software

AD-2000 consists of set of interactive graphics procedures plus GRAPL written language. Interactive graphics set makes CRT terminal a drawing board of any size. Automatic drafting procedures include scaling, zooming, mirroring, translation, duplication, and rotation. GRAPL enables user to prepare geometric designs and permits generation of same data structure, in a written form, as that created by interactive graphics definitions. Design created in interactive mode can also be converted to GRAPL. **Honeywell, Inc,** 200 Smith St, Waltham, MA 02154.

Circle 341 on Inquiry Card

CAD/CAM software package

IDS-80 version 2 software for the IDS-80 CAD/CAM system features the Graphics Oriented Language for Design (GOLD™) that allows user prepared design programs to be installed and used interactively during full graphics design operations. The AUTOPART™ automatic family-of-parts capability allows users to parameterize families of parts and family-based part modeling jobs during the routine design cycle, while the AUTOPATH™ capability permits automatic placement of electronic components and automatic routing of circuit paths in PCB design. **Gerber Systems Technology, Inc,** 40 Gerber Rd E, South Windsor, CT 06074.

Circle 342 on Inquiry Card

Multipass Pascal compiler

Designed for Data General computers, compiler conforms to the proposed ANSI std and features 117 error messages and a compilation speed of over 400 lines/min. Generated code is claimed to execute twice as fast as that produced by Data General's FORTRAN IV compiler. The compiler's final pass automatically links executable code to the Pascal support library, directly creating an executable file and saving the time required to manually perform the linking operation. Device compiles 4000-line programs in less than 32k words of memory. **Rhintek, Inc,** PO Box 220, Columbia, MD 21045.

Circle 343 on Inquiry Card

Ada compiler

TeleSoft-Ada™ compiler performs full Ada syntax checking and produces code for all but the most complex features of the language. It produces an intermediate code that can be translated or interpreted to execute on new processors with a minimum of modification. The compiler supports packages, tasks, exceptions, identifier overloading, and separate compilation (with limitations). **TeleSoft,** 10639 Roselle St, San Diego, CA 92121.

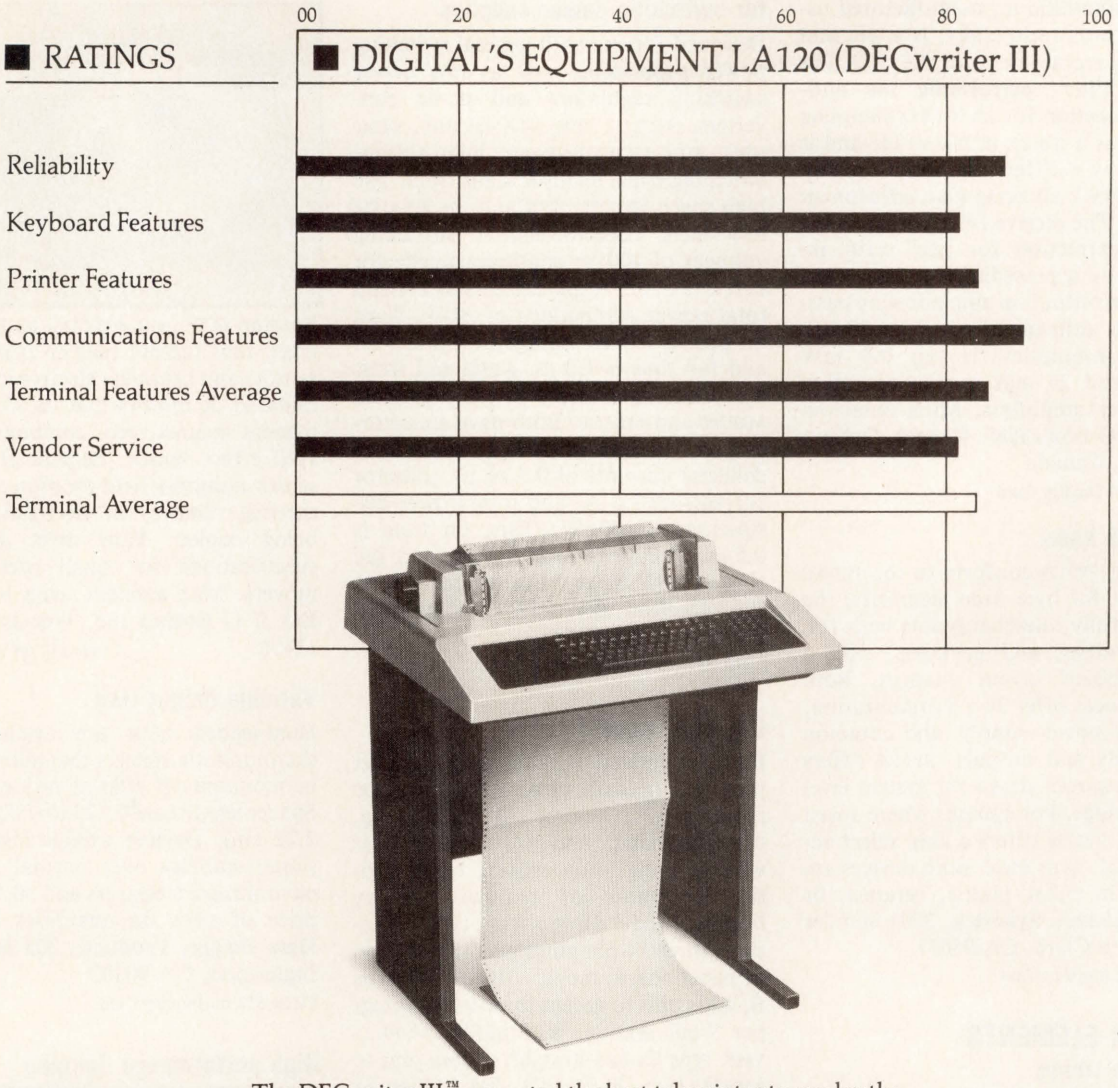
Circle 344 on Inquiry Card

Image processing system

EPPL™ displays images on TV monitors and then uses software features to change image contrast, color and brightness; to extract pertinent data; and to enhance images to illustrate specific information. The system consists of both software and related hardware, including a DEC PDP-11 computer plus the company's image digitizing and display systems, laser writers, and hardcopy output equipment. Image data are stored on disc or magnetic tape. **Eikonix Corp,** 23 Crosby Dr, Bedford, MA 01730.

Circle 345 on Inquiry Card

DECwriter III users are happier.



The DECwriter III™ was rated the best teleprinter to use by the people who use it.*

It was rated particularly high in ease-of-use categories and in reliability.

We point this out not only to call attention to our high-throughput, 1200-baud DECwriter III, but also to mention Digital's long-standing commitment to products that work well for people.

You see, we believe people work better when they're given tools that work better.

To buy a DECwriter III, contact your local terminals dealer. For the name of the one nearest you, call (800) 225-9378 (outside the Continental U.S. and in Massachusetts call (617) 467-7068) between 8:30am and 5:00pm Eastern time, or contact your local Digital sales representative.

Digital Equipment Corporation, Terminals Product Group, MR2-2/M67, One Iron Way, Marlboro, MA 01752. Tel. (617) 467-7068. In Europe: 12 Av. des Morgines, CH-1213 Petit-Lancy/Geneva. In Canada: Digital Equipment of Canada, Ltd.

*According to Data Decisions, Inc. For a copy of the survey entitled "Interactive Terminal Ratings," write to Data Decisions, Inc., 20 Brace Road, Cherry Hill, New Jersey 08034.

digital

We change the way people work.

CIRCLE 170 ON INQUIRY CARD

INTEGRATED CIRCUITS

PCM transmit/receive filters

MT8912 monolithic IC, manufactured using ISO² CMOS technology, is a pin and functional replacement for the 12912. The transmit filter, performing the anti-aliasing function for an 8-kHz sampling system, has a notch at 50/60 Hz and is preceded by a differential input op amp with feedback allowing gain adjustment of 20 dB. The receive filter performs the sin x/x correction for gain error introduced by a preceding D-A converter, and has an output op amp allowing passband gain adjustment of up to 20 dB. Power consumption is typ 0.4 mW standby and 25 mW during operation with driver amplifiers. **Mitel Semiconductor**, PO Box 13089, Kanata, Ontario K2K 1X3, Canada.

Circle 346 on Inquiry Card

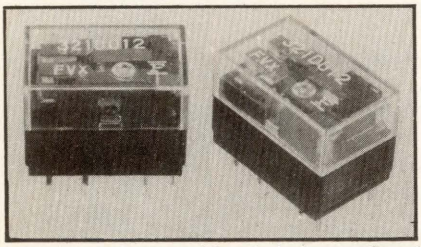
16k static RAMs

SY2128 and SY2129 conform to the JEDEC std pinout for byte wide memories; the units are fully interchangeable with 16k ROMs, EPROMs, and EEPROMs, with a min of board layout changes. Both 24-pin devices offer 2k x 8 organization, single 5-V power supply, and common data inputs and outputs. SY2128 offers automatic power down for system level power savings. For systems where speed is critical, SY2129 offers a chip select access time of 50 ns max. Both devices are available in either plastic, ceramic, or cerdip packages. **Synertek**, 3001 Stender Way, Santa Clara, CA 95051.

Circle 347 on Inquiry Card

SYSTEM ELEMENTS

Miniature relays



FBR 311 series provides 3-A (or optional 5-A) rating spdt contacts for PCBs, while FBR 321 series provides 3-A rating dpdt contacts. Both feature high density mounting, flux contamination immunity, and versatile switching performance from signal level to handling 3 A. Contact ratings are 3 A at 28 Vdc, resistive, and 3 A at 120 Vac, resistive. Initial contact resistance is 100 mΩ max at 6 Vdc, 0.5 A. Rated coil voltages are 5, 6, 9, 12, and 24 Vdc. **Fujitsu America, Inc, Component Div**, 910 Sherwood Dr-23, Lake Bluff, IL 60044.

Circle 348 on Inquiry Card

Power transistors for switching power supplies

Designed for use with general switching power supplies as well as low power switching regulators and dc-dc converters, NTC2752 NPN, NTA1156 PNP, NT340 NPN, and NT350 PNP are high voltage switching triple diffused transistors. The high speed NTC2752 NPN and the NTA1156 PNP have collector-emitter sustaining voltages of 400 V; continuous collector currents of 0.5 A; pk currents of 1 A and total power dissipations of 20 W. Turn on time is 1.0 μs, storage time is 2.5 μs, and fall time is 1.0 μs. NT340 and NT350 are direct equivalents to the Motorola MJE340 and MJE350. Both have collector-emitter voltages of 300 V; continuous collector currents of 0.5 A; pk collector currents of 1.0 A; and total power dissipations of 20 W. Turn on time is 0.5 μs, storage time is 2.3 μs, and fall time is 0.35 μs. **NEC Electronics U.S.A. Inc, Electron Div**, 252 Humboldt Ct, Sunnyvale, CA 94086.

Circle 349 on Inquiry Card

Universal panel boards

Fully populated with SP series socket pins and manufactured to MIL-P-55110C requirements, boards offer mounting, DIP placement, and pin locations for wirewrapping using existing tapes identical to those of popular industry boards. Model 4-UPB-A-VHF, type A, accepts three 14-pin plugs per 9-col section of panel board; model 4-UPB-B-VHF, type B, adds pins to accept three 28-pin plugs per 9-col section; and model 4-UPB-C-VHF, type C, has straight, square pins to accept two 40-contact flat cables or similar connectors with contacts having 0.100″ (0.254-cm) spacing per 9-col section. **Hybricon Corp**, 410 Great Rd, Littleton, MA 01460.

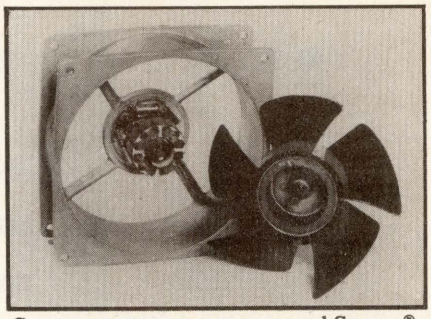
Circle 350 on Inquiry Card

Fallback switch modules

Analog, coaxial, and digital switching capabilities are provided by FBM-2 series switches. Units offer means of manually switching data lines between active and fallback or alternate positions, permitting user to shift circuit to alternate computer port or terminal in event of primary equipment failure in data communication network. Models are offered with digital RS-232/V.24; 4-wire analog; 2-wire coaxial; or 2-channel, 2-wire coaxial interface connections. **Atlantic Research Corp**, 5390 Cherokee Ave, Alexandria, VA 22314.

Circle 351 on Inquiry Card

Brushless fans



Spartan ECDC, MIL 80 ECDC, and Saucer® ECDC fans feature built-in performance sensors and brushless electronically commutated dc motors that use ferrite permanent magnet rotor commutated by a Hall effect sensor. Second Hall effect sensor monitors field rotation to prevent thermal runaway in electronics system being cooled. Fans meet MIL-B-23071 specifications for small precision air movers. Max ambient temp is 100 °C. **EG & G Rotron Inc**, Woodstock, NY 12498.

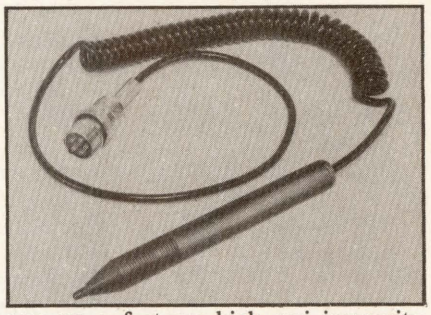
Circle 352 on Inquiry Card

Variable height LEDs

Dual-leaded LEDs are available with thermoplastic spacers that allow them to be mounted off PCBs at various heights. Spacer lengths are 0.125 to 0.875 (0.32 to 2.22 cm). Devices exhibit high dimensional stability over normal operating environments. Spacers add $0.10 each to price of LEDs (in quantities of 5000). **Data Display Products**, 303 N Oak St, Inglewood, CA 90302.

Circle 353 on Inquiry Card

High performance lightpen

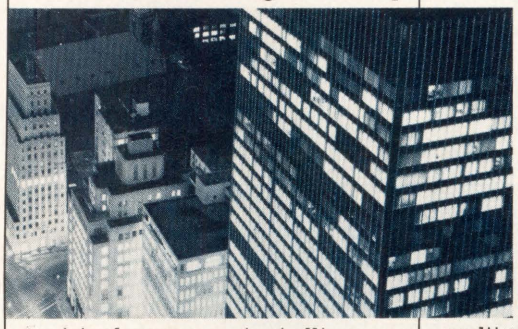


LTP 105 A features high emi immunity and max scan rate responses up to 5000 cm/ms typ. Lightspot size and optical field of view are 0.01 and 0.080 to 0.160″ (0.03 and 0.2 to 0.4 cm), respectively. Optical switching eliminates mechanical switching and contact bounce. Lightpen is activated by depressing push tip against CRT screen. Single 5-Vdc power supply is required. **Photobell Co Inc, Sub of Ampower Instrument Co, Inc**, 26 Just Rd, Fairfield, NJ 07006.

Circle 354 on Inquiry Card

When the Canadian Government needed a totally secure local data distribution network, they ordered our Fiber Optic System.

The data distribution Problem: The Canadian Government made their problem completely clear. One of their agencies was expanding its headquarters into several floors of an adjacent office building and they insisted upon installing a secure local data distribution network to carry "sensitive" traffic. Minimal start-up costs and future expandability were further considerations.



The Fiber Optic Solution: Versitron's System Design Group studied the problem and recommended a fiber optic network utilizing advanced fiber optic modems. This recommendation assured total traffic security throughout the network. Not only because of fiber optic's inherent physical protection, but also through a unique intrusion alarm feature that immediately shuts down any data link where the integrity is suspect. The start-up cost for this system proved to be highly competitive with an equivalent coaxial system. Plus, the fiber optic system's capacity could be expanded by a factor of fifteen by merely replacing the single channel modem with Versitron's 15 channel multiplexer system.

The Final Outcome: The Canadian Government was impressed. They ordered the fiber optic system and, in one stroke, met all of their requirements for security, cost, and expandability.

The lesson learned here is applicable to a large range of data distribution situations. Let Versitron's System Design Group assist you on your next project. Call us at (202) 882-8464. Or write to: 6310 Chillum Place N.W., Washington, D.C. 20011.

VERSITRON, INC.

CIRCLE 171 ON INQUIRY CARD

SYSTEM ELEMENTS

GaAs LED infrared emitter

LD-271, housed in a T-1¾ dark plastic package, is offered in 3 radiant intensity groups: LD-271A<7, LD-271<10, and LD-271H<16 mW/sr at 100 mA with half angle of 25 degrees. Pin photodiodes are designated SFH-205 (sensitive on rounded side) and SFH-206 (sensitive on flat side) with black encapsulated packages that serve as a filter and are transparent to infrared emission. Leads are spaced at 0.1″ (2.54 mm) and devices can be vertically mounted on PCBs. **Litronix, Inc,** 19000 Homestead Rd, Cupertino, CA 95014.

Circle 355 on Inquiry Card

Sensitive snap-in pushbutton switches

PS14, PS15, PS16, and PS17 type switches feature snap-in mounting in both spdt and dpdt circuit configurations. Both solder lug and PC terminal versions offer ratings of 5 A for single-pole circuits and 1 A for double-pole circuits at 120 Vac or Vdc. Switches with 1- and 5-A ratings have std contact construction of silver with gold flash for solderability. Epoxy sealing covers all terminals. **Eaton Corp, Cutler-Hammer Products,** 4201 N 27th St, Milwaukee, WI 53216.

Circle 356 on Inquiry Card

Subminiature precision snap action switch

Cost-reduced type 16 switch, featuring simplified contact design, replaces individual stationary contacts with silver inlay on terminals. Movable contacts are identical to existing type 16 switches. Switch is rated at 5 A, 125 Vac. Both 0.110″ (0.279-cm) quick disconnect and PC terminals are std. Options are available on custom basis. **Licon, Div of Illinois Tool Works Inc,** 6615 W Irving Park Rd, Chicago, IL 60634.

Circle 357 on Inquiry Card

2-axis encoding system

MicroSeries μS6.4k/16 receives inputs (azimuth and elevation) from 2 optical encoders. Upon an input command, the system converts the encoder outputs into 2 BCD words. Words are given in units of mils (6400 mils equal 360 degrees). Other codes can be provided with slight hardware/software modifications. Encoders are available in 1.6 and 2.3″ (4.1- and 5.8-cm) OD sizes and offer resolutions up to 16 bits. **Itek Measurement Systems Div,** 27 Christina St, Newton, MA 02161.

Circle 358 on Inquiry Card

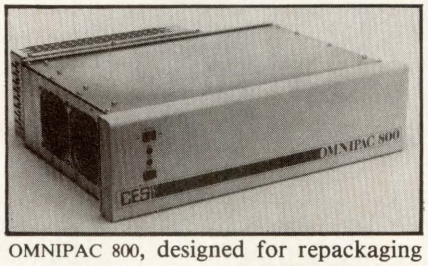
Super miniature aluminum electrolytic capacitors

PDS series radial lead capacitors are available in 15 packages ranging from 0.160″ dia x 0.295″ length (0.406 x 0.749 cm) to 0.630″ dia x 0.827″ length (1.6 x 2.1 cm). Voltage range is 6.3 to 50 Vdc; capacitance range is 0.1 to 2200 μF. Leakage current is rated at I = 0.01 CV or 3 μA, whichever is greater, and op temp range is −40 to 85 °C. Prices start at less than $0.10 each (production quantities). **International Components Corp, OEM Div,** 105 Maxess Rd, Melville, NY 11747.

Circle 359 on Inquiry Card

INTERCONNECTION & PACKAGING

Computer chassis



OMNIPAC 800, designed for repackaging PDP-8 systems, is compatible with KK8A and KK8E CPUs and all OMNIBUS control boards. It offers 9 hex-wide slots, positive ventilation, a limited function front panel, and a switching power supply in a std 19 x 5.25″ (48 x 13.34-cm) chassis. The unit also functions as an expansion chassis for PDP-8 computers, allowing upgrading to 128k-word memory using the KT8A memory management unit and adding RL01 or RL02 disc controllers or other hex-wide option boards. **Computer Extension Systems, Inc,** 17511 El Camino Real, Houston, TX 77058.

Circle 360 on Inquiry Card

Card-edge connectors

Series CT connectors have 0.045″ (0.114-cm) sq contact tails on 0.156 x 0.188″ (0.396 x 0.478-cm) centers. Selectively plated with 0.00003″ (0.00076-mm) gold, the bifurcated cantilever contacts offer high performance and protection of critical surfaces during repeated board insertions. Contact tails are suitable for wirewrapping or solderless connections. Connectors are available in std sizes, including right angle and straight types. **Eby Co,** 4701 Germantown Ave, Philadelphia, PA 19144.

Circle 361 on Inquiry Card

DEVELOPMENT SYSTEMS

Universal microprocessor development system

UMDS-50 supports up to 20 users and 35 different microprocessors and includes high speed 16-bit CPU (11/44), memory management unit, cache memory, dual 10M-byte discs, 256k bytes of memory, and 16 serial ports. Software includes the company's microprocessor development software and DEC's RSX-11M operating system, editor, and other utilities. Development software is user accessible and operates entirely within user's memory space. **Boston Systems Office,** 469 Moody St, Waltham, MA 02154.

Circle 362 on Inquiry Card

CMOS microprocessor development system

Z1802 utilizes a 64k microcomputer running under CP/M, a fast relocatable cross assembler, a full screen editor, and a linker to speed software development. A symbolic logic analyzer uses the symbol table created by the cross assembler to supply symbolic addresses within the logic code, eliminating manual address referencing. Additional trace search and comparison features ease trace analysis. For hardware independent software development, a software emulator displays register, memory, and CPU state values with a multiple sequence nested breakpoint structure. **Scientific Development Technologies, Inc,** Naperville, IL 60566.

Circle 363 on Inquiry Card

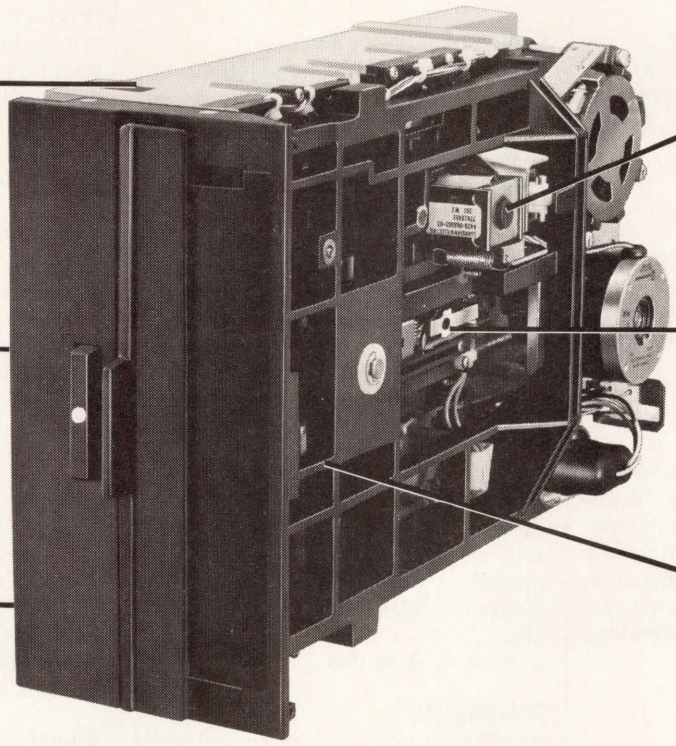
8-station multi-user development system for Z8000

Full hardware and software support for the Z8000, including slave emulation and a Pascal compiler, is now offered on the GenRad DSD single/multi-user development system. Software support is available with a Pascal compiler for the 68000. Full hardware support with slave emulation is also available for the 6809. The 8086 can also be supported with software and hardware.

Individual stations consist of a console and optional peripherals such as local mass storage (hard or floppy disc), a printer, a P/ROM programmer, and up to eight slave emulators for simultaneous, multiple processor development. All users share a common data base stored on hard disc. **GenRad, Development Systems Div,** 5730 Buckingham Pkwy, Culver City, CA 90230.

Circle 364 on Inquiry Card

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The OEM industry has always needed an 8" double-sided flexible disk drive. But not the problems that were associated with it, like excessive media wear. Noise. Or big power requirements.

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We make a complete family of 8" and 5¼" floppy drives, and they're all ready for delivery. So call your ARROW or KIERULFF distributor, your Control Data rep, or our OEM Product Sales people in Oklahoma City. 405/324-3160.

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LITERATURE

Plastic capacitors
Technical bulletin describes miniature and microminiature devices, detailing pros and cons of metallized film and ceramic units in microelectronic applications. **Inter-Technical Group, Inc,** Irvington, NY.
Circle 365 on Inquiry Card

Power line noise suppression
Reference manual for protection of sensitive electronic equipment provides technical data and applications. **Topaz, Inc,** San Diego, Calif.
Circle 366 on Inquiry Card

Video monitors
Color and monochrome image processing and display systems are profiled in brochure that contains photos and electrical/mechanical specs. **DeAnza Systems Inc,** San Jose, Calif.
Circle 367 on Inquiry Card

CAD/CAM software
Brochure presents ANVIL-4000™ packages for automated design, drafting, and manufacturing; full-color computer generated graphics illustrate view/scale and geometric elements, manipulation, and applications. **Manufacturing and Consulting Services, Inc,** Santa Ana, Calif.
Circle 368 on Inquiry Card

Stepper motors
Specs and test data are detailed in 48-p catalog that features performance curves, nomographs, and dimensional drawings. **Bodine Electric Co,** Chicago, Ill.
Circle 369 on Inquiry Card

Insulation displacement connectors
Product spec guide, illustrated with photos, diagrams, charts, and engineering drawings, covers IDC and flat cable design, installation, and operation. **CW Industries,** Southampton, Pa.
Circle 370 on Inquiry Card

Trimming potentiometers
Wirebound and cermet trimmers and resistors are subject of 76-p catalog providing specs, circuit diagrams, applications, and selection guide for commercial and military users. **Bourns, Inc, Trimpot Div,** Riverside, Calif.
Circle 371 on Inquiry Card

Voice response technology
Handbook discusses increased productivity and reduced errors in data entry, and contains glossary and applications information. **Perception Technology Corp,** Winchester, Mass.
Circle 372 on Inquiry Card

Power sources and switchers
Featured in engineering guide are test and application techniques, ac-dc and dc-dc selection guides, performance criteria, electrical and mechanical specs, options, and glossary. **Semiconductor Circuits, Inc,** Windham, NH.
Circle 373 on Inquiry Card

Communications and telecommunications terminology
Glossary defines nearly 900 terms and acronyms at semi-technical level. **Computer Communications Group,** Ottawa, Ontario, Canada.
Circle 374 on Inquiry Card

Switching power supplies
Ac-dc, dc-dc, linear open frame, and ferroresonant supplies are highlighted in handbook listing performance characteristics, in addition to common, mechanical, and electrical specs. **Acme Electric Corp,** Cuba, NY.
Circle 375 on Inquiry Card

Test systems
Brochures feature 179X functional and 2270 in-circuit systems, presenting photos, specs, and architectural diagrams. **GenRad, Inc,** Waltham, Mass.
Circle 376 on Inquiry Card

Filtering EMI
Application note explains emi/rfi terms and energy emission modes; 65000A decoupling, signal and power routing, and shielding and filtering; and how to meet VDE and FCC requirements. **Hewlett-Packard Co,** Palo Alto, Calif.
Circle 377 on Inquiry Card

Network software
Software tools used in the design and management of networks are described in 32-p publication. **Network Analysis Corp,** Great Neck, NY.
Circle 378 on Inquiry Card

EEPROM applications
Handbook discusses operation of 16k-bit 21816, and shows ways to interface it to microprocessor and program it from 5-V power supply. Request E²PROM Family Applications Handbook in writing from **Intel Corp,** Literature Dept SV3-3, 3065 Bowers Ave, Santa Clara, CA 95051, or call 408/734-8102.
Circle 379 on Inquiry Card

Remote analog and digital I/O
Booklet presents SL-800/800M intelligent serial units, outlining applications and specs. **Serial Lab Products Inc,** Marlboro, Mass.
Circle 380 on Inquiry Card

EMI shielding spray
Brochure details how to cope with new FCC requirements by using Enforcer™, a group of sprayable electrically conductive acrylic coatings that provide emi shielding for plastics. **Chomerics, Inc,** Woburn, Mass.
Circle 381 on Inquiry Card

Communications systems and network integration
Booklet shows how co's data communications products can be connected to build networks, and describes configuration for network-wide management and fault control. **Timeplex, Inc,** Rochelle Park, NJ.
Circle 382 on Inquiry Card

Stepper and synchronous motors
Presented in 4-p catalog are illustrations and specs for AMY series of synchronous motors, AMA series of steppers, SAA series of ICs, and five types of snap-on, interchangeable reduction gears. **Landis & Gyr, Inc,** Elmsford, NY.
Circle 383 on Inquiry Card

Power supplies
Catalog/handbook contains descriptions, specs, and dimensional drawings for linear, ferroresonant, and switching modules, as well as applications and glossary. **Kepco Inc,** Flushing, NY.
Circle 384 on Inquiry Card

Linear ICs
Cross-reference chart, features, and specs are found in catalog that describes DACs, ADCs, voltage references, op amps, analog multiplexers and switches, military ICs, and custom LSI. **Micro Power Systems, Inc,** Santa Clara, Calif.
Circle 385 on Inquiry Card

Microcomputer software
Catalog summarizes 6800/6809 products for single-, multi-user, and network operating systems. **Software Dynamics,** Anaheim, Calif.
Circle 386 on Inquiry Card

LED circuit board indicators
Photos, dimensional drawings, and selector chart are included in short form catalog that highlights red, green, and yellow LEDs, QUAD-LED™ 4-element arrays, and bicolor. **Dialight,** Brooklyn, NY.
Circle 387 on Inquiry Card

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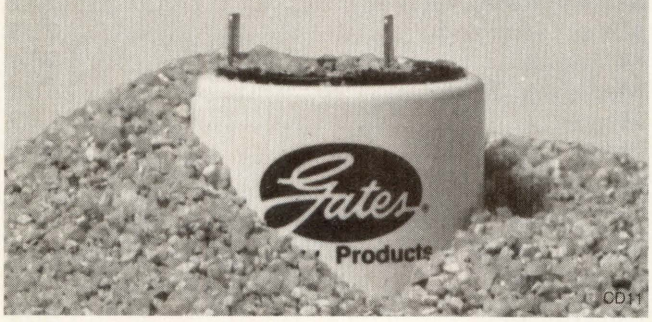
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CIRCLE 172 ON INQUIRY CARD

HIGH INTEREST IN CAREER GROWTH— But Concern with Lifestyle

Careful Evaluation of Company Choice

Recently, COMPUTER DESIGN sent out a series of questionnaires to selected groups of our readers entitled "Career Growth/Personal Objectives Survey". The purpose of this study was to give engineers, throughout the country, the opportunity to express their perceptions and opinions about their careers, and future career paths. Additionally, we wanted to determine their views about the leading employers of systems designers within the industry.

One thousand questionnaires were sent out to each of the four major design groups within our audience. The areas surveyed included: General Design, Software Design, CAD/CAM and Data Communications. Within one week COMPUTER DESIGN received over 550 completed responses. Within three weeks the return rate was close to one thousand. To those of you who completed and returned a questionnaire, we wish to take this opportunity to thank you for the time invested in this detailed survey.

The remarkable success of this survey demonstrated to us your strong interest in the future of the industry. Also, it highlighted your eagerness to help change or alter some of the factors which have a major effect on your lifestyle and career growth. The importance of surveys like this cannot be underestimated in the effect they will have on the entire industry. The opinions expressed could likely change the way major companies structure their programs and benefits to attract top design talents for years to come.

COMPUTER DESIGN is presently compiling and tabulating the vast amount of data we have received. Beginning with the December issue we will be reporting, in this section, some of the more important conclusions of this study.

This survey is another significant part of our continuing commitment to our readers. Information of this type is vital to helping major corporations better structure programs to attract you. As a result of your input, these companies will now have a clearer understanding of how the leading systems designers perceive them as a potential employer.

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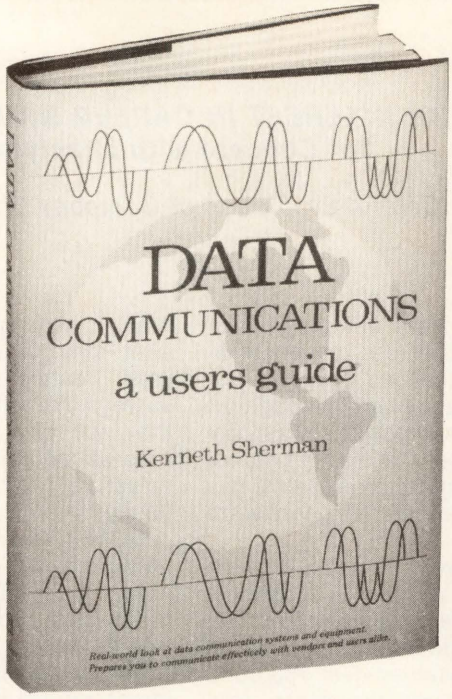
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348 pages; 95 illustrations; Reston Publishing Company Inc; $21.95. 1981.
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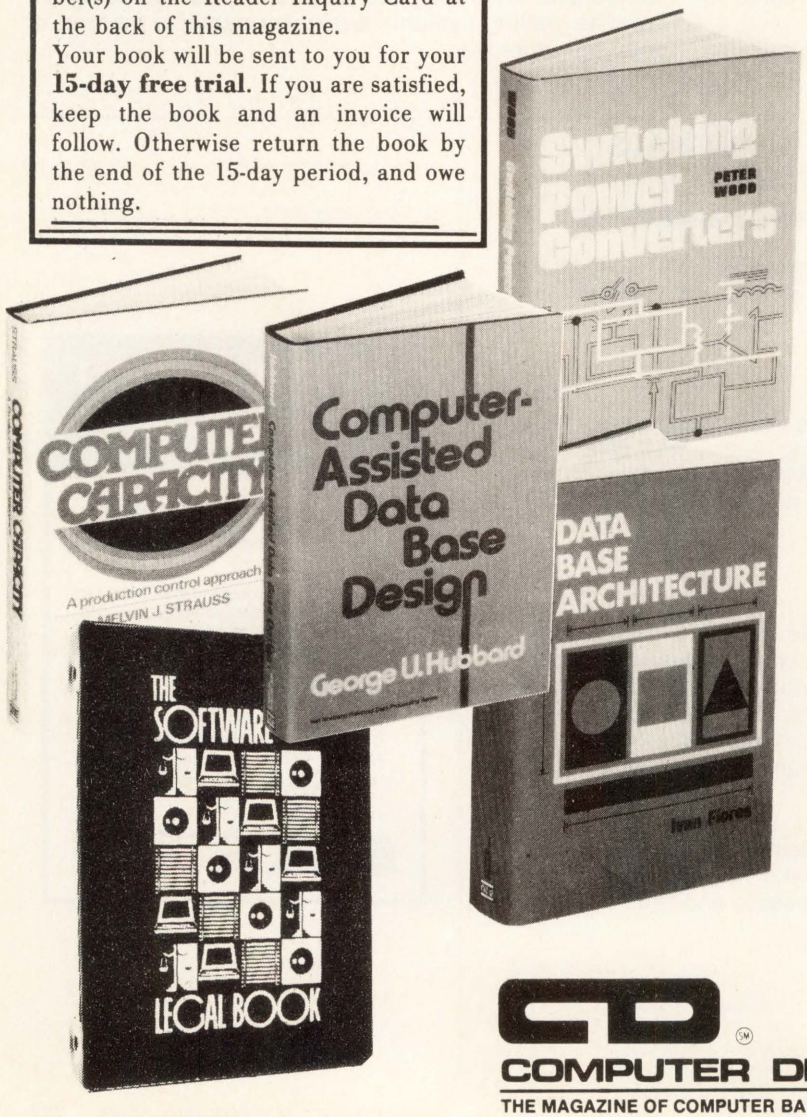


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280 pages; 6 x 9; 128 illustrations; Van Nostrand Reinhold; $24.95. July, 1981.
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Data Base Architecture by *Ivan Flores, Ph.D.*

This is the definitive guide to data base organization, giving the answers to the why's and how's. It describes the structure and use of information organized into a data base, and how application programs, data structures, data base management systems (DBMS), the operating system, and hardware relate to each data base organization.

408 pages; 295 illustrations; 6 x 9; Van Nostrand Reinhold; $26.50. July, 1981.
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179 pages; L.L. bound; Carnegie Press; $59.95. 1981. Circle 219 on Inquiry Card

Computer-Assisted Data Base Design by *George U. Hubbard.*

This book not only thoroughly explains the theoretical aspects, but also provides explicit directions on all data base design procedures. In addition to a practical design methodology it discusses the ways to automate the major portions of this methodology. However, all of the techniques can be utilized without computer assistance.

320 pages; 123 illustrations; 6 x 9; Van Nostrand Reinhold Data Processing Series; $24.95. August, 1981. Circle 220 on Inquiry Card

COMPUTER DESIGN
THE MAGAZINE OF COMPUTER BASED SYSTEMS

Designer's Bookcase

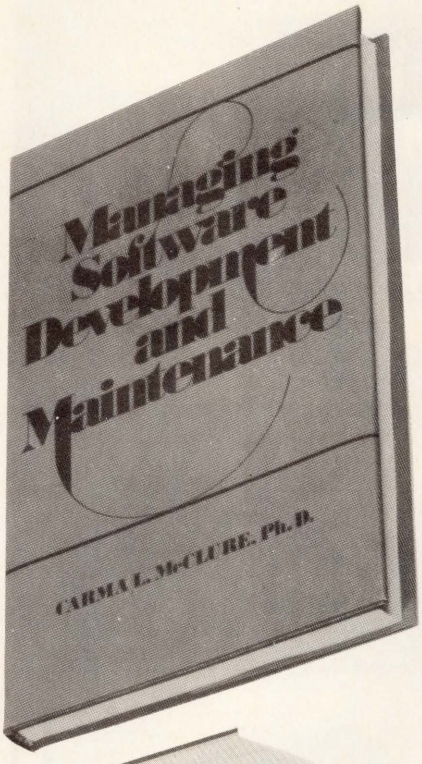
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Evaluating Data Base Management Systems by *Judy M. King.*

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296 pages; 57 illustrations; 6 x 9; Van Nostrand Reinhold Data Processing Series; $21.95. Publication date: July, 1981.

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248 pages; $16.95. 1978.

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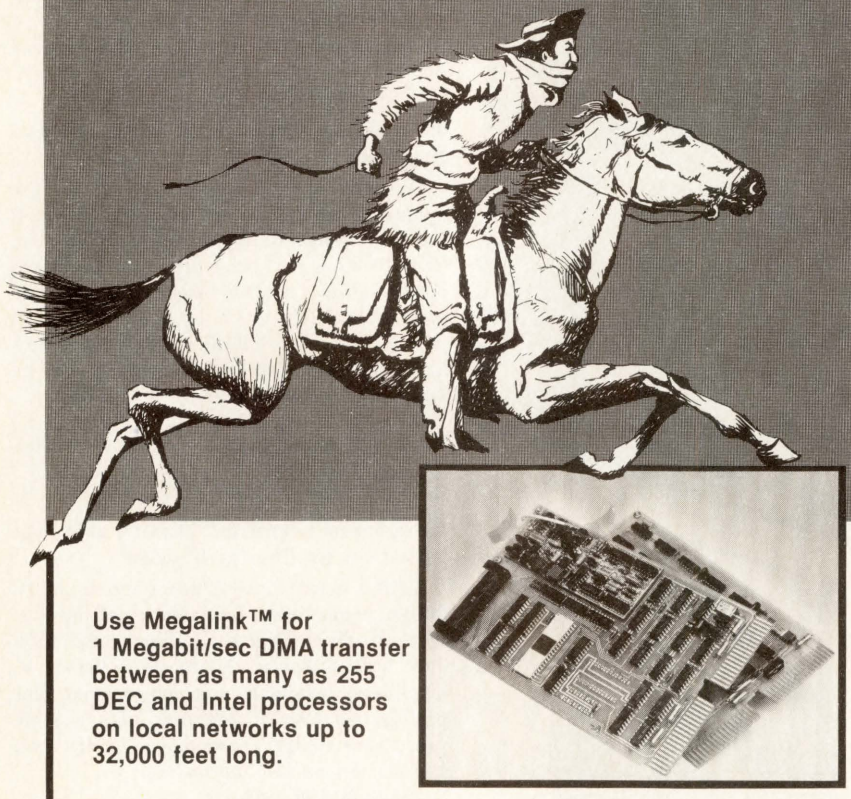
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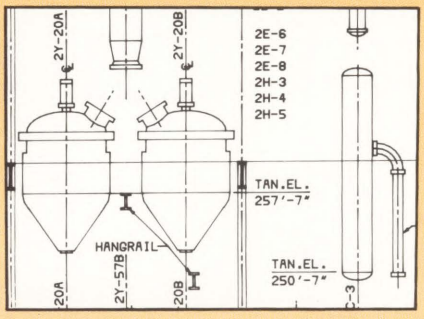


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